1. The skin effect governs the behavior of all conductors. As an example, Figure below depicts the series resistance of RG-58C/U coaxial cable plotted as a function of frequency. The plot uses log-log axes. Assume the center conductor radius \( r = 0.455 \) mm, and per-unit-length inductance \( L = 253 \) nH/m. The conductivity of copper is \( \sigma = 5.8 \times 10^7 \) S/m.

   a) Calculate the per-unit-length DC resistance of center conductor.
   
   b) Calculate frequency \( f_1 \) where skin depth approximately take effect on center conductor \( (R_{AC} > R_{DC}) \).
   
   c) Calculate frequency \( f_2 \) where \( \omega L > R_{copper} \).
2. For the per-unit-length representations of a lossless transmission line shown below in three structures, derive the transmission-line equations in the limit as $\Delta z \to 0$. Note that the total per-unit-length inductance and capacitance in each circuit are $l$ and $c$, respectively. This shows that the structure of the per-unit-length equivalent circuit is not important in the limit as $\Delta z \to 0$. 

![Diagram of per-unit-length representations](image)

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3. Sketch the input voltage to the line $V(0, t)$ and the load voltage $V(L, t)$ for the problem depicted in the figure below for $0 < t < 24 \text{ ns}$. What should these plots converge to in the steady state?
4. Highly mismatched lines in digital products can cause what appears to be “ringing” on the signal output from the line. This is often referred to as “overshoot” or “undershoot” and can cause digital logic errors. To simulate this we will investigate the problem shown in figure below. Two CMOS gates are connected by a transmission line as shown. A 5 V step function voltage of the first gate is applied.

a) Sketch the output voltage of the line (the input voltage to the load CMOS gate) for $0 < t < 9T$.

b) Use series matching and sketch the output voltage of the line for $0 < t < 9T$.

c) Use parallel matching to ground and sketch the output voltage of the line for $0 < t < 9T$.

d) Use both series matching and parallel matching to ground, then sketch the output voltage of the line for $0 < t < 9T$. 

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5. (Bonus) Use LTSPICE to confirm your answer for the four plots in problem 4.
6. It is somewhat common to find one source driving two or more transmission lines that are in parallel as illustrated in the figure below. Investigate this configuration by using LTSPICE to plot the load voltage $V_{L1}(t)$ at the open-circuited end of one of the lines for two values of $R_s$, $R_s = 25\,\Omega$ and $R_s = 50\,\Omega$.

a) What can you conclude about the choice of $R_s$ that provides complete matching at least of the line outputs?

b) Repeat this analysis, assuming the second line has a time delay of 1 ns instead.