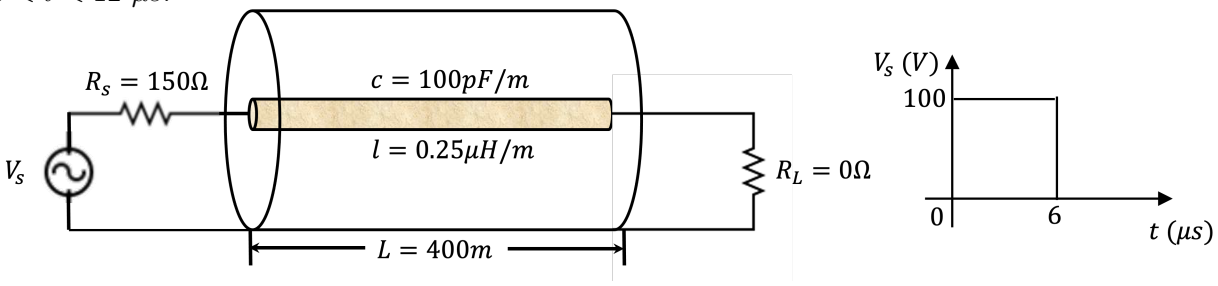
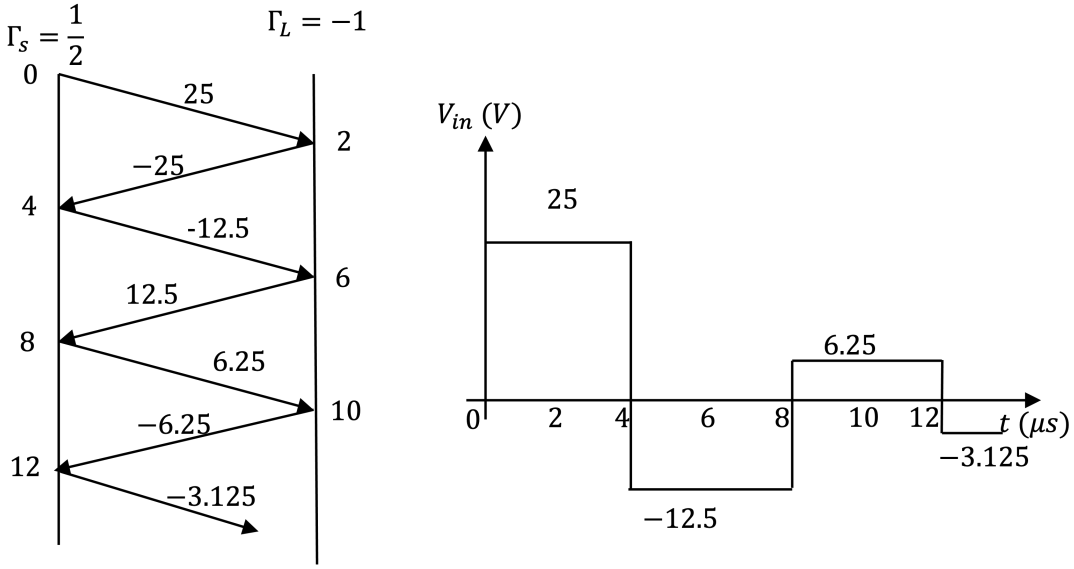
**ECE 498YVS-EMC** **Homework 4** **Due: Tuesday, Oct. 1, 2024, 11:59PM Central Time**

**Recommended Reading:** Paul: Chapter 4.

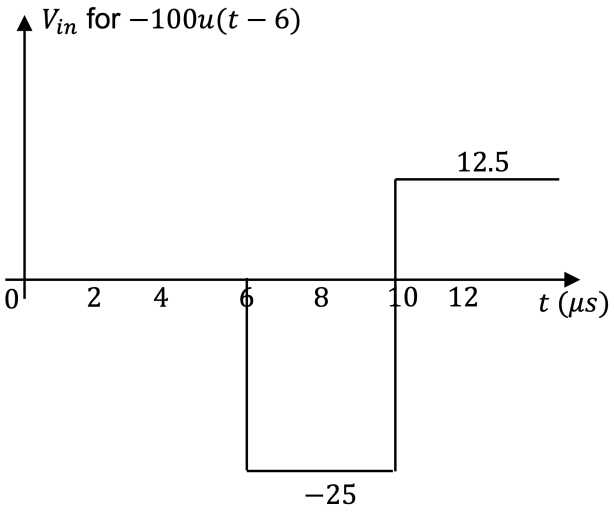
1. (Pulse width longer than the round-trip delay)
Consider a RG58U coaxial cable which is is specified by its per-unit-length capacitance and inductane: $c = 100\ pF/m$ and $l = 0.25\ \mu H/m$. The cable is connected to a source voltage of $100[u(t)-u(t-6\mu s)]$ V voltage source with duration of 6 $\mu s$. The source resistance $R_s = 150\ \Omega$, and the load end is short circuit ($R_L = 0\ \Omega$). Sketch the voltage at the input (source side) to the transmission line from $0 < t < 12\ \mu s$.



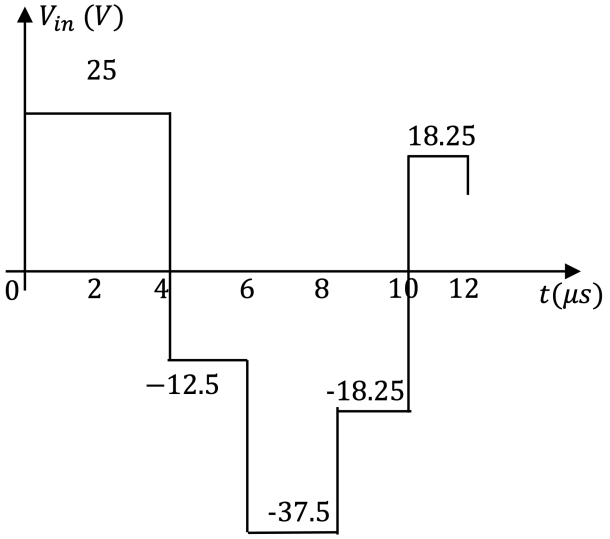

Solution:
The characteristic impedance of the coaxial cable is $Z_c = \sqrt{\frac{l}{c}} = \sqrt{\frac{0.25\times10^{-6}}{100\times10^{-12}}} = 50\ \Omega$
The propagation speed in the coax is $v_p = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{0.25\times10^{-6}\times100\times10^{-12}}} = 2\times10^8\ m/s$
The delay time of the coaxial cable is $T_d = L/v_p = \frac{400}{2\times10^8} = 2\ \mu s$
For the transmission line, the injection coefficient is $k = \frac{Z_c}{R_s+Z_c} = \frac{50}{150+50} = \frac{1}{4}$
Reflection coefficient at the source side is $\Gamma_s = \frac{R_s-Z_c}{R_s+Z_c} = \frac{150-50}{150+50} = \frac{1}{2}$
Reflection coefficient at the load side is $\Gamma_L = \frac{R_L-Z_c}{R_L+Z_c} = \frac{0-50}{0+50} = -1$
We first draw the bounce diagram for input voltage as $100u(t)$




The voltage output for $-100u(t-6\mu s)$ is

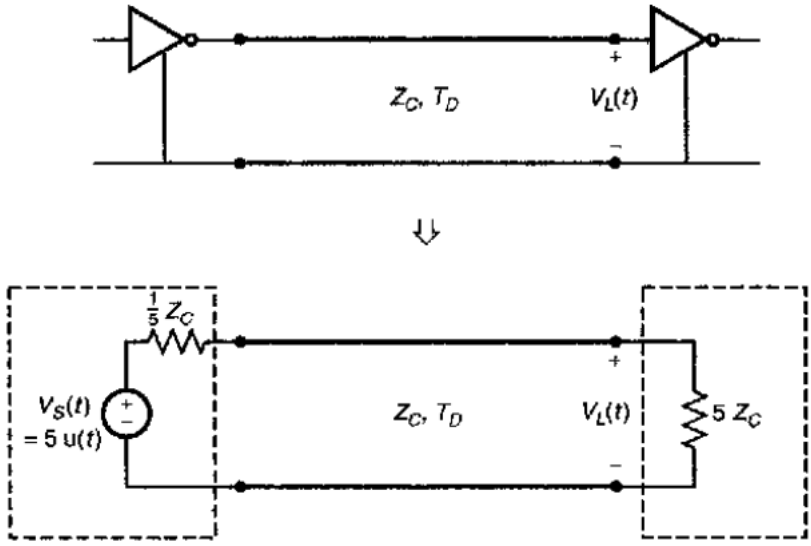



Add two voltage plots together,




2. Highly mismatched lines in digital products can cause what appears to be "ringing" on the signal output from the line. This is often referred to as "overshoot" or "undershoot" and can cause digital logic errors. To simulate this we will investigate the problem shown in figure below. Two CMOS gates are connected by a transmission line as shown. A 5 V step function voltage of the first gate is applied.
   a) Sketch the output voltage of the line (the input voltage to the load CMOS gate) for $0 < t < 9T$.
   b) Use series matching and sketch the output voltage of the line for $0 < t < 9T$.
   c) Use parallel matching to ground and sketch the output voltage of the line for $0 < t < 9T$.

d) Use both series matching and parallel matching to ground, then scketch the output voltage of the line for $0 < t < 9T$.



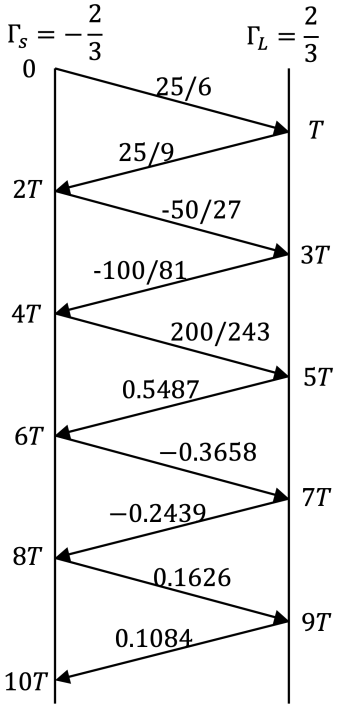

Solution:

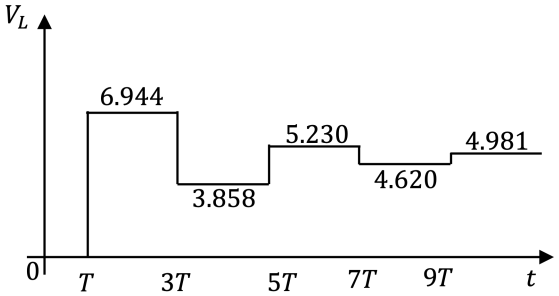
a) We first calculate three coefficients

Injection coefficients $k = \frac{Z_c}{\frac{1}{5}Z_c + Z_c} = \frac{5}{6}$

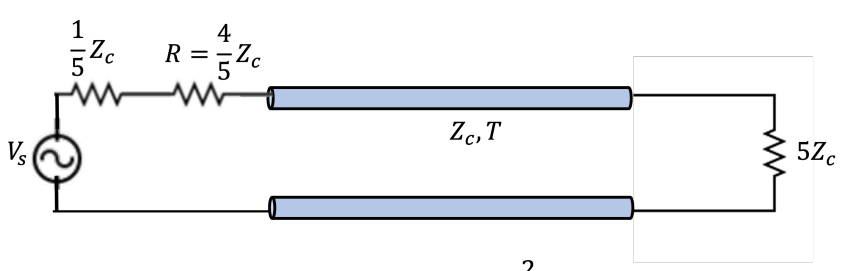
Reflection coefficient at source side $\Gamma_s = \frac{\frac{1}{5}Z_c - Z_c}{\frac{1}{5}Z_c + Z_c} = -\frac{2}{3}$

Reflection coefficient at load side $\Gamma_L = \frac{5Z_c - Z_c}{5Z_c + Z_c} = \frac{2}{3}$



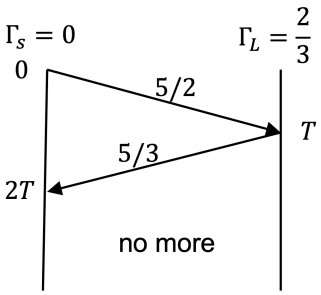

b) Series termination at the source, we have $R = Z_c - \frac{1}{5}Z_c = \frac{4}{5}Z_c$

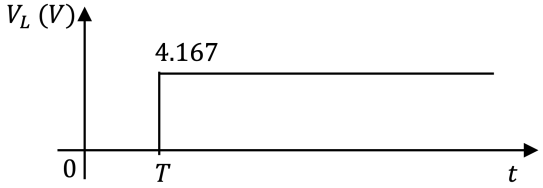



$$k = \frac{Z_c}{Z_c + Z_c} = \frac{1}{2}$$

$$\Gamma_s = \frac{Z_c - Z_c}{Z_c + Z_c} = 0$$

$$\Gamma_L = \frac{5Z_c - Z_c}{5Z_c + Z_c} = \frac{2}{3}$$



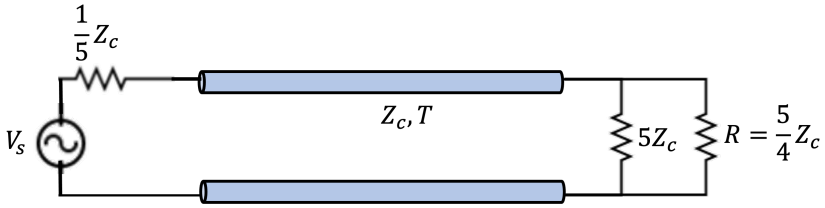




c) Parallel termination to ground, we need to match load impedance to characteristic impedance of the line

$$Z_L = R//5Z_c = Z_c$$

$$\frac{1}{R} + \frac{1}{5Z_c} = \frac{1}{Z_c}$$

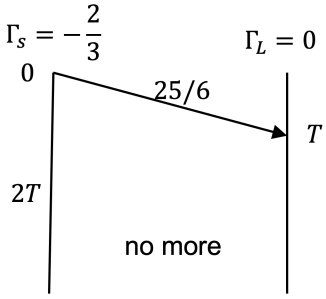
$$R = \frac{5}{4}Z_c$$

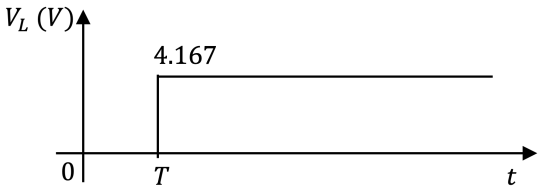



$$k = \frac{Z_c}{\frac{1}{5}Z_c + Z_c} = \frac{5}{6}$$

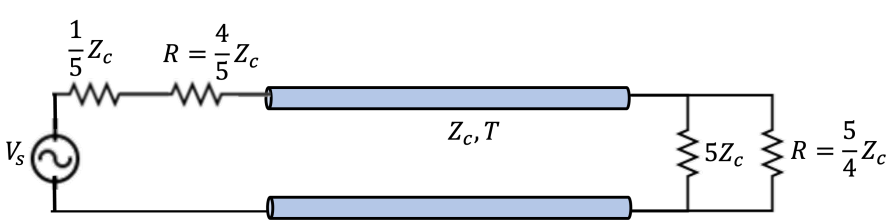
$$\Gamma_s = \frac{\frac{1}{5}Z_c - Z_c}{\frac{1}{5}Z_c + Z_c} = -\frac{2}{3}$$

$$\Gamma_L = 0$$



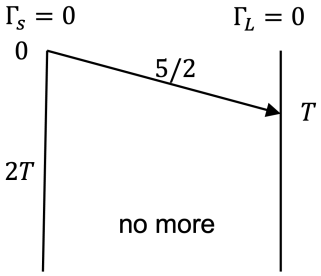

d) Both series and parallel termination, we have

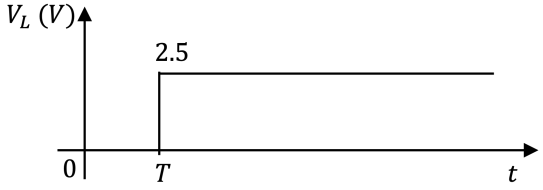



$$k = \frac{Z_c}{Z_c + Z_c} = \frac{1}{2}$$

$$\Gamma_s = \frac{Z_c - Z_c}{Z_c + Z_c} = 0$$

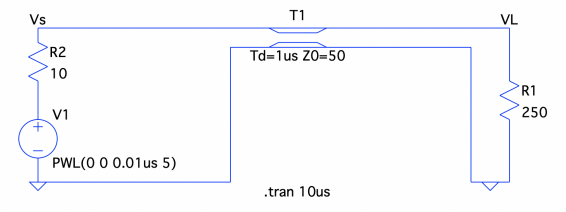
$$\Gamma_L = \frac{Z_c - Z_c}{Z_c + Z_c} = 0$$

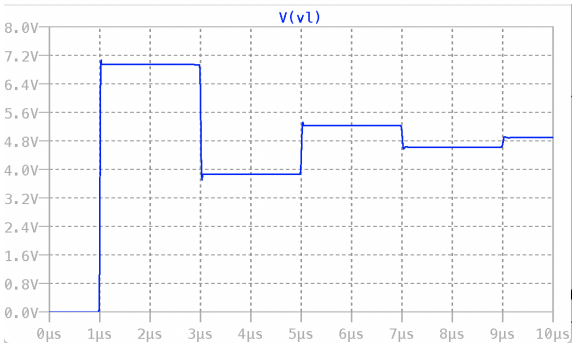


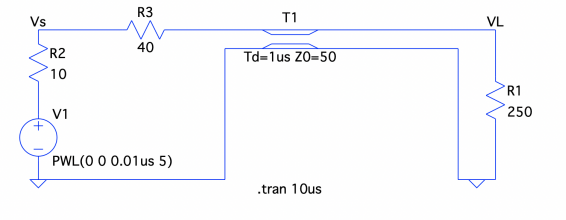
3. (For graduate students, 5 extra points for undergrads) Use LTSPICE to confirm your answer for the four plots in problem 2.

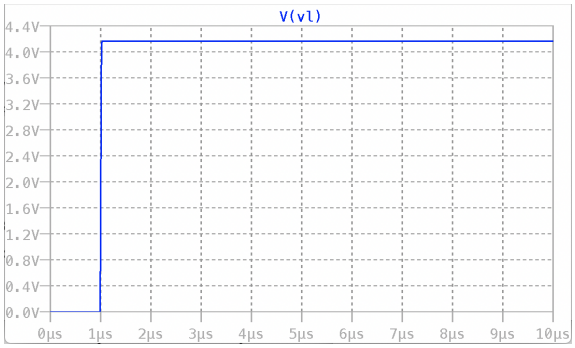
Solution:
a)



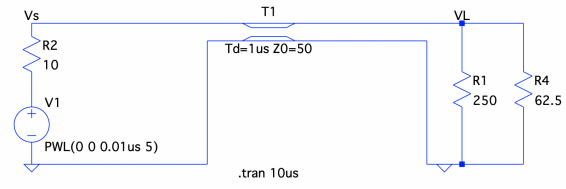



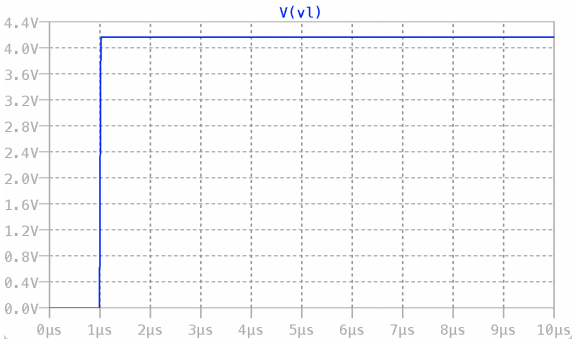

b) parallel termination to ground



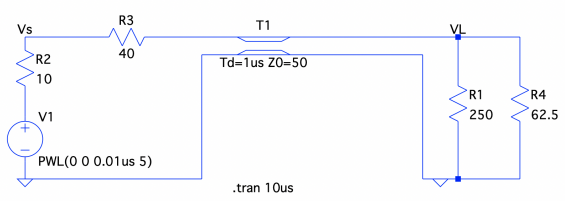



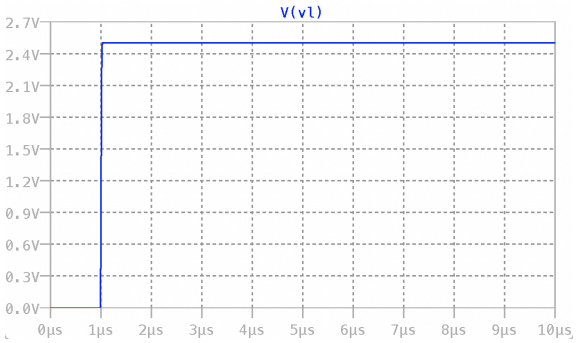

c) series termination




d) Both series and parallel termination

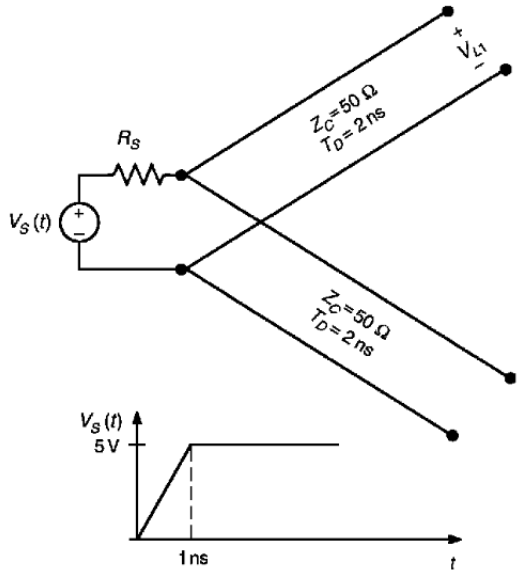


4. It is somewhat common to find one source driving two or more transmission lines that are in parallel as illustrated in the figure below. Investigate this configuration by using LTSPICE to plot the load voltage $V_{L1}(t)$ at the open-circuited end of one of the lines for two values of $R_s$, $R_s = 25\Omega$ and $R_s = 50\Omega$.

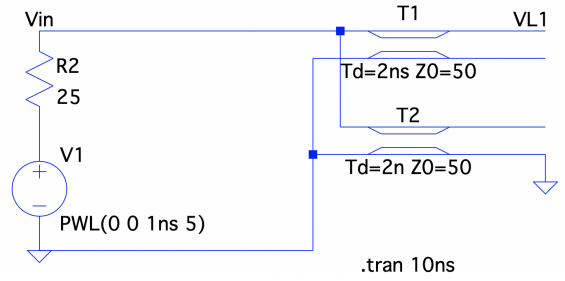
   a) What can you conclude about the choice of $R_s$ that provides complete matching at least of the line outputs?

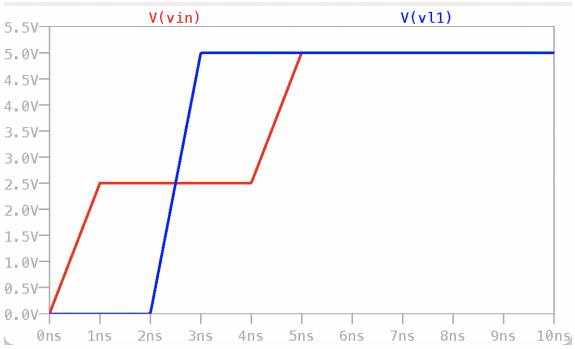
   b) Repeat this analysis, asumming the second line has a time delay of 1 ns instead.

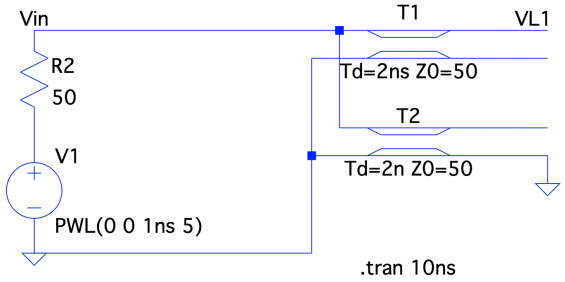


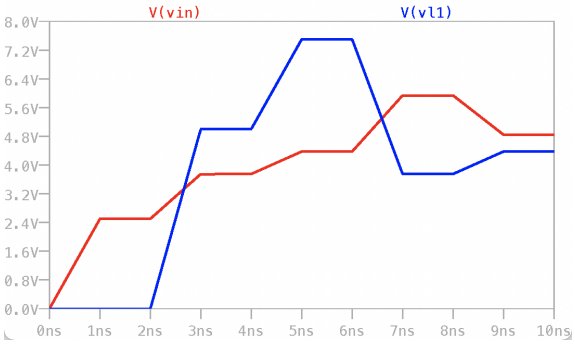

Solution:

a) We can compare the voltage at line parallel connection and load side for two values of $R_s$, 25 Ω and 50 Ω respectively.



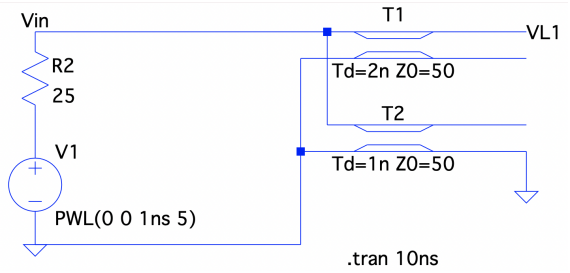



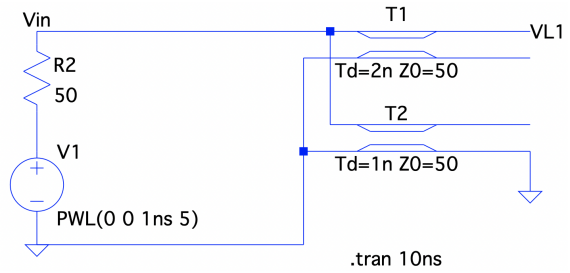



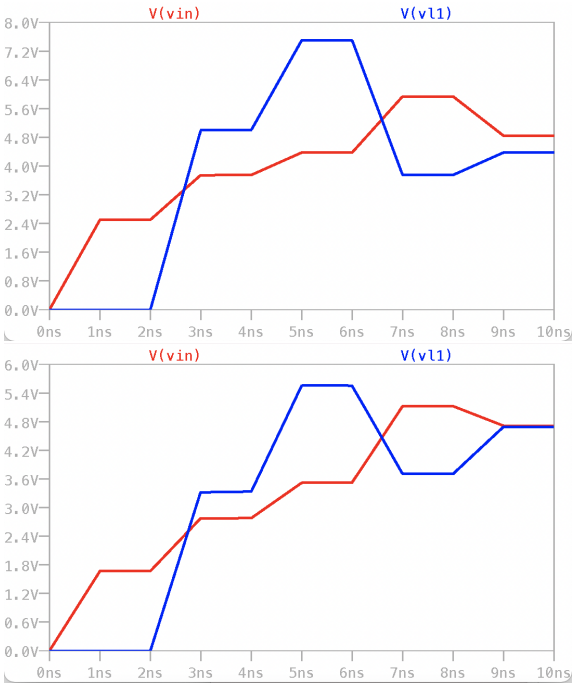



The two transmission lines are connected in parallel. The input impedance is $50\Omega//50\Omega = 25\Omega$. So when $R_s = 25\ \Omega$, the line has matched impedance.

b) The delay time of the 2nd line is changed to 1ns. The circuit diagram and voltage $V_{L1}$ are




5. A #32 AWG solid round copper wire has a diameter of 0.008 inches. Conductivity of cooper is $\sigma = 5.8 \times 10^7$ S/m.
   a) What is the per-unit length dc resistance of the wire?
   b) Determine the skin depth of the wire at 1MHz and 1GHz.
   c) Determine the frequency $f_1$ where the internal inductance of the wire begins to decrease due to skin effect.
   d) Calculate the internal inductance of this wire at 100 MHz.

   Solution:
   a) radius $r = 0.008/2\ inch = 0.0001016\ m$
   per unit length DC resistance of the wire is

$$R_{DC} = \frac{1}{\sigma A} = \frac{1}{5.8 \times 10^7 \times (0.0001016)^2} = \boxed{0.532\ \Omega/m}$$

   b) Skin depth at 1MHz is

$$\delta_{1MHz} = \frac{1}{\sqrt{\pi f \mu \sigma}} = \frac{1}{\sqrt{\pi \times 10^6 \times 4\pi \times 10^{-7} \times 5.8 \times 10^7}} = \boxed{0.0661\ mm}$$

   Skin depth at 1GHz is

$$\delta_{1MHz} = \frac{1}{\sqrt{\pi f \mu \sigma}} = \frac{1}{\sqrt{\pi \times 10^9 \times 4\pi \times 10^{-7} \times 5.8 \times 10^7}} = \boxed{2.09\ \mu m}$$

c) the frequency $f_1 \approx 2\delta$ where $\delta$is the skin depth

$$r = \frac{2}{\sqrt{\pi f_1 \mu \sigma}}$$

$$f_1 = \frac{4}{\pi \mu \sigma r^2} = \boxed{1.69\ MHz}$$

d) Internal inductance at 100 MHz is

$$l_{hf} = \frac{\mu \delta}{4\pi r} = \frac{1}{4\pi r}\sqrt{\frac{\mu}{\pi \sigma f}} = \boxed{6.50\ nH/m}$$

6. (15 bonus points for grads only) Read the paper about partial inductance (link) and answer the following questions:
   a) Explain why partial inductance is necessary in high-speed digital circuits instead of relying solely on loop inductance.
   b) Using the example of a PCB with traces and ground planes, what is ground bounce and power rail collapse?
   c) Describe how partial inductance can help reduce ground bounce.
   d) Discussion: In a complex PCB design, how would you apply the concept of partial inductance to minimize electromagnetic interference (EMI)?
   Solution:
   a) On page 41, Prof. Paul explained a list of problems with using loop inductance and why partial inductance is preferred:

   * To compute loop inductance, you MUST determine the RETURN PATH for the loop current. That's virtually impossible for most PCBs.
   * There is NO unique return path for ALL frequencies. At lower frequencies a current will return to its source along one path, while at higher frequencies that very same current will return along another path.
   * Even IF you could determine a unique loop for the current, where would you place the loop inductance in that loop? There is NO UNIQUE answer!
   * You cannot compute ground bounce and power rail collapse UNIQUELY with loop inductance.
   * Partial inductance solves ALL these problems. You just compute self and mutual partial inductances for all conductor segments of concern, place the self and mutual partial inductances in those conductor segments, and "turn the crank" by simply analyzing the resulting circuit. With this equivalent circuit you don't need to "guess" where the return for the current goes; you determine it from the equivalent circuit.

   b) Ground bounce occurs when the voltage at the "ground" pin of an IC or circuit fluctuates, rather than staying at the expected zero-voltage level. This happens due to the inductance of the ground path, which causes a voltage drop when there is a rapid change in current.
   Power rail collapse occurs when the voltage on the power supply line (the "power rail") drops instead of staying at VDD due to inductive effects in the power distribution network.

   c) Partial inductance allows us to calculate the inductance of individual sections of the ground trace. By pinpointing sections of the ground path with higher partial inductance, you can take steps to reduce the ground bounce (which is due to inductive effects $Z = j\omega L_{partial}$) in those specific areas.

   d) In a complex PCB design, partial inductance can be applied to minimize electromagnetic interference (EMI) in the following ways:
   * Reducing loop area (e.g., by placing traces closer together or near a ground plane), the partial inductance is reduced, which will reduce the magnetic field.
   * Using ground and power planes to lower the inductance of return paths.
   * Managing mutual inductance between parallel wires (e.g. by running differential wires in parallel over long distances), which will also reduce inductive coupling between traces and reducing EMI.

* Use partial inductance to determine where to put decoupling capacitors. By providing low-inductance paths for high-frequency currents close to critical components, decoupling capacitors help suppress voltage spikes and reduce EMI.