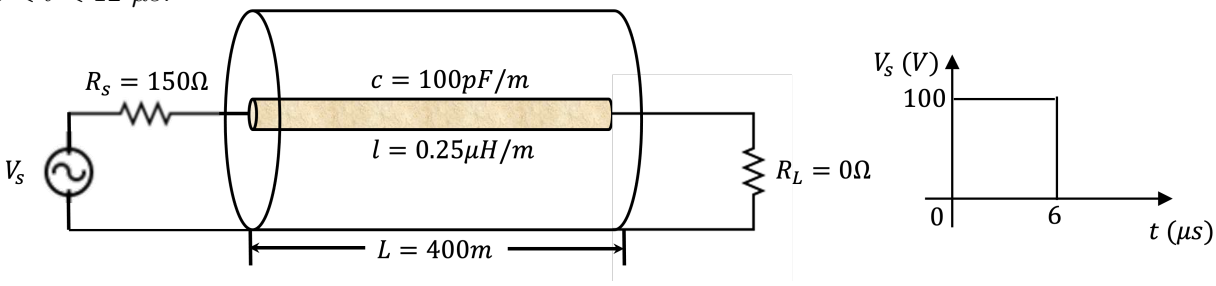
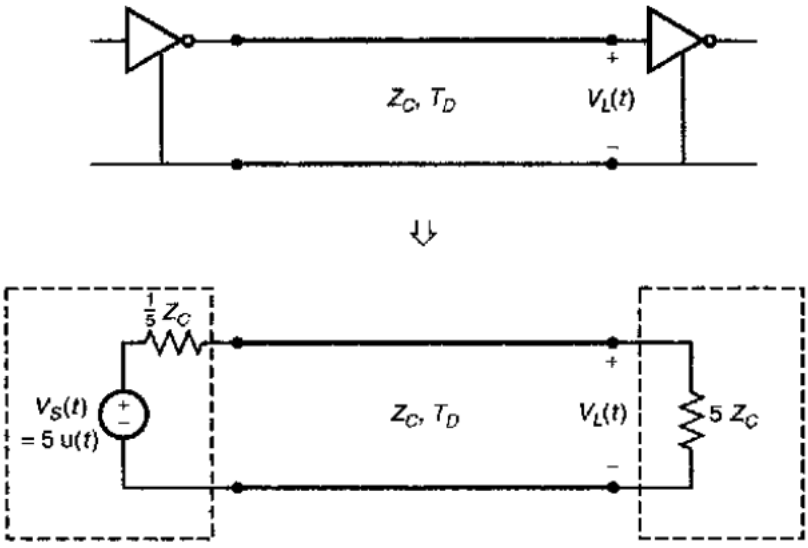
ECE 498YVS-EMC Homework 4 Due: Thursday, September 26, 2024, 11:59PM Central Time

Recommended Reading: Paul: Chapter 4, selected Chapter 5.

1. (Pulse width longer than the round-trip delay)
   Consider a RG58U coaxial cable which is is specified by its per-unit-length capacitance and inductance: $c = 100\ pF/m$ and $l = 0.25\ \mu H/m$. The cable is connected to a source voltage of $100[u(t) - u(t - 6\mu s)]$ V voltage source with duration of 6 μs. The source resistance $R_s = 150\ \Omega$, and the load end is short circuit ($R_L = 0\ \Omega$). Sketch the voltage at the input (source side) to the transmission line from $0 < t < 12\ \mu s$.



2. Highly mismatched lines in digital products can cause what appears to be "ringing" on the signal output from the line. This is often referred to as "overshoot" or "undershoot" and can cause digital logic errors. To simulate this we will investigate the problem shown in figure below. Two CMOS gates are connected by a transmission line as shown. A 5 V step function voltage of the first gate is applied.
   a) Sketch the output voltage of the line (the input voltage to the load CMOS gate) for $0 < t < 9T$.
   b) Use series matching and sketch the output voltage of the line for $0 < t < 9T$.
   c) Use parallel matching to ground and sketch the output voltage of the line for $0 < t < 9T$.
   d) Use both series matching and parallel matching to ground, then sketch the output voltage of the line for $0 < t < 9T$.

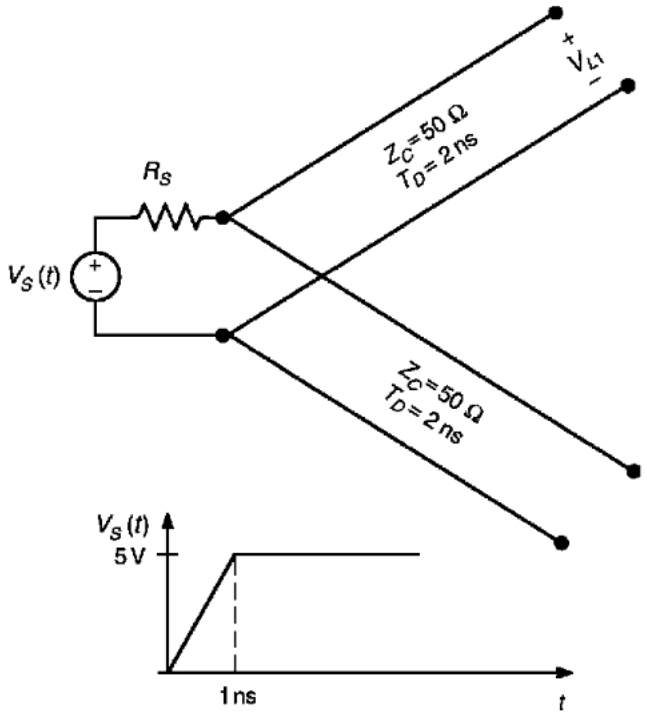


3. (For graduate students, 5 extra points for undergrads) Use LTSPICE to confirm your answer for the four plots in problem 2.

4. It is somewhat common to find one source driving two or more transmission lines that are in parallel as illustrated in the figure below. Investigate this configuration by using LTSPICE to plot the load voltage $V_{L1}(t)$ at the open-circuited end of one of the lines for two values of R_s, $R_s = 25\Omega$ and $R_s = 50\Omega$.

   a) What can you conclude about the choice of R_s that provides complete matching at least of the line outputs?

   b) Repeat this analysis, assuming the second line has a time delay of 1 ns instead.



5. A #32 AWG solid round copper wire has a diameter of 0.008 inches. Conductivity of cooper is $\sigma = 5.8 \times 10^7$ S/m.
   a) What is the per-unit length dc resistance of the wire?
   b) Determine the skin depth of the wire at 1MHz and 1GHz.
   c) Determine the frequency f_1 where the internal inductance of the wire begins to decrease due to skin effect.
   d) Calculate the internal inductance of this wire at 100 MHz.

6. (15 extra points for grads only) Read the paper about partial inductance (link) and answer the following questions:
   a) Explain why partial inductance is necessary in high-speed digital circuits instead of relying solely on loop inductance.
   b) Using the example of a PCB with traces and ground planes, what is ground bounce and power rail collapse? Describe how partial inductance can help reduce ground bounce.
   c) Discussion: In a complex PCB design, how would you apply the concept of partial inductance to minimize electromagnetic interference (EMI)?