University of Illinois at Urbana-Champaign
Department of Electrical and Computer Engineering

ECE 482 Fall Semester 2018 Course Information

Class Meetings: 3 PM – 3:50 PM, MWF, 2017 ECE Building
Instructor: Professor Naresh Shanbhag
Office Hours: Tuesday and Thursday – 2:00 PM – 3:00 PM, 414 CSL
Email: shanbhag@illinois.edu

Teaching Assistants:
Hassan Dbouk
Email: hdbouk2@illinois.edu
Office Hours:
Monday 1:00 PM – 2:00 PM and Wednesday 10:00 AM – 11:00 AM, Room: 3034 ECE Building
Siyu Liu
Email: siyuliu3@illinois.edu
Office Hours:
Friday 11:00 AM – 12:00 AM, Room: 5034 ECE Building

Textbook (required)

J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits: A Design Perspective, Second Edition,* Prentice Hall, 2003.
Course notes by instructor will be provided as a supplement to the text.

Other Reference Books (on reserve at Grainger Engineering Library)

A. Vladimirescu, *The Spice Book*, John Wiley & Sons, 1994.
D. Hodges, H. Jackson and R. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology, Third Edition*, McGraw-Hill, 2004.
S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits, Third Edition*, McGraw-Hill, 2003.
K. Bernstein *et al.*, *High Speed CMOS Design Styles*, Kluwer, 1998.
N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, 2nd Ed.*, Addison Wesley, 1993.

Grading

- Weekly Homework 15%

  Homework is due by 5:00 PM on Wednesdays in dropbox #66 on the 3rd floor of ECEB. Late homework will not be accepted. Homework solutions will be posted on the class web page. The lowest score will be discarded in calculating the course grade. Students can use this flexibility to accommodate interview travel or unanticipated illness. A student who is seriously ill for more than 7 consecutive days should contact the instructor so as not to be penalized for missing more than one assignment.

  Students are permitted to engage in discussion of the course material and approaches to solving the homework problems with each other. Ultimately, however, homework is to be completed individually. Plagiarized work will receive a score of zero and the student will be reported to the ECE department for possible disciplinary action. The lowest score will be discarded in calculating the course grade. Students can use this flexibility to accommodate interview travel or unanticipated illness.
- First Midterm Exam 15%
- Second Midterm Exam 15%
- Final Exam 30%
- Design Project Report 25%

Students will work in instructor-assigned groups. Reports will be due in class on Dec. 15. All the members of a group will receive the same grade except in the case that a group member does not make a good faith effort to contribute significantly. The design project assignment will be provided around mid/end-October.

ECE482 Web Site and Q&A Forum on Piazza

http://courses.engr.illinois.edu/ece482/

Check the web site a few times per week; this is where all announcements will be posted, including corrections to homework assignments and changes to office hours. It is your responsibility to check the website regularly. Tutorial material will also be available on the class web site.

http://piazza.com/illinois/fall2018/ece482/home

All questions regarding the homework assignments, homework solutions or exams should be posted to piazza. Registered class members should already be registered for this on-line forum; otherwise, clicking the above link will allow you to join. Piazza is the primary means of staff-student communication outside of class hours. The TAs or instructor will check this forum multiple times per day and will post responses to any queries. Email should be used only for matters of a personal nature.

Weekly reading assignments:

A reading assignment will be written at the top of each problem set. Problem sets (i.e., homework assignments) will be posted each Wednesday at 4:00 PM. It is your responsibility to download the problem set and make note of the reading assignment. Paper copies of the assignments will not be provided after the first week of class.

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ECE 482 Syllabus - Fall Semester 2018

Lecture	Date	Topic	Reading
1	27-Aug	Introduction to ECE 482	Ch. 1, Insert B, Notes-1
2	29-Aug	Overview of Digital Circuits	Sec 3.3, Notes-1
3	31-Aug	The MOSFET Threshold Voltage	Sec 3.3, Notes-2
	Labor Day (9/3/2018)		
4	5-Sep	The MOSFET I-V model	Sec 3.3 - 3.5, Notes-2
5	7-Sep	Subthreshold Conduction	Sec 3.3 - 3.5, Notes-2
6	10-Sep	MOSFET DC Analysis	Sec 3.3 - 3.5, Notes-2
7	12-Sep	IC Fabrication, Layout, Design Rules, CAD tools	Sec 2.1 - 2.3, Insert A, Sec 3.3.4
8	14-Sep	MOSFET Capacitances	Sec 4.1 - 4.3.1, Notes-2
9	17-Sep	Static Behavior of Inverter	Sec 5.2 - 5.3, Notes-3
10	19-Sep	Calulating Inverter Delay	Sec 5.4.1-2, Notes-3
11	21-Sep	Sizing Inverter for minimum delay	Sec 5.4.3, Notes-3
12	24-Sep	Sizing Inverter Chain for minimum delay	Sec 5.4.3, Notes-3
13	26-Sep	Inverter Power and Energy	Sec 5.5, Notes-3
14	28-Sep	CMOS Logic Schematic & Layouts	Sec 6.2.1, Insert D
15	1-Oct	CMOS Logic VTC and Delay Calculations	Sec 6.2.1
16	3-Oct	CMOS Logic Energy and Power	Sec 6.2.1
17	5-Oct	MIDTERM 1	
18	8-Oct	Ratioed Logic	Sec 6.2.2
19	10-Oct	Pass-Transistor Logic	Sec 6.2.3
20	12-Oct	Domino Logic	Sec 6.3 - 6.5
21	15-Oct	Signal Integrity Issues in Dynamic Logic	Sec 6.3 - 6.5
22	17-Oct	Sizing Logic Networks for minimum delay - Logical Effort	Sec 6.2.1
23	19-Oct	Logical Effort	Sec 6.2.1
24	22-Oct	Synchronous System Design	Sec 7.1
25	24-Oct	Static Latches and Registers - D,MSFF,CC	Sec 7.2
26	26-Oct	Dynamic Latches and Registers - PT, TSPC, pulse-based	Sec 7.3
27	29-Oct	Interconnect RLC and Delay Models	Ch. 4, Sec 9.2
28	31-Oct	Minimzing Interconnect Delay - Buffer Insertion	Sec 9.3
29	2-Nov	Adder Design	Sec 11.3
30	5-Nov	Semiconductor Memory Architectures	12.1 - 12.2.1
31	7-Nov	CMOS ROM	12.2.1 - 12.2.2, 12.3
32	9-Nov	Non-voltatile Memory - Flash Architecture	
33	12-Nov	6T SRAM	Sec 12.2.3
34	14-Nov	6T SRAM	Sec 12.2.3
35	16-Nov	MIDTERM 2	
	Thanksgiving Break (11/17/2018 - 11/25/2018)		
36	26-Nov	Sense Amplifiers	12.3
37	28-Nov	Sense Amplifiers - The StrongARM Latch	12.3
38	30-Nov	Peripherals - Voltage references, Charge Pumps	12.3
39	3-Dec	Peripherals - Address Decoders	12.3
40	5-Dec	DRAM	Sec 12.2.3
41	7-Dec	DRAM Sensing	Sec 12.2.3
42	10-Dec	Advanced Topics - 8T, 10T, CAM, subthreshold	
43	12-Dec	Advanced Topics - variability & robust design	
	Reading Day (12/13/2018)		