

Transient Response of Transmission Lines

Prof. Victoria Shao

Outlines

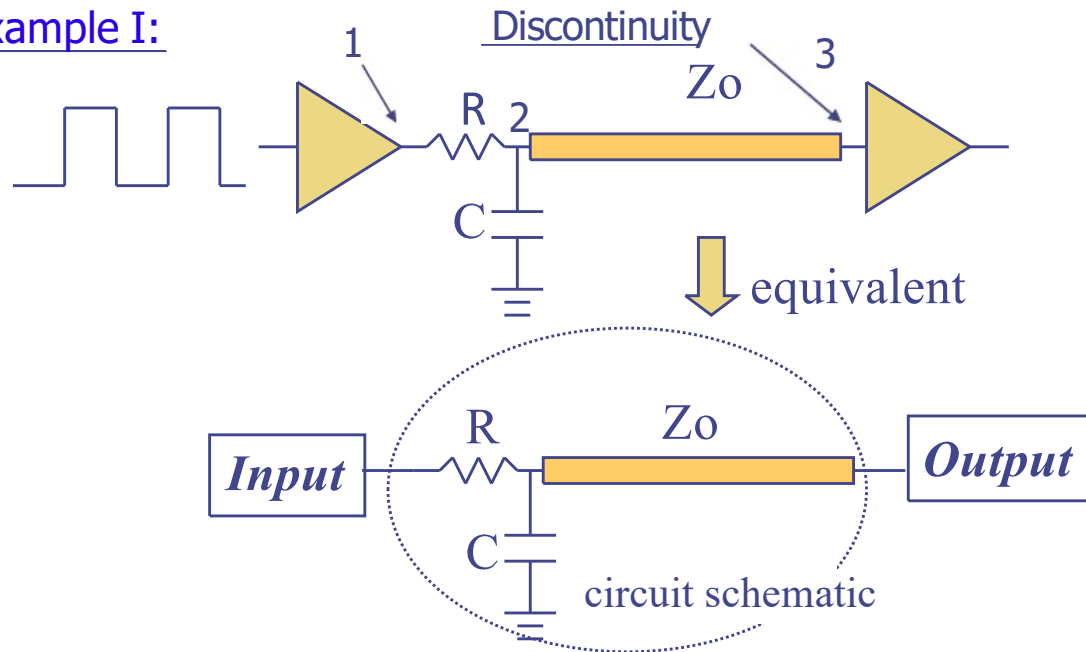
- Why do we learn the transient response of transmission line ?
 - Discontinuity of signal trace
 - Bounce diagram and examples
- Reflection at Discontinuity
 - Resistive discontinuity
 - Reactive discontinuity
 - Capacitive discontinuity
- Termination



1 Why do we learn transient response ?

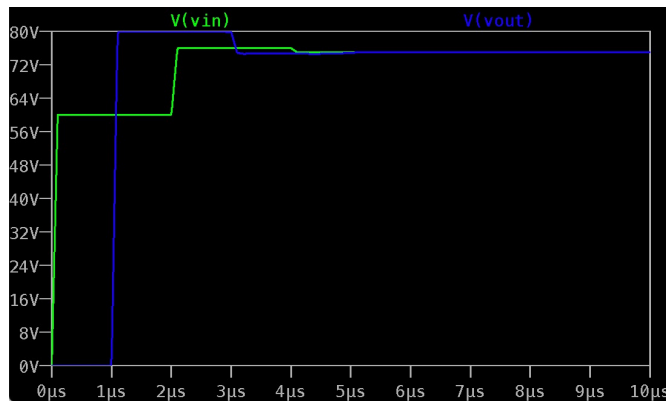
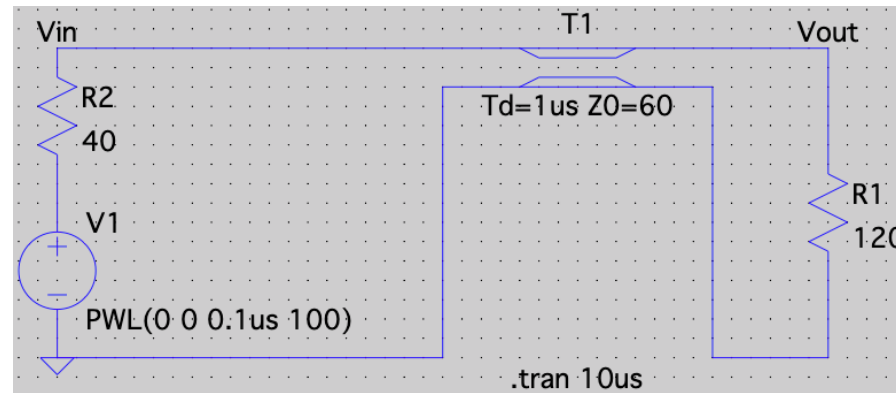
- Discontinuity can not be avoided in the high speed digital circuits.

Example I:

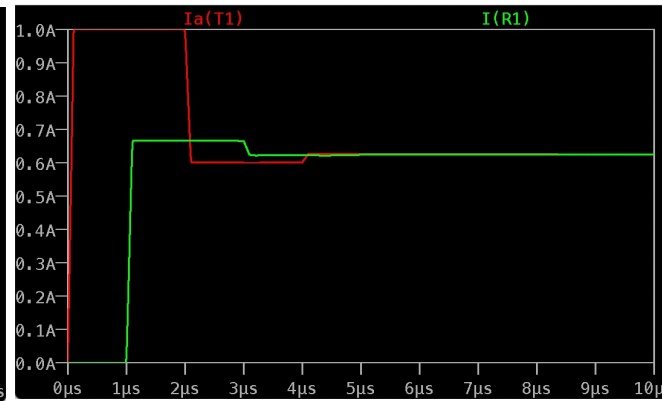


LTSPICE Example

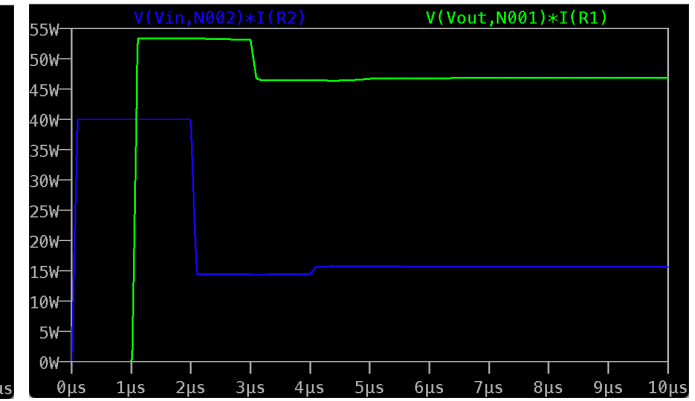
Bounce_Diagram_1line.asc



Voltage



Current



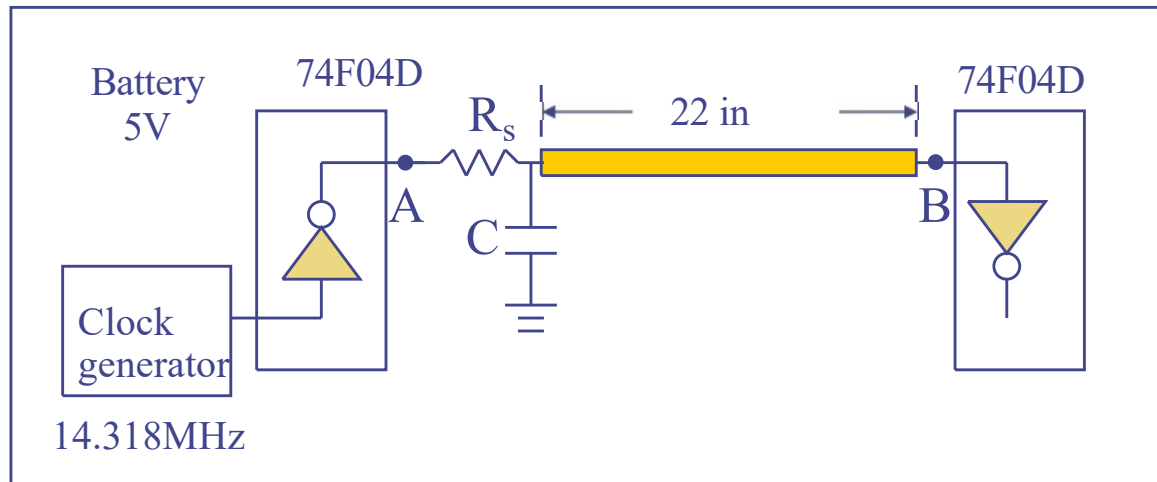
Power



Why do we learn transient response ? (Example: I)

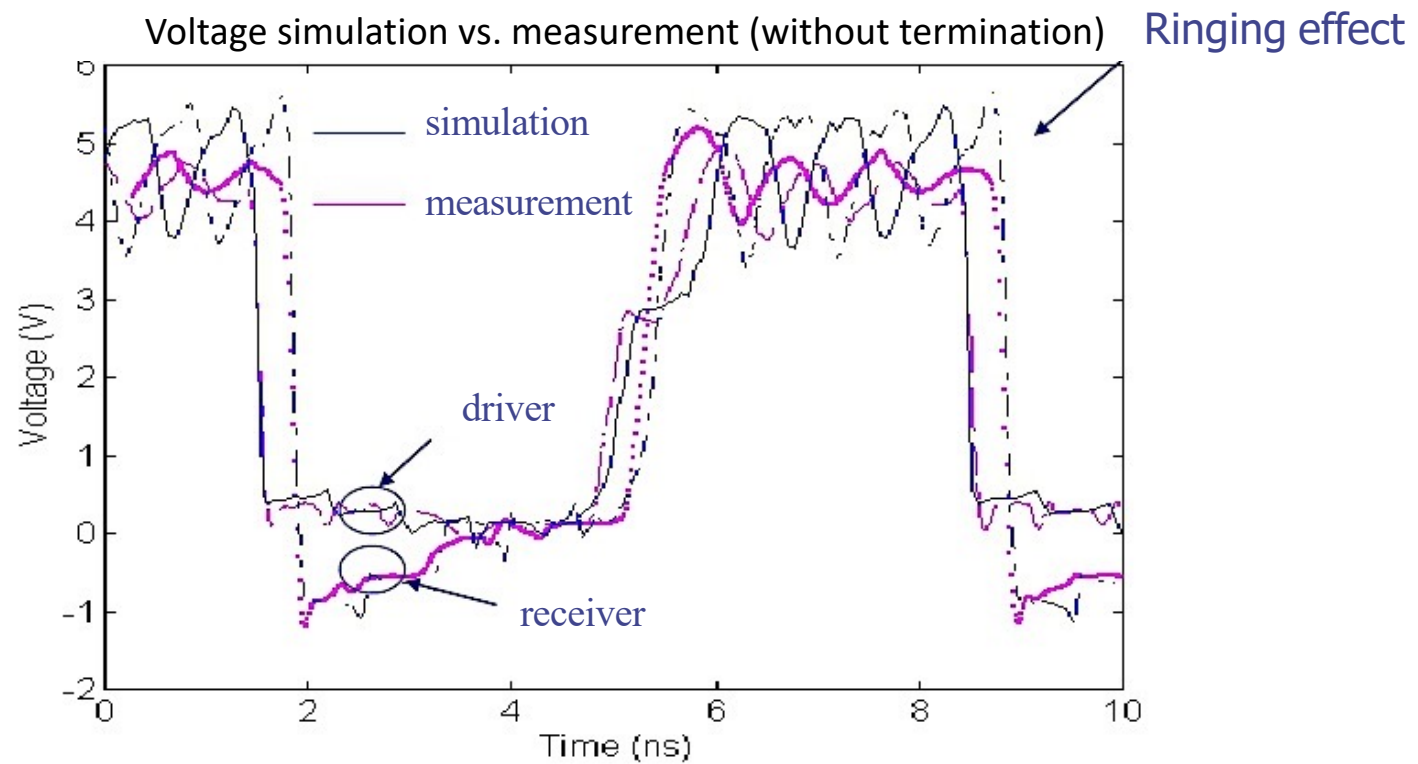
◆ Experimental setup

- PCB: 22*3in (L*W), $h=0.059$ in, $\epsilon_r=4.5$



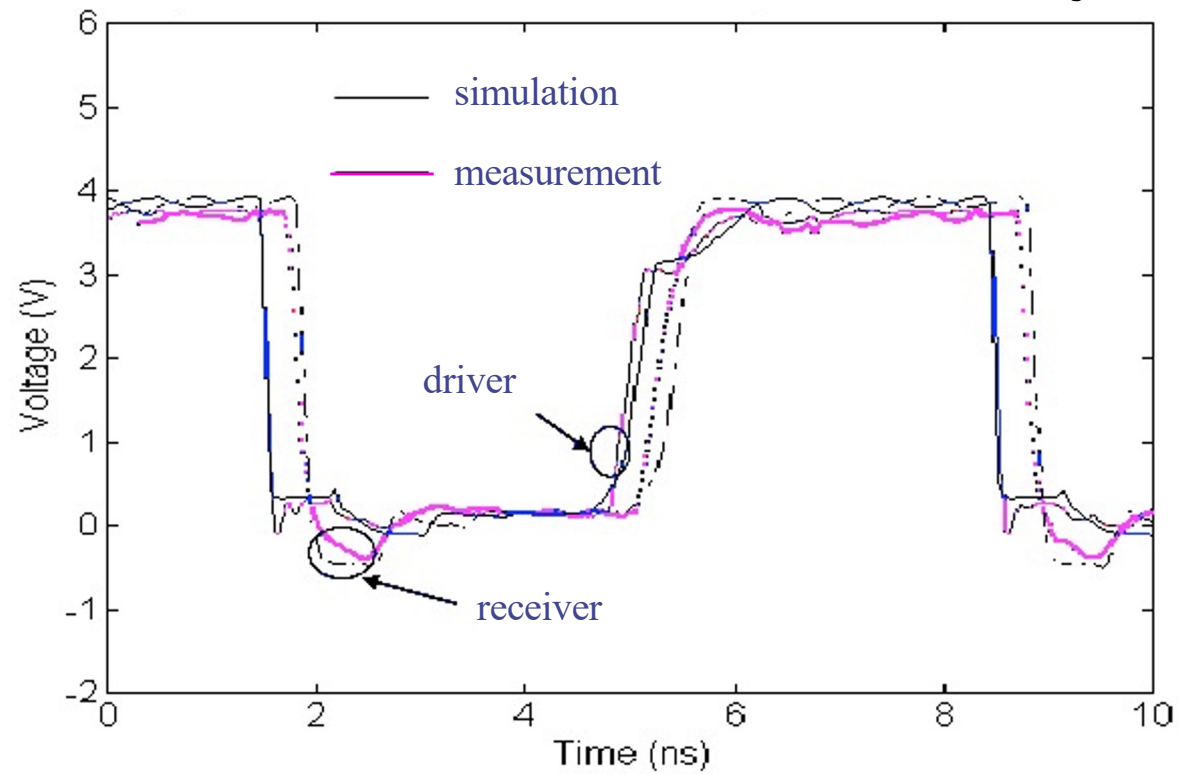
- Measuring the driver (A) / receiver(B) output with digital oscilloscope (BW=500MHz)

Why do we learn transient response ? (Example: I)



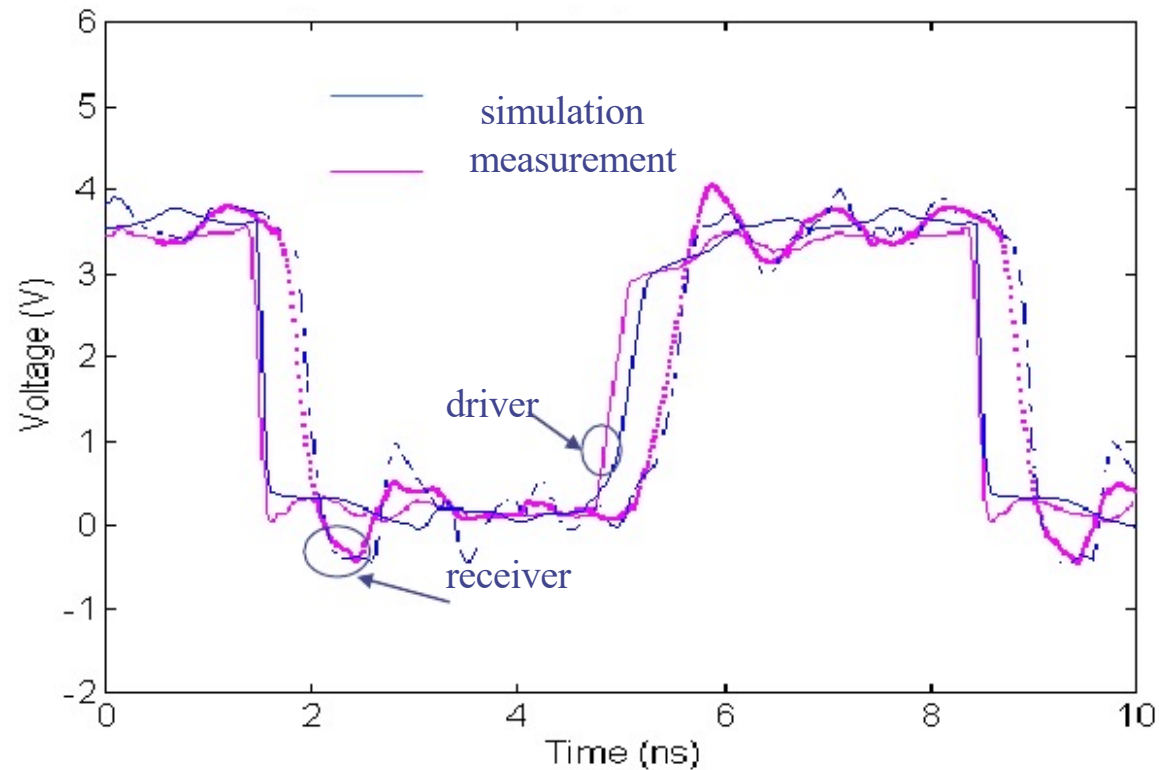
Why do we learn transient response ? (Example: I)

Voltage simulation vs. measurement (with source termination $R_s = 62 \Omega$)



Why do we learn transient response ? (Example: I)

Voltage simulation vs. measurement (with source termination $R_s = 62 \Omega$, $C = 22\text{pF}$)



1 Why do we learn transient response ?

(Rule of Thumb)

Rule of Thumb:

Transmission Line effect should be considered when

$$\text{Length (of transmission)} > \frac{1}{6} \frac{T_{rise}}{T_d}$$

For example:

Rambus 28Ω signal line, $T_d \approx 170$ ps/ inch

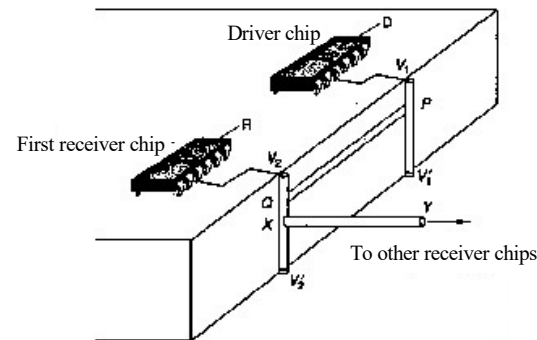
For 200 ps rising edge, Length ≈ 0.49 cm !!

The reflection effect will occur when the Rambus signal Length is longer than 5mm!

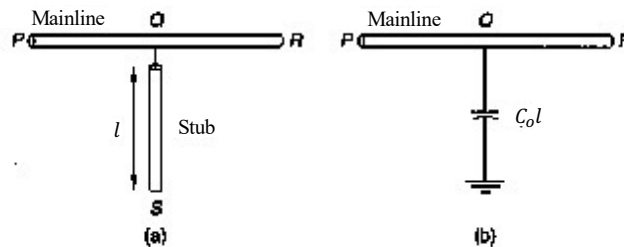


1 Why do we learn transient response ?

- Discontinuity of signal trace (such as stub, via, ..)



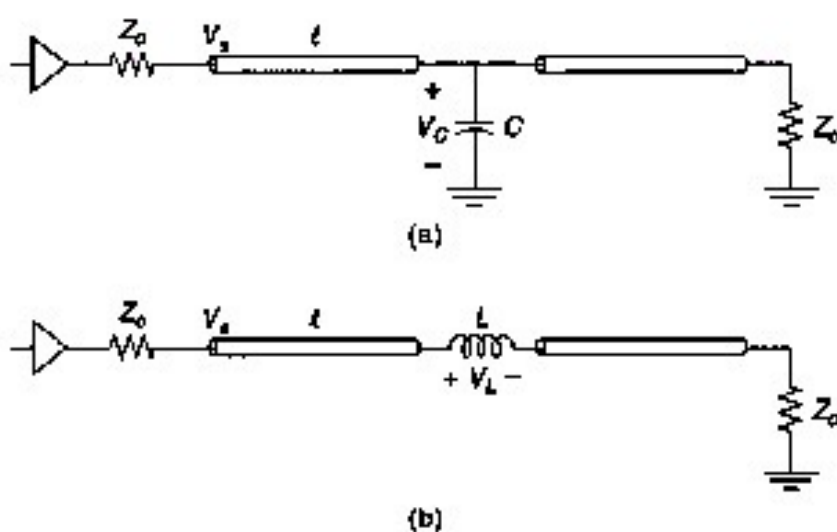
DV₁, RV₂ are metals on the board surface.
 PQ, XY are board internal traces.
 V₁V₁', V₂V₂' are through vias.
 The path DV₁PQXY is the mainline, while
 RV₂Q, PV₁' and XV₂' are stubs.



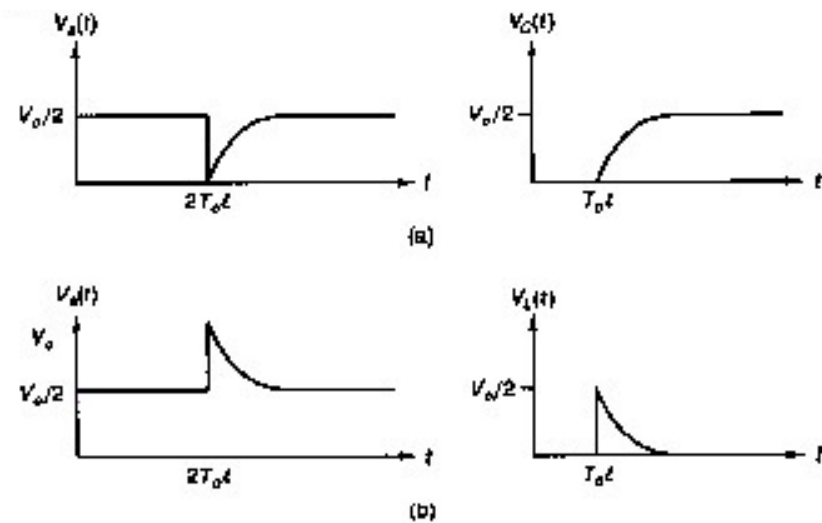
A short stub (a) reflects as a capacitor (b)

4.1.2 Why do we learn transient response ? (Example: II)

- Discontinuity of signal trace (such as stub, via, ..)



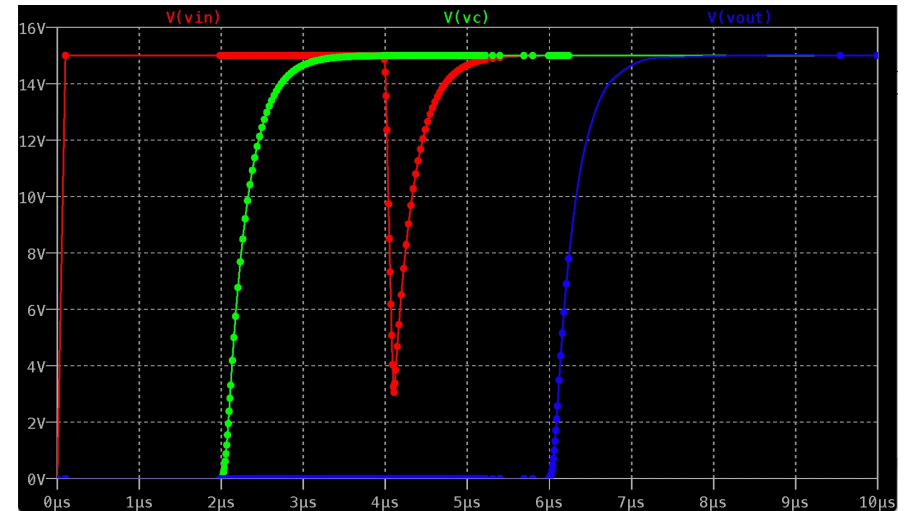
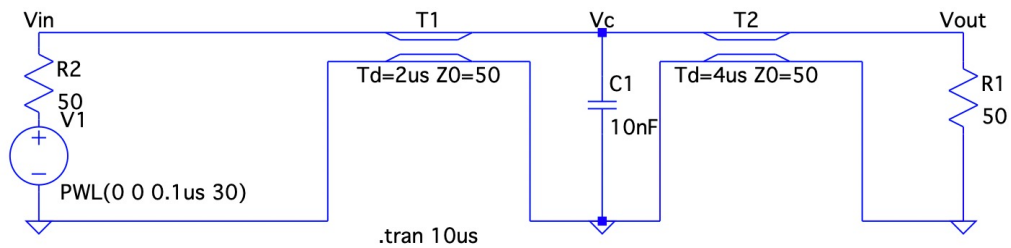
Circuit to show reflection from (a) a capacitive and (b) an inductive load



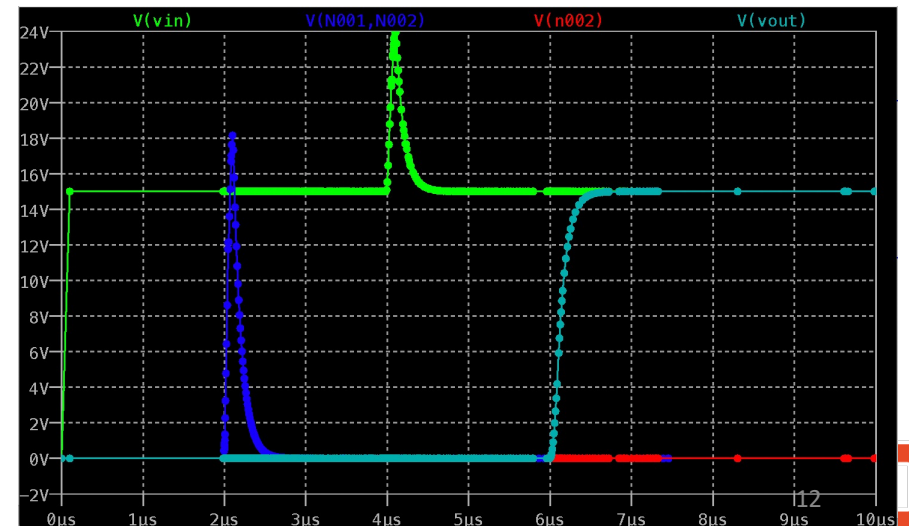
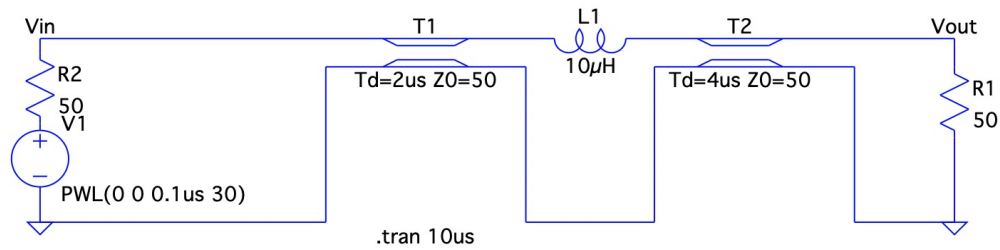
Waveforms at the source and across the lumped load for (a) a capacitor, and (b) an inductor

LTSPICE Transient Simulation

Capacitive_load.asc



Inductive_load.asc



Line terminated by Resistive Loads

Bounce Diagram

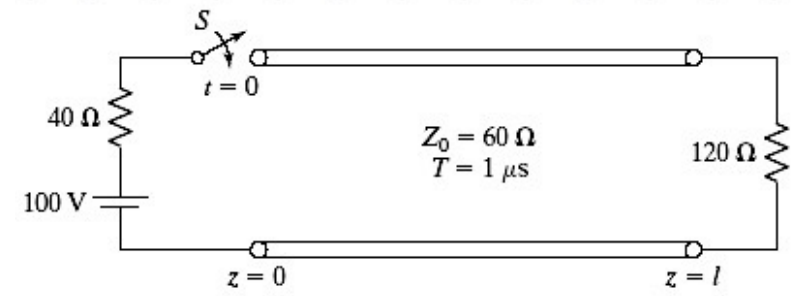
Quantity computation

Voltage carried by the initial (+) wave

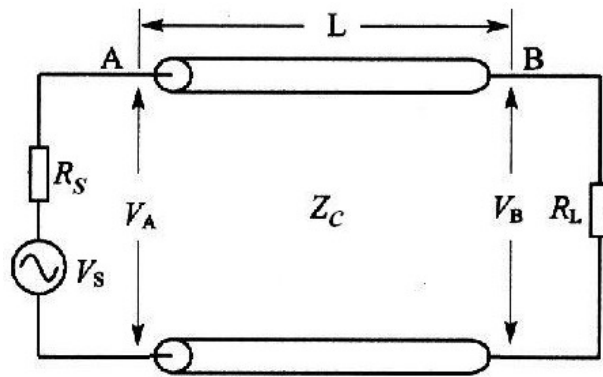
Current carried by the initial (+) wave

Voltage reflection coefficient at load

Voltage reflection coefficient at source



Coefficients



Special case:

$$R_L = 0, \Gamma_L = -1$$

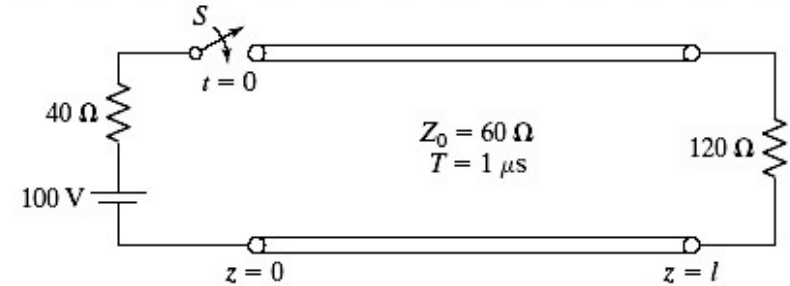
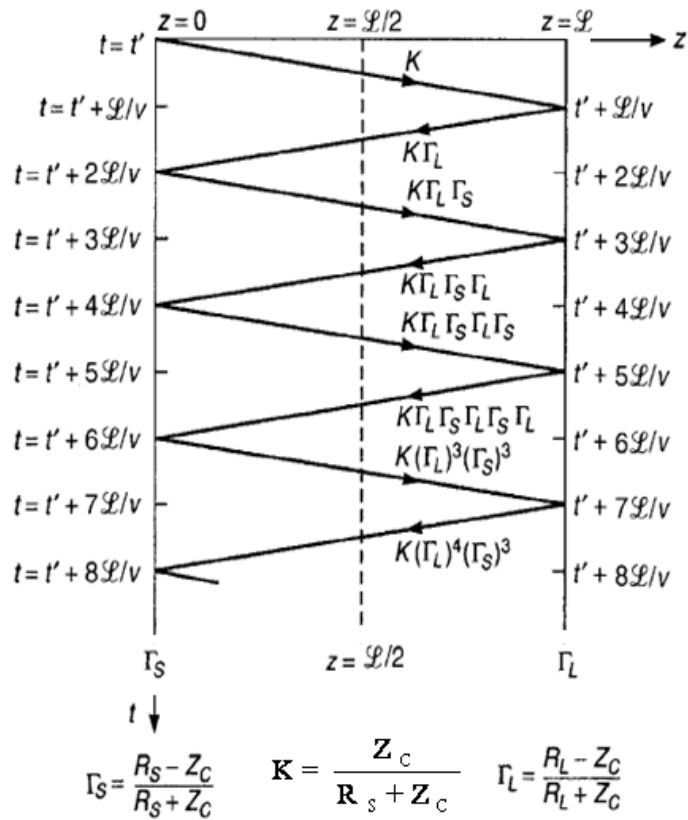
$$R_L = \infty, \Gamma_L = 1$$

$$\text{Injection coefficient: } \tau = \frac{Z_c}{R_s + Z_c}$$

$$\text{Reflection Coefficient of load terminal: } \Gamma_L = \frac{R_L - Z_c}{R_L + Z_c}$$

$$\text{Reflection Coefficient of source terminal: } \Gamma_s = \frac{R_s - Z_c}{R_s + Z_c}$$

Graphical Solutions-Bounce Diagram



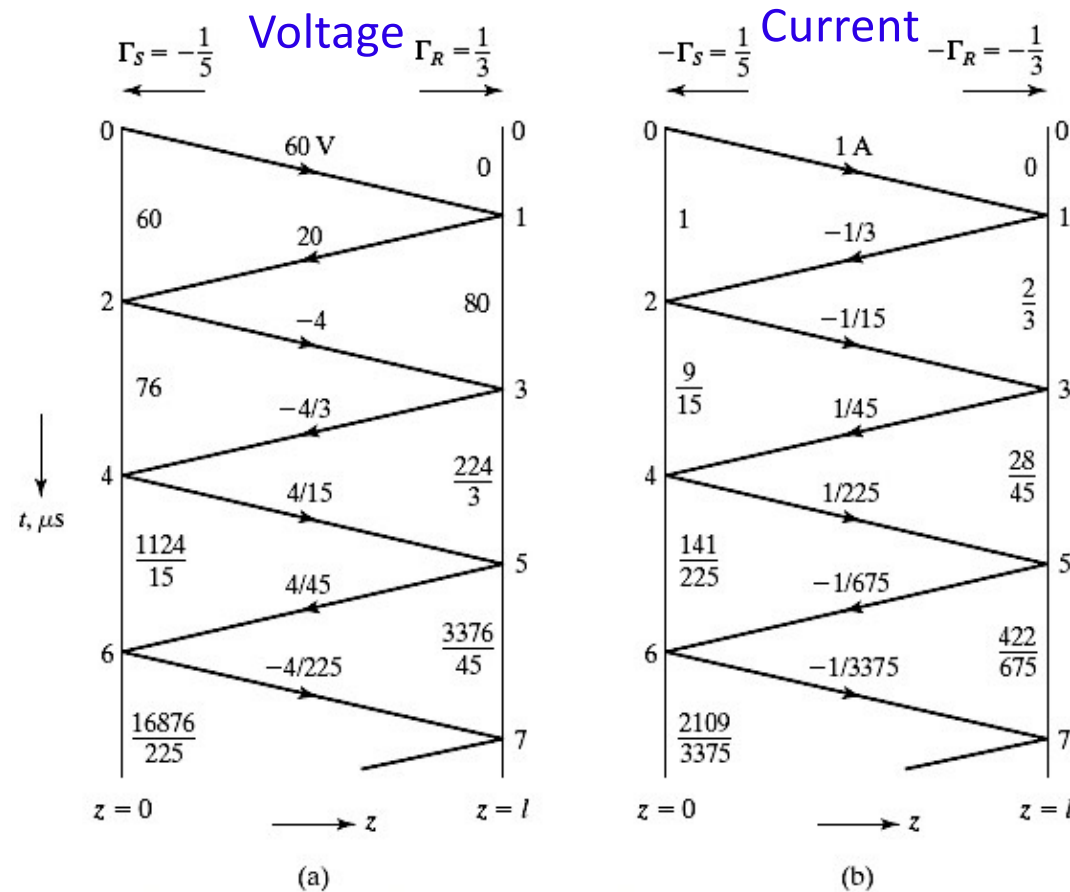
$$\Gamma_S = \frac{40 - 60}{40 + 60} = -\frac{1}{5}$$

$$\Gamma_L = \frac{120 - 60}{120 + 60} = \frac{1}{3}$$

$$\tau = \frac{60}{40 + 60} = \frac{3}{5}$$

Line terminated by Resistive Loads

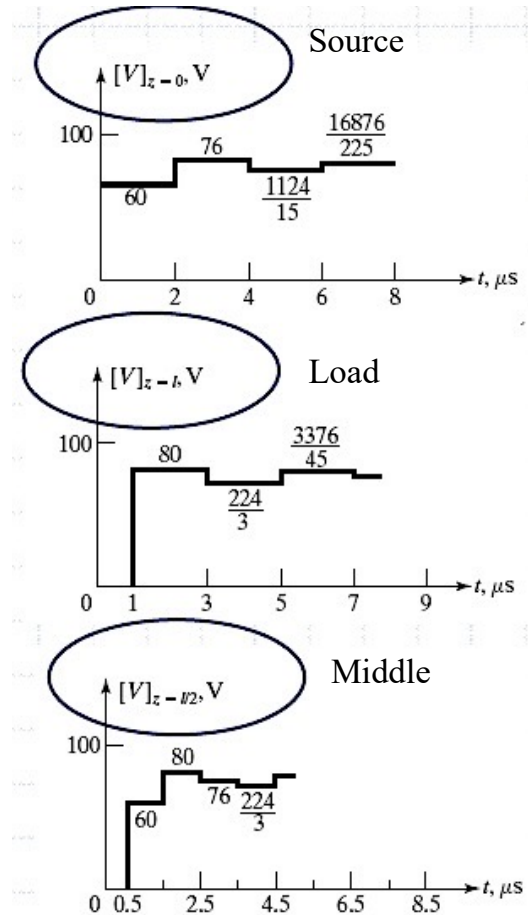
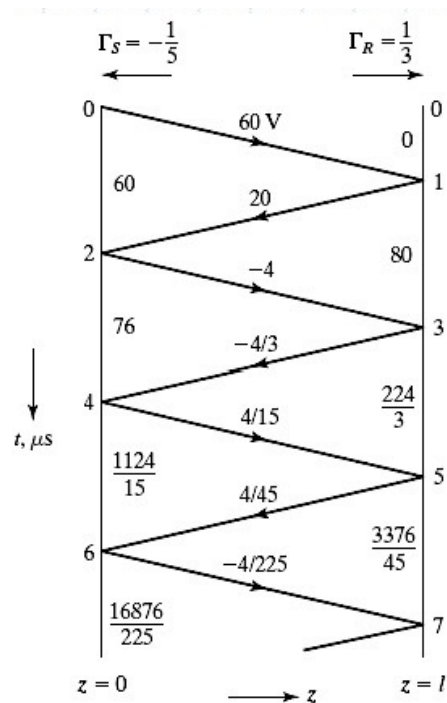
Bounce Diagram



Line terminated by Resistive Loads

Bounce Diagram

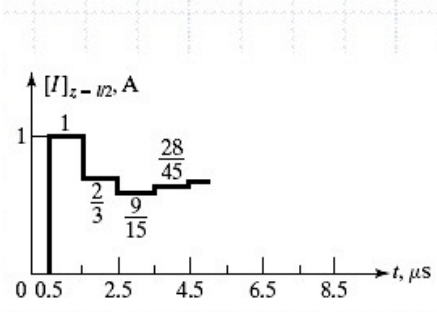
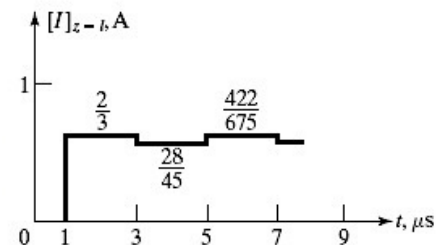
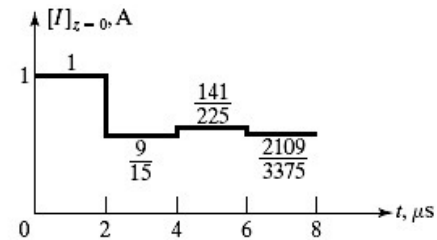
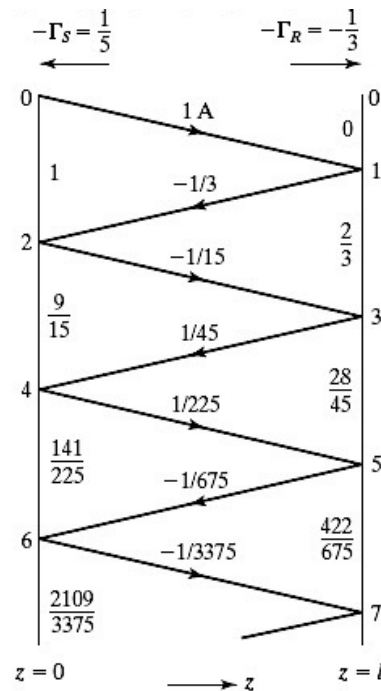
Plots of line voltage versus t (transient)



Line terminated by Resistive Loads

Bounce Diagram

Plots of line current versus t (transient)



The above time-domain are the **transient behavior** of V and I.
What is the **steady state** of this switch circuits for V and I?

Graphical Solutions-Bounce Diagram

Steady state

As time progresses, the line voltage and current tend to converge to certain values, which we can expect to be the steady state values.

In the steady state, the situation consists of a single (+) wave, which is actually a superposition of the infinite number of transient (+) waves, and a single (-) wave, which is actually a superposition of the infinite number of transient (-) waves.

$$V_{ss}^+ = 60 - 4 + \frac{4}{15} - \dots = 60 \left(1 - \frac{1}{15} + \frac{1}{15^2} - \dots \right) = 56.25 \text{ V}$$

$$I_{ss}^+ = 1 - \frac{1}{15} + \frac{1}{225} - \dots = 1 - \frac{1}{15} + \frac{1}{15^2} - \dots = 0.9375 \text{ A}$$

$$V_{ss}^- = 20 - \frac{4}{3} + \frac{4}{45} - \dots = 20 \left(1 - \frac{1}{15} + \frac{1}{15^2} - \dots \right) = 18.75 \text{ V}$$

$$I_{ss}^- = -\frac{1}{3} + \frac{1}{45} - \frac{1}{675} + \dots = -\frac{1}{3} \left(1 - \frac{1}{15} + \frac{1}{15^2} - \dots \right) = -0.3125 \text{ A}$$

The steady-state line voltage and current can now be obtained to be

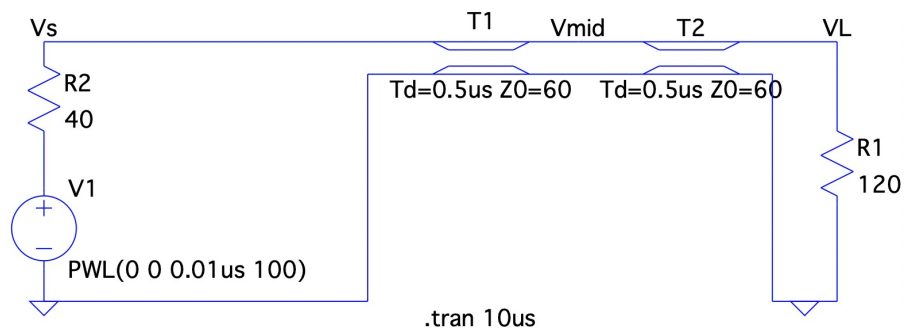
$$V_{ss} = V_{ss}^+ + V_{ss}^- = 75 \text{ V}$$

$$I_{ss} = I_{ss}^+ + I_{ss}^- = 0.625 \text{ A}$$

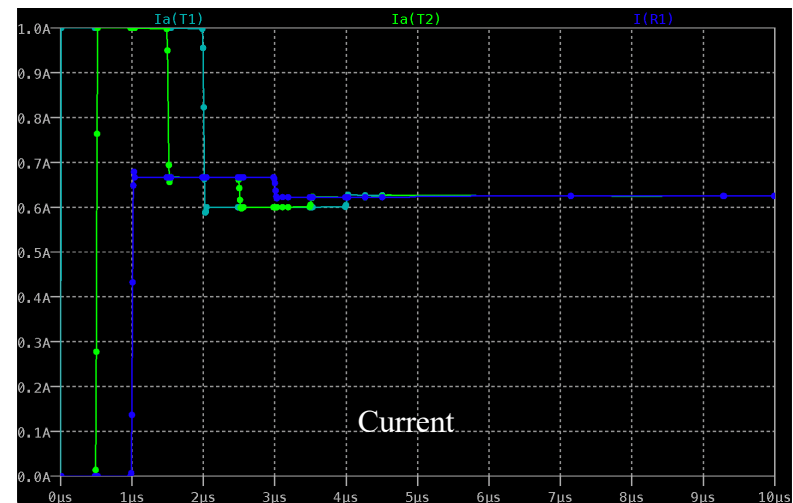
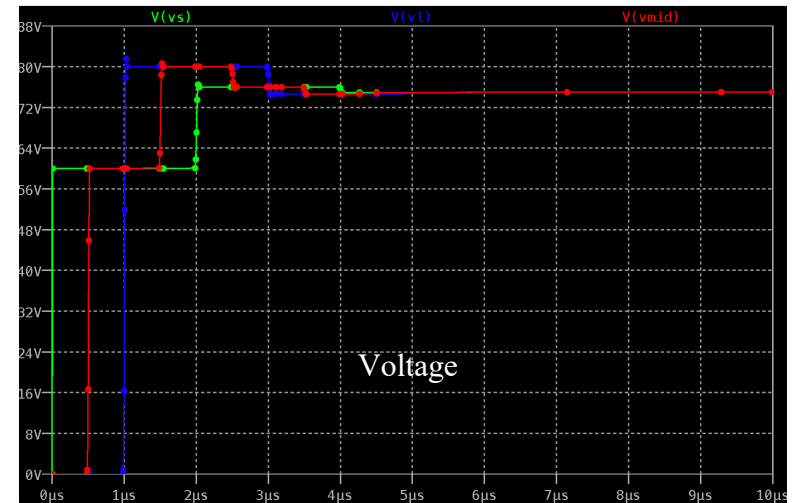
Is there any intuitive concept to explain the results



LTSPICE Simulation



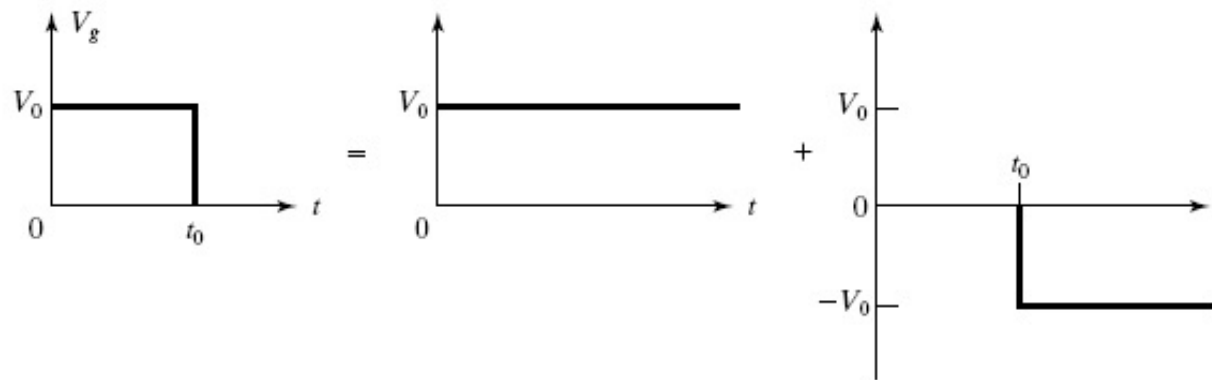
Bounce_Diagram_2lines.asc



Line terminated by Resistive Loads

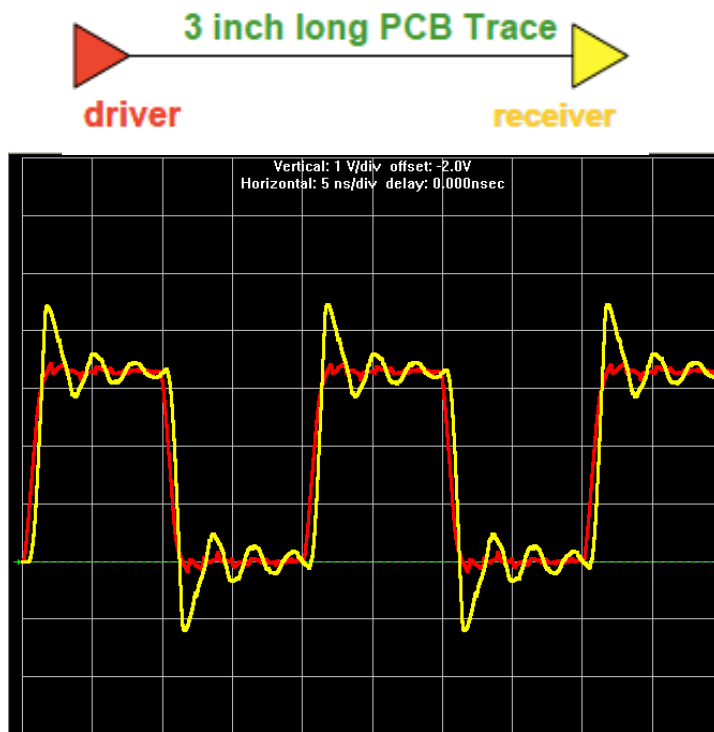
Excitation by Pulse Voltage Source

This can be done by representing the pulse as the superposition of two step functions, and superimposing the bounce diagrams for the two sources one on another

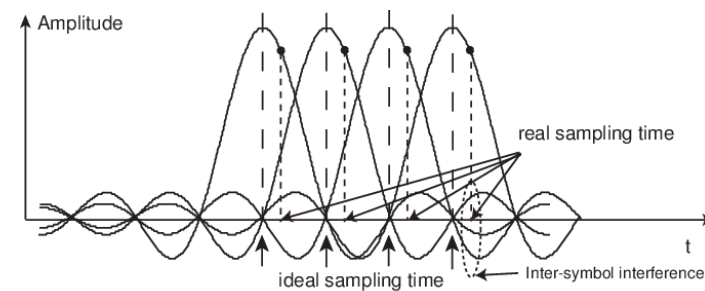


Representation of a rectangular pulse as the superposition of two step functions.

Why Do we Care About Reflections?

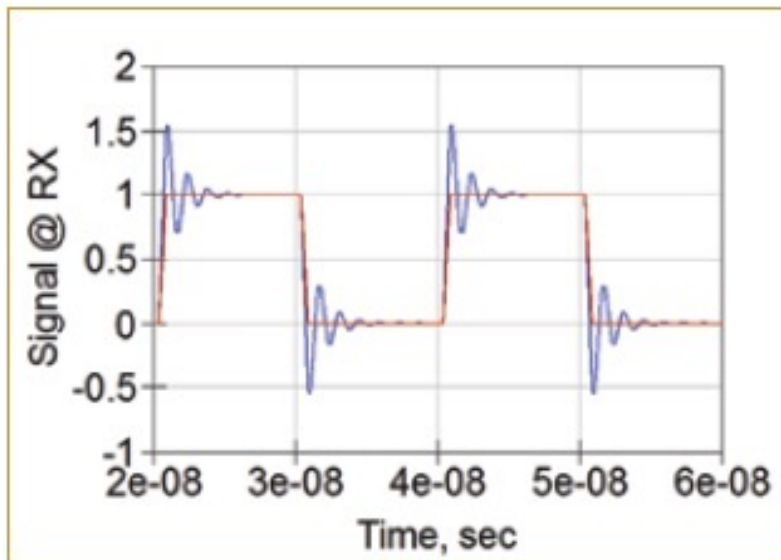


- Reflections can cause signal distortion and collapse of the eye.
- Overshoot: reliability problem
- Undershoot, potential noise margin hit
- If ringing extends into the next bit: intersymbol interference (ISI)
- A good habit: if it is free, always try to improve performance



InterSymbol Interference (ISI)

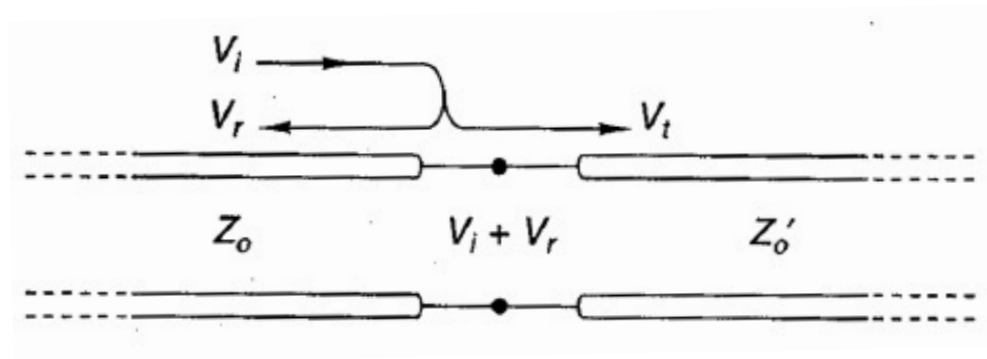
Predicting Reflection Noise



An example of ringing in an unterminated transmission line and with proper transmission

1. Problem: non-uniformity of the transmission lines
✓ Solution: use controlled impedance lines
2. Problem: the ends of the lines
✓ Solution: use a termination strategy
3. Problem: routing topology
✓ Solution: use a linear route, keep branches short
4. Problem: discontinuities
✓ Solution: keep them short, match to line impedance

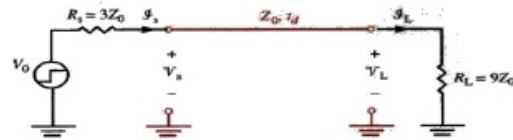
2.1 Reflection at Discontinuity (impedance discontinuity)



Reflection coefficient $\Gamma = \frac{V_r}{V_i} = \frac{Z'_0 - Z_0}{Z'_0 + Z_0}$

$$V_{tot} = V_i + V_r = V^+ + V^- = (1 + \Gamma)V^+$$

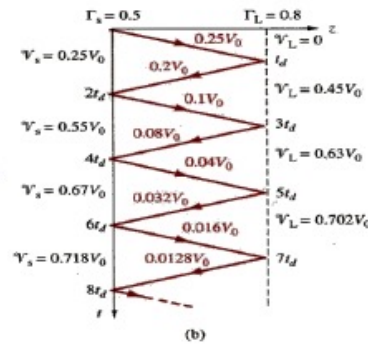
Reflection at Discontinuity (resistive discontinuity)



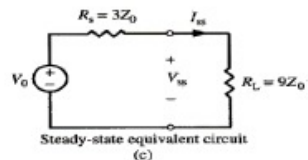
(a)

Bounce diagram

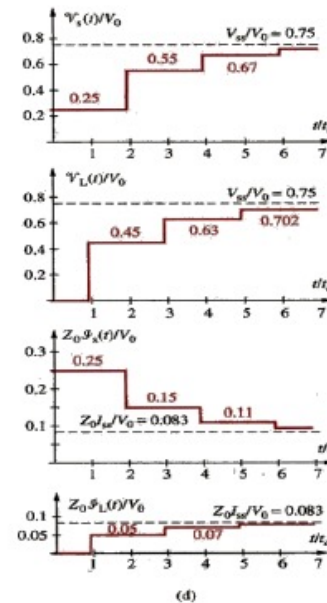
(covered in the previous lecture)



(b)



(c)



(d)

Voltage Transient response at the source end

Voltage Transient response at the load end

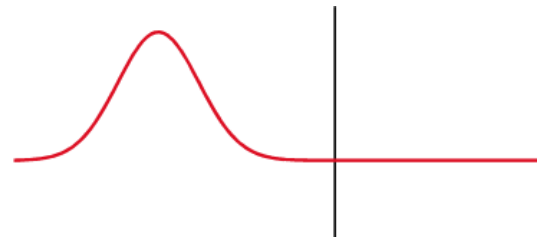
Current Transient response at the source end

Current Transient response at the load end

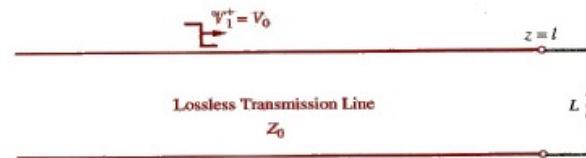
Step excitation of a resistively terminated lossless line. (a) the circuit configuration. (b) Bounce diagram. (c) steady state equivalent circuit seen by the source. (d) Normalized source- and load-end voltage and source- and load-end current as a function of t/t_d .

2.2 Reflection at Discontinuity (reactive discontinuity)

- Concept

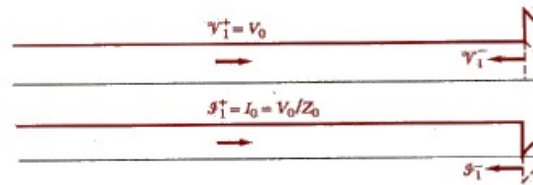


Signal (or energy) transmitted and reflected from a discontinuity



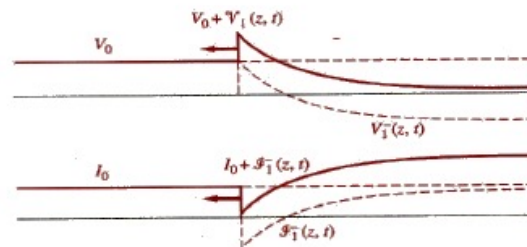
(a)

- Transient step response of an inductor



(b)

Reflection coefficient depends on frequency



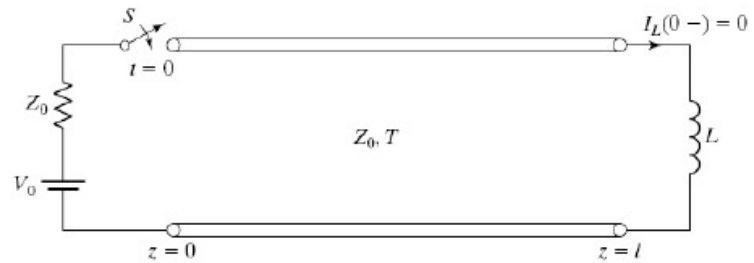
(c)

When steady state (DC), inductance acts like a short.

Reflection from a purely inductive load.

2.2.1 Inductive termination

A line of length l is terminated by an inductor L with zero initial current and a constant-voltage source with internal resistance equal to the characteristic impedance of the line is connected to the line at $t = 0$.



2.2.1 Inductive termination

A line of length l is terminated by an inductor L with zero initial current and a constant-voltage source with internal resistance equal to the characteristic impedance of the line is connected to the line at $t = 0$.

The boundary condition at $z = l$

$$\frac{V_0}{2} + V^- = L \frac{d}{dt} \left(\frac{V_0}{2Z_0} - \frac{V^-}{Z_0} \right)$$

$$\Rightarrow \frac{L}{Z_0} \frac{dV^-}{dt} + V^- = -\frac{V_0}{2} \quad \Rightarrow V^-(t) = -\frac{V_0}{2} + Ae^{-(\frac{Z_0}{L})t}$$

Initial condition

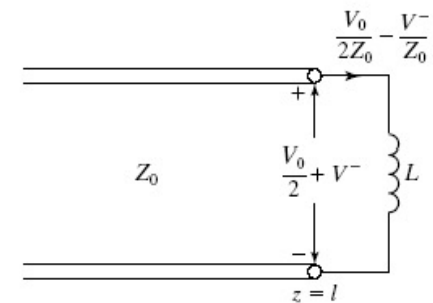
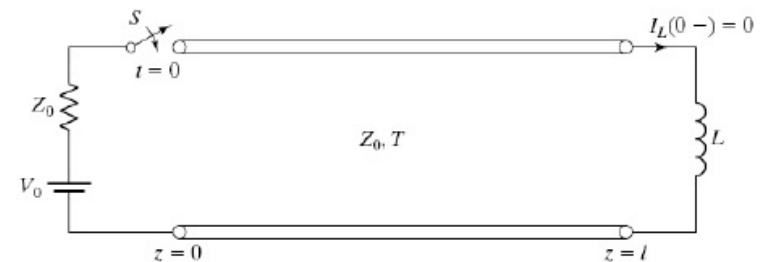
$$\left[\frac{V_0}{2Z_0} - \frac{V^-}{Z_0} \right]_{t=T} = 0$$

$$[V^-]_{t=T} = \frac{V_0}{2}$$

Solution:

$$A = V_0 e^{(Z_0/L)T}$$

$$V^-(l, t) = -\frac{V_0}{2} + V_0 e^{-(Z_0/L)(t-T)} \quad \text{for } t > T$$



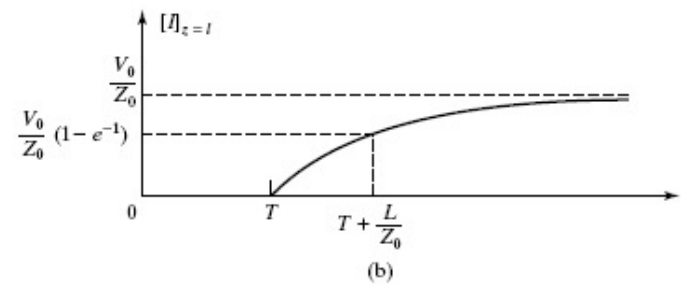
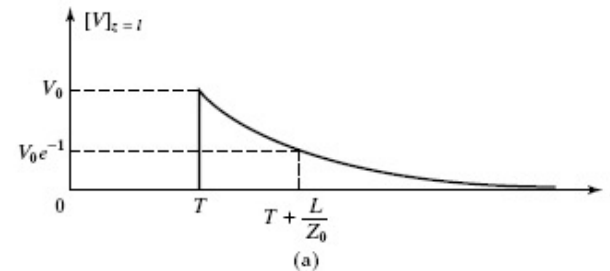
2.2.1 Inductive termination

$$V(l,t) = \frac{V_0}{2} + V^-(l,t)$$

$$= \begin{cases} 0 & \text{for } t < T \\ V_0 e^{-(Z_0/L)(t-T)} & \text{for } t > T \end{cases}$$

$$I(l,t) = \frac{V_0}{2Z_0} + I^-(l,t)$$

$$= \begin{cases} 0 & \text{for } t < T \\ (V_0 / Z_0) [1 - e^{-(Z_0/L)(t-T)}] & \text{for } t > T \end{cases}$$



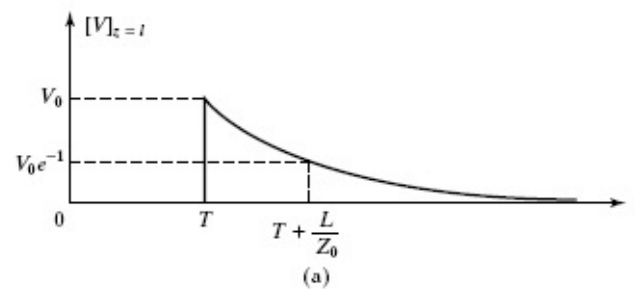
Remember we also predicted the waveform behavior by an intuitive physical concept last class.

2.2.1 Inductive termination

The inductor is looked as

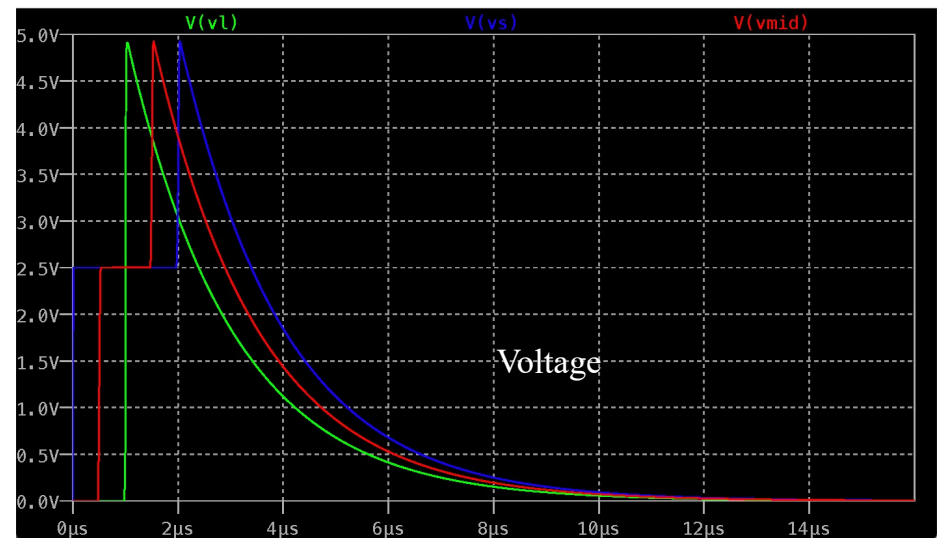
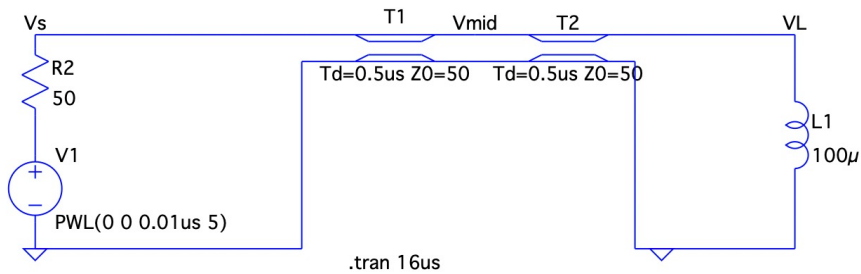
1. Short circuit at steady state $t = \infty$.
2. Open circuit at initial transient for $t = T$.

Between $t = T$ and $t = \infty$, the behavior follows the time constant L/Z_0 .



LTSPICE Simulation

Bounce_Diagram_Inductor_load.asc



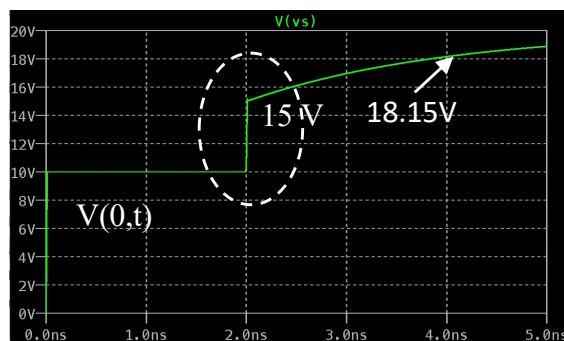
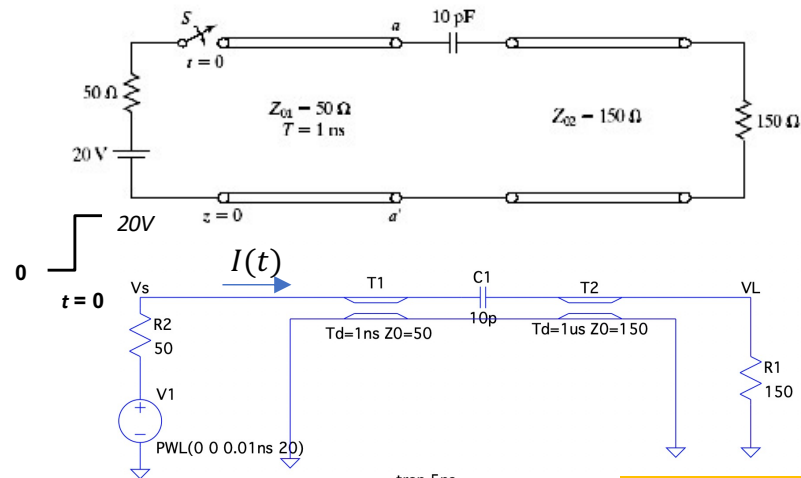
2.2.2 Capacitive discontinuity

Can you explain the waveform behavior?

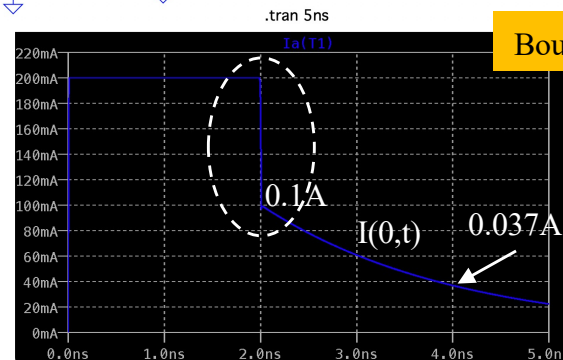
Why 15V at $t = 2\text{ns}$?

What is the steady state voltage?

What is the time constant?



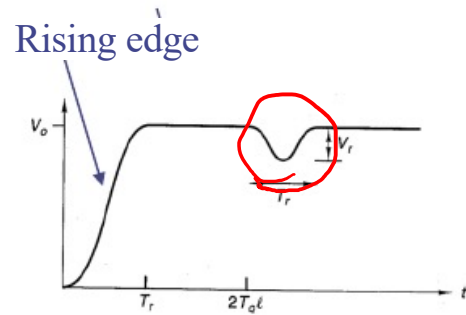
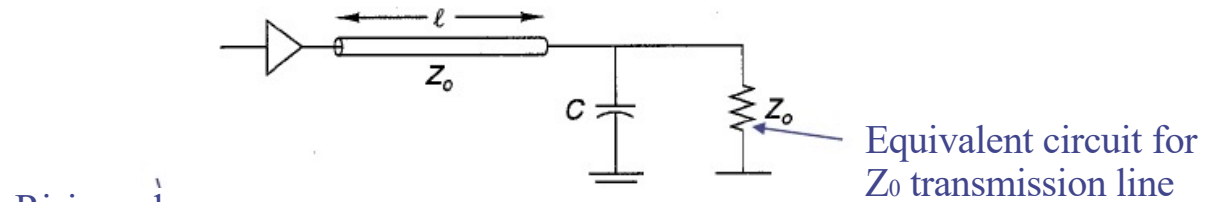
Voltage at source



Current at source

Bounce_Diagram_capacitor_load.asc

2.2.2 Capacitive discontinuity



Reflection waveform
by a small shunt capacitance

The maximum reflected noise
by the capacitance

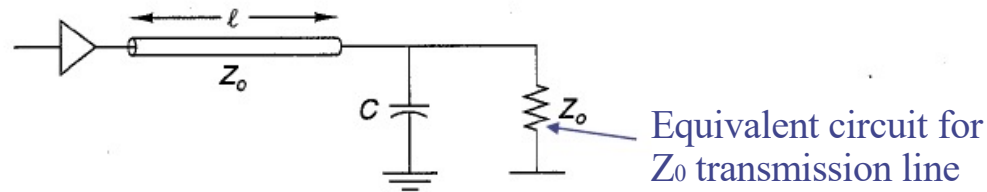
$$V_r = -\frac{CZ_0}{2T_r}V_0$$

T_r : Rise time of the input step signal



2.2.2 Capacitive discontinuity

•Theory



$$\Gamma = \frac{V_r}{V_0} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

$$Z_L = \left(\frac{1}{j\omega C} \parallel Z_0 \right) = \frac{Z_0}{1 + j\omega C Z_0}$$

Reflected voltage $V_r = -\frac{j\omega C Z_0}{2 + j\omega C Z_0} V_0$

Assume $|j\omega C Z_0| \leq 2$

$$V_r \approx -\frac{C Z_0}{2} j\omega V_0$$

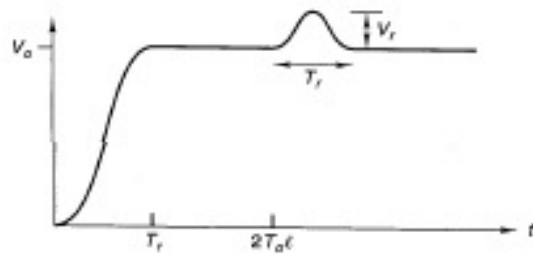
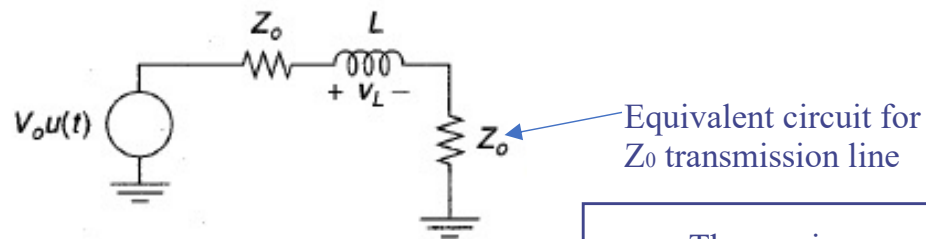
In time domain,

$$v_r(t) \approx -\frac{C Z_0}{2} \left(\frac{dv_0(t)}{dt} \right)$$

so, The maximum noise $V_r = -\frac{C Z_0}{2 T_r} V_0$

at the rising edge

Similar Approximation for Inductive discontinuity



Reflection waveform
by a small series inductance

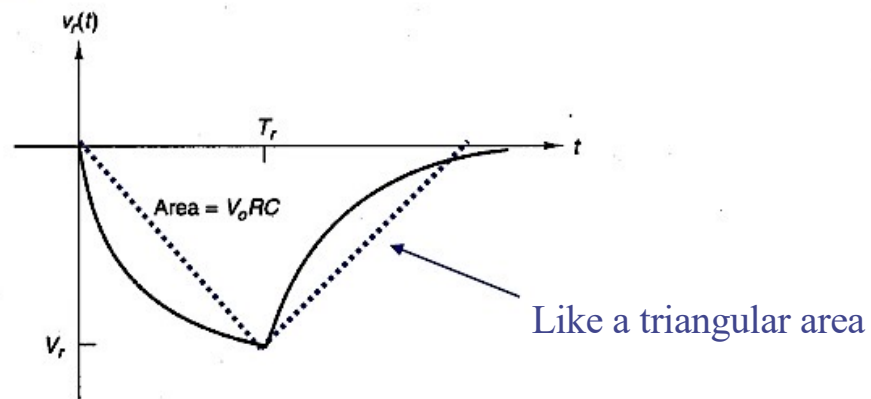
The maximum reflected noise
by the inductance

$$V_r = \frac{L}{2Z_0 T_r} V_0$$

T_r : Rise time of the input step signal

2.2.2 Capacitive discontinuity

•Theory

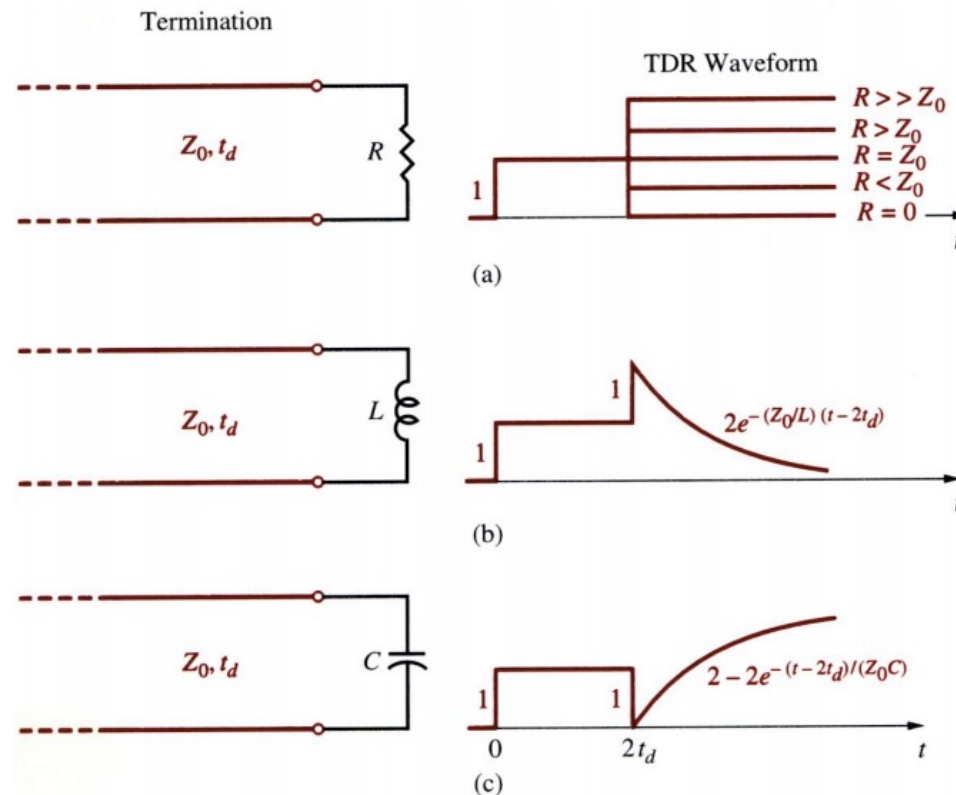


It can be proved that the total area under the curve is

$$area = \frac{CZ_0}{2T_r} V_0 \times 2T_r \times \frac{1}{2} = C \frac{Z_0}{2} V_0$$

It is independent on the rise time !!

2.3 All kinds of discontinuities



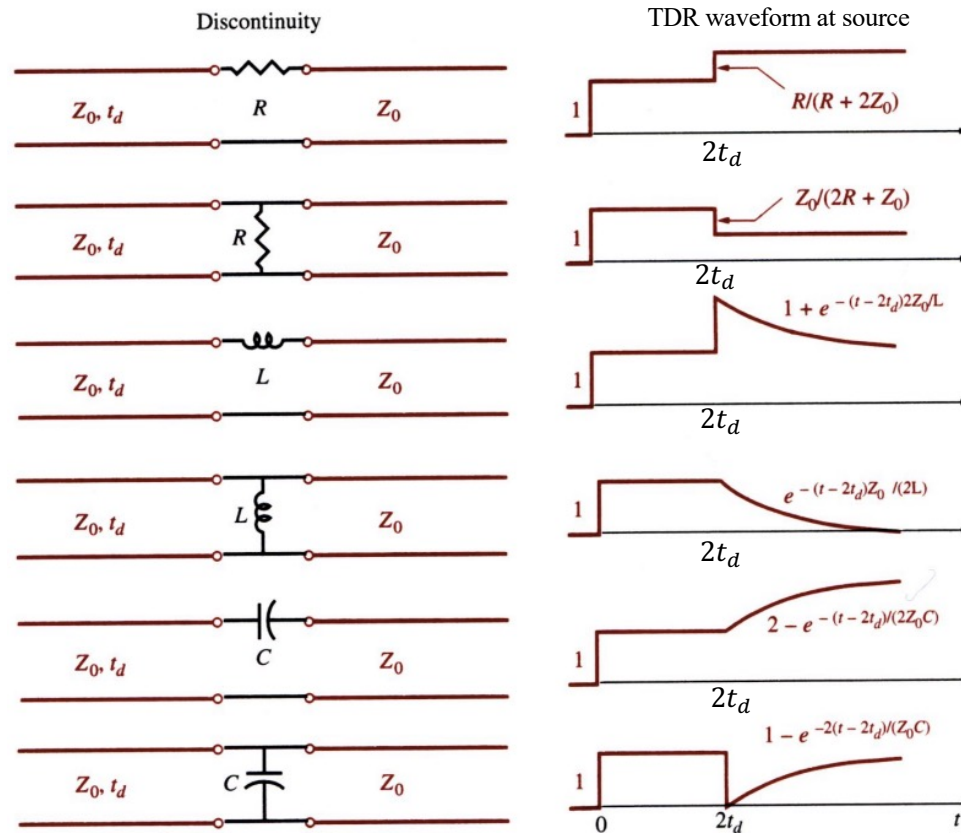
Termination
(At the load side)

TDR signatures produced by simple discontinuities

Source end voltage signatures for purely resistive, inductive and capacitive discontinuities.

$V_0 = 2V$ and $R_S = Z_0$

TDR signatures produced by simple discontinuities



Between two lines

L: Open at first, then short at steady state

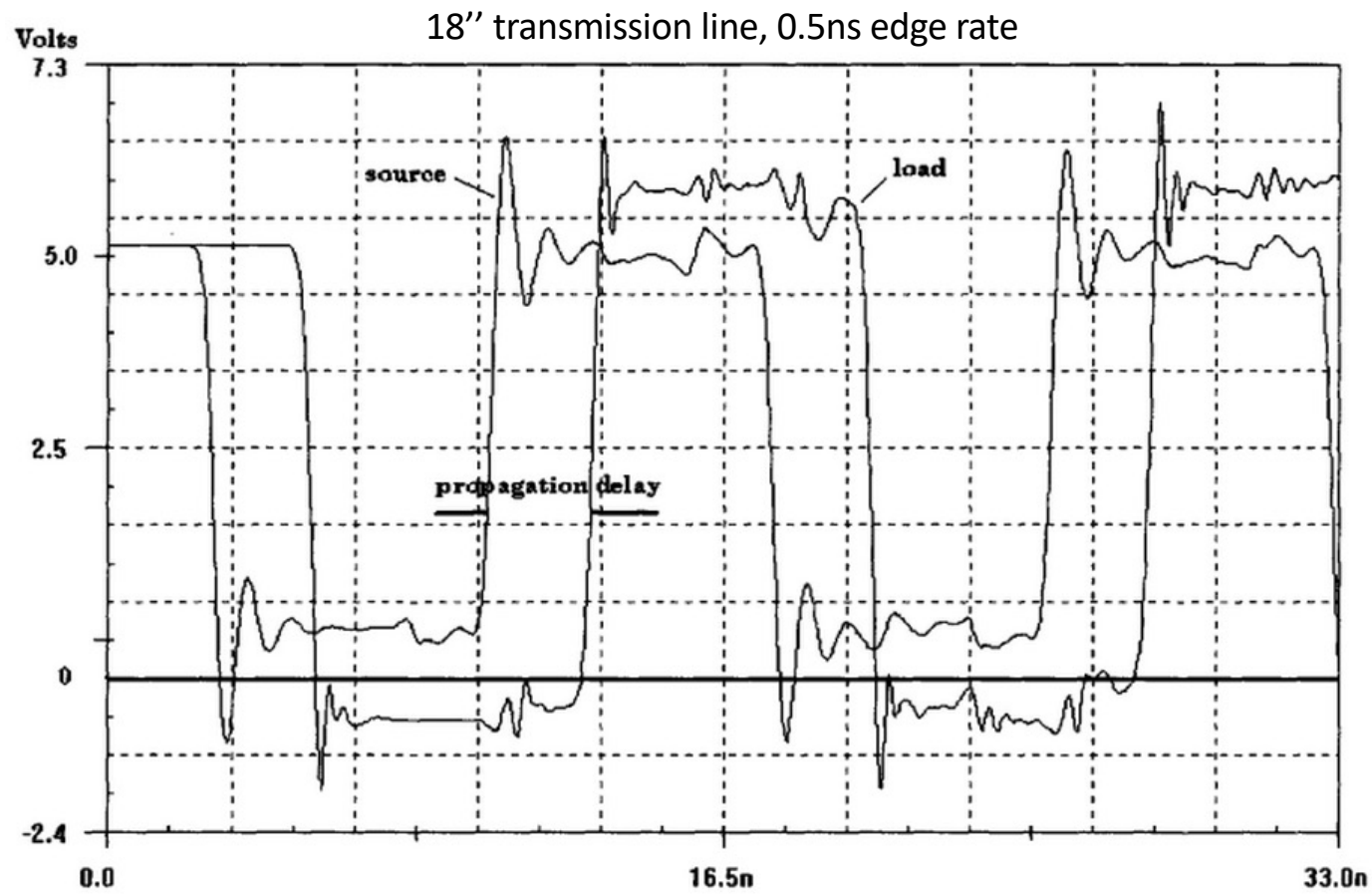
C: Short at first, then open at steady state

Source end voltage signatures (TDR reading) for shunt or series purely resistive, inductive and capacitive discontinuities.
 $V_0 = 2V$ and $R_S = Z_0$

3 Why termination signals?

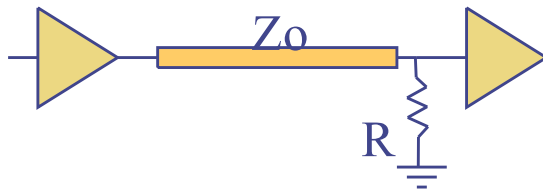
- Proper termination technique reduces reflections which mitigates overshoot, undershoot, ringing problems
- Two common termination topologies:
 - Source termination
 - End termination
- Four common termination schemes:
 - Parallel termination
 - Thevenin termination
 - Series termination
 - AC termination

Termination? no termination? That's a question.

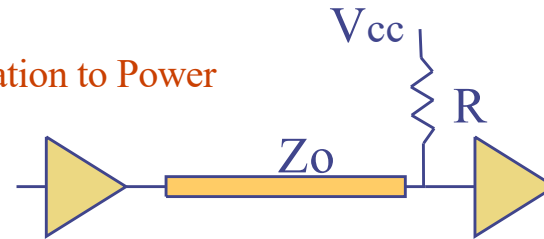


Termination – Parallel termination

Termination to Ground

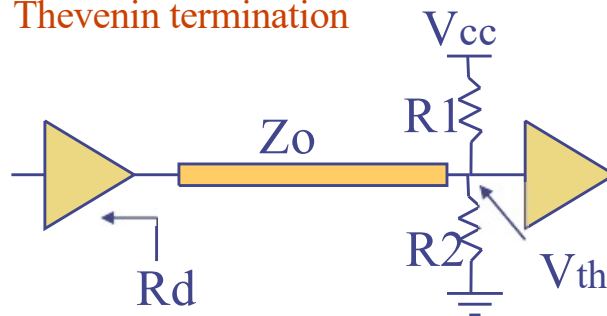


Termination to Power

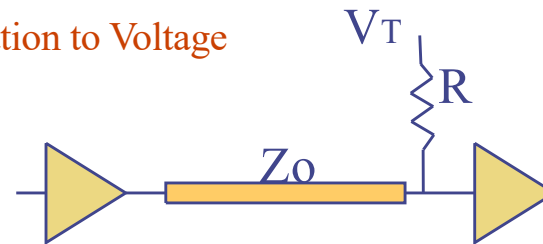


Termination at load

Thevenin termination



Termination to Voltage



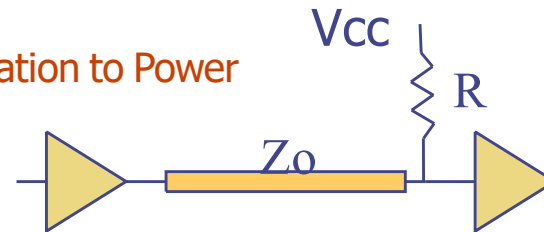
Termination – Parallel termination

Termination to Ground



Design Equation: $R=Z_0$

Termination to Power



Design Equation: $R=Z_0$

Power dissipation

$$P = \frac{1}{2} \left(\frac{\Delta V_{lo}^2}{R} + \frac{\Delta V_{hi}^2}{R} \right)$$

Assume Duty cycle is 50%

Ex: Suppose $V_0=3.3V$, $R=50\Omega$

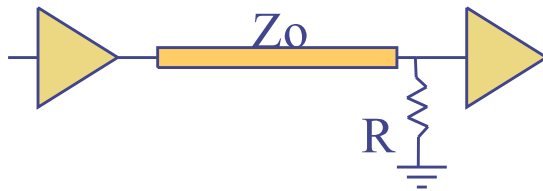
Power consumed by far end termination to ground (50% duty cycle)

$$P = \frac{1}{2} \left(\frac{0}{50} + \frac{3.3^2}{50} \right) = 100mW$$

Much less power if $\ll$ 50% duty cycle and ground termination, or $\gg$ 50% duty cycle and Vcc termination

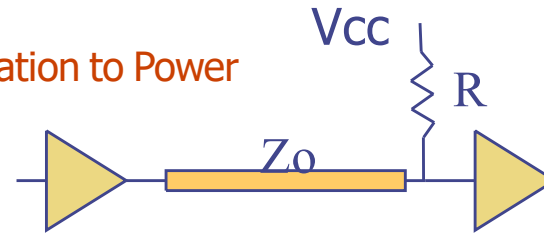
Termination – Parallel termination

Termination to Ground



Design Equation: $R=Z_0$

Termination to Power



Design Equation: $R=Z_0$

Advantages:

- Simplest
- The full driver voltage is delivered to the receiver

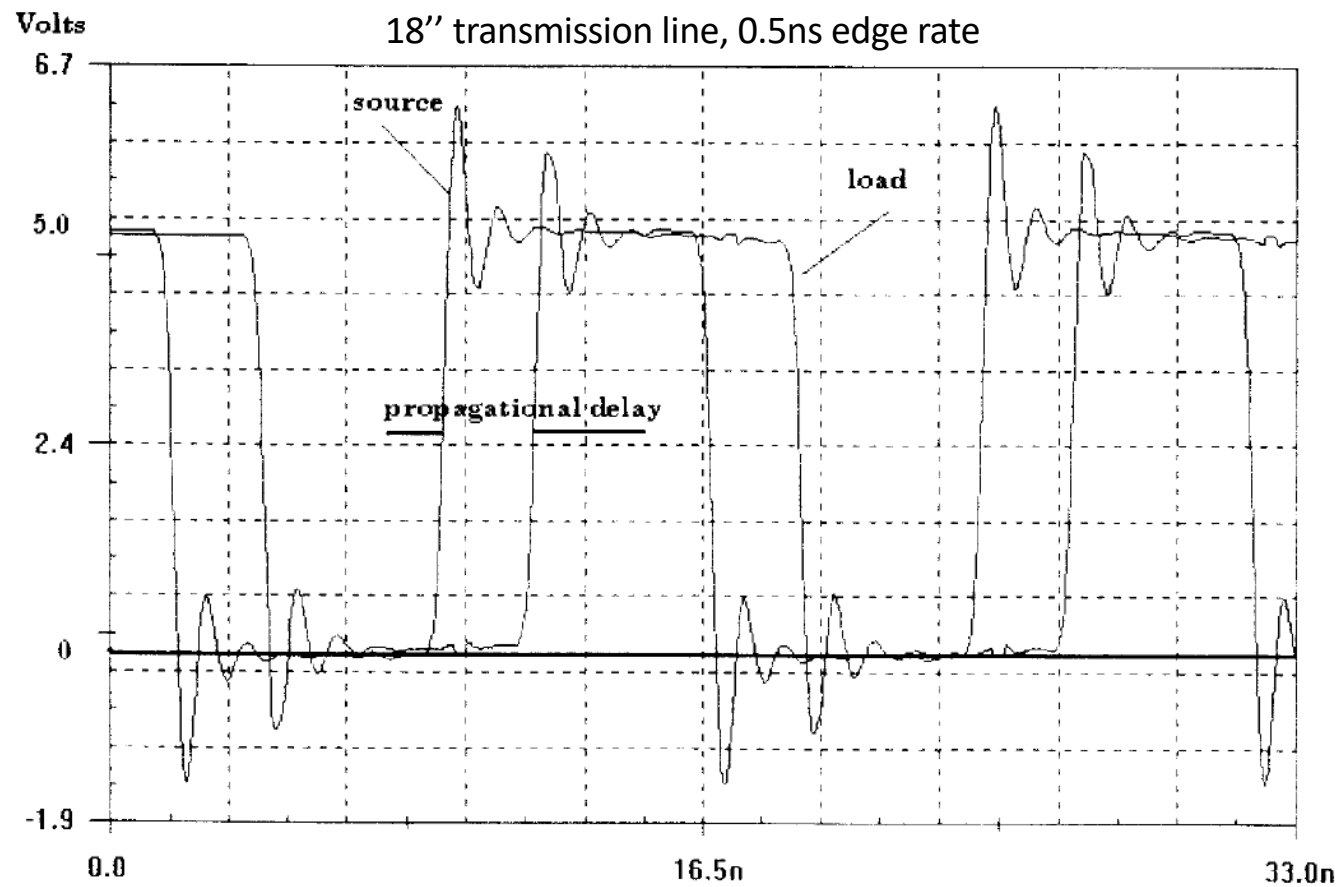
Disadvantage

- Power consumption
- Cost R elements and PCB space

Which one is better if you have to choose one ?

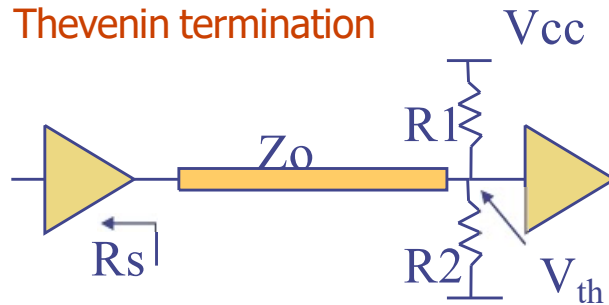
A common approach is to terminate to Ground since we have more access to grounds in our system.

Termination – Parallel termination w. R to Ground



Termination – Parallel termination

Thevenin termination



provide a termination impedance to an arbitrary voltage

Design Equations:

$$Z_{th} = R_1 // R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

Termination impedance



$$V_{th} = V_{cc} \left(\frac{R_2}{R_1 + R_2} \right)$$

Termination voltage

$$\Rightarrow R_1 = \frac{V_{cc} \times Z_{th}}{V_{th}} \quad R_2 = \frac{R_1 \times V_{th}}{V_{cc} - V_{th}}$$

Termination – Parallel termination

Thevenin termination

Example: We have a $50\ \Omega$ transmission line that needs to be load terminated. We have a system with a 3.3V power supply. We want to use a Thevenin equivalent network to form a termination impedance of $50\ \Omega$ to 2V. What are the values of R_1 and R_2 ?

$$Z_{th} = R_1 // R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2} = 50\ \Omega$$

$$V_{th} = V_{DD} \left(\frac{R_2}{R_1 + R_2} \right) = 2\text{V}$$

A: $R_1 = \sim 80\ \Omega$ and $R_2 = \sim 135\ \Omega$

Termination – Parallel termination

Thevenin termination

Advantages:

- Balanced
- No additional voltage generation circuit

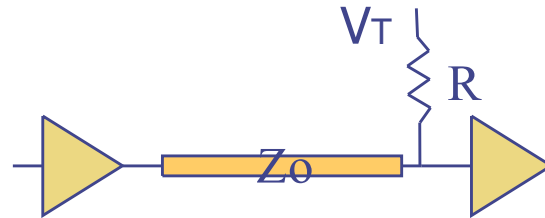
Disadvantage

- Static Power consumption
- Require an additional R elements and PCB space compared to termination to ground approach
- Resistors only come in pre-defined values

Often used to terminate signals driven to memory devices, such as double data rate (DDR) memories.

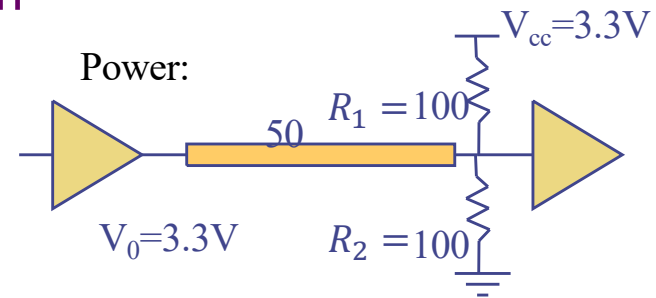
Termination – Parallel termination

Termination to Voltage



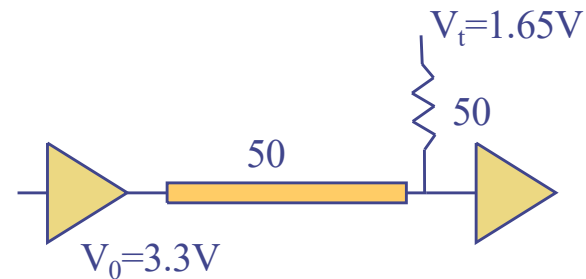
Design Equation: $R=Z_0$

- ◆ Advantages:
 - Less static power consumption
- ◆ Disadvantage
 - Static Power consumption
 - Cost R elements and PCB space



Thevenin Termination

$$P = \frac{1}{2} \left(\frac{\Delta V_{lo}^2}{R_1} + \frac{\Delta V_{hi}^2}{R_2} \right) = \frac{1}{2} \left(\frac{3.3^2}{100} + \frac{3.3^2}{100} \right) = 100mW$$

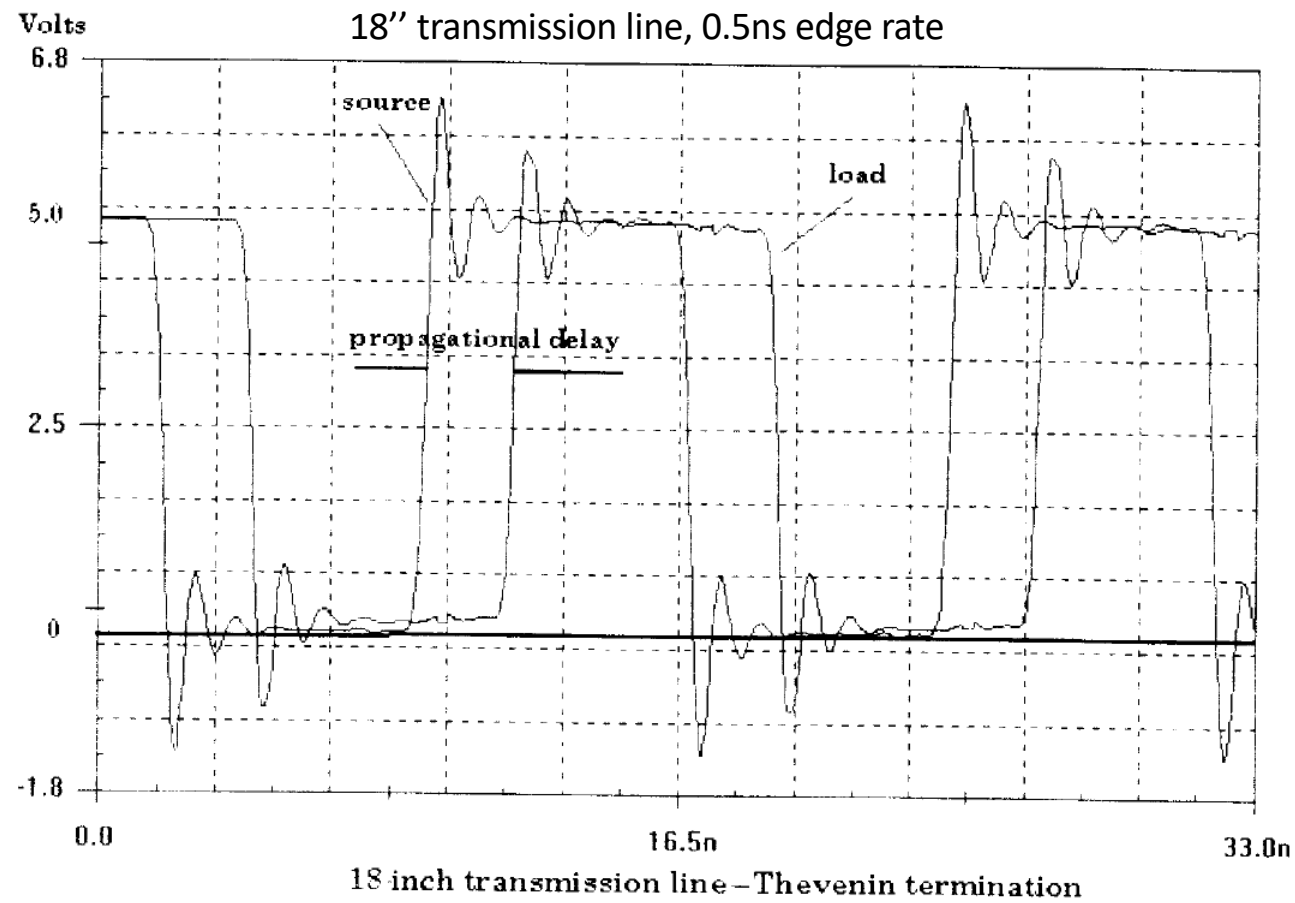


Termination to Voltage

$$P = \frac{1}{2} \left(\frac{(V_R/2)^2}{R_1} + \frac{(V_R/2)^2}{R_1} \right) = \frac{1}{2} \left(\frac{1.65^2}{50} + \frac{1.65^2}{50} \right) = 50mW$$

Vt termination consumes half the power as Thevenin far end!

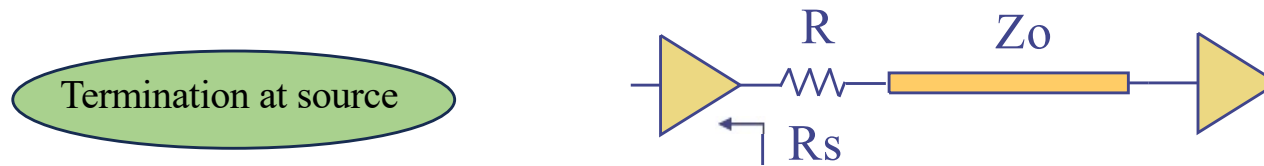
Termination – Thervenin termination



Termination – Parallel termination Summary

- Advantages:
 - Simple
 - If the receiver is capacitive (which it is), the termination resistor will increase the effective time constant of the load.
 - The full driver voltage is delivered to the receiver (assume $R_s=0$)
- Disadvantages:
 - When the transients have ended, the driver now has a DC load that it is driving. This increases DC power consumption.
 - When the source has output impedance (R_s), after the transients have ended, there will be a resistive divider between R_s and R_L . This means that the full voltage of the driver will not be seen at the receiver.

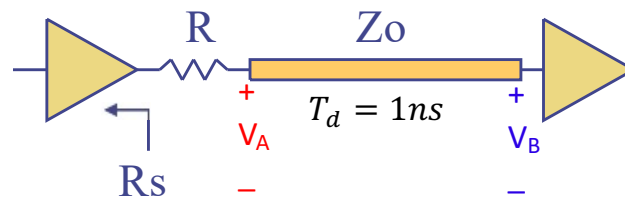
Termination – Series termination



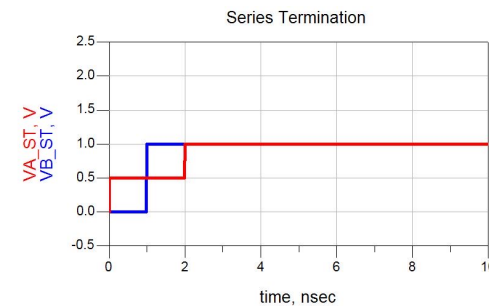
Design Equation: $R = Z_0 - R_s$

1. 50% reduction in drive voltage from the output of the resistor before traveling from source to load
2. The half wave travels down the TL and arrives at the load end T_d delay time later.
3. The forward waves sees an open load, so reflection coefficient is 1.
4. The reflected signal from the load with propagate back to the source at a 50% voltage level
5. After T_d delay time, the backward wave has 50% magnitude. The 50% reflected signal, plus the incoming 50% source signal, will add together and provide the full voltage level signal at the load.
6. No more reflection at the source side

Termination – series termination



Design Equation: $R = Z_o - R_s$



Advantages:

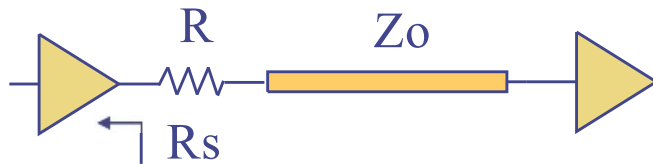
- Simple
- Consume less power

Disadvantage

- The R_s is different for Pull-up and Pull-down
- Rise time degrades due to the increased RC time constant.

☒ 3.3V ☐ 5.0V				
V_{OH}	2.4	V	Z_H	112.499
I_{OH}	8	mA		
V_{OL}	0.5	V	Z_L	20.8333
I_{OL}	24	mA		

Termination – Series termination



$$R = Z_o - R_s$$

Termination at source

Effects of edge rate degradation

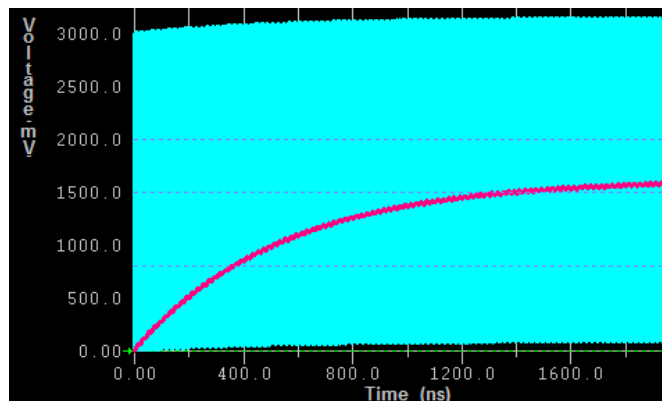
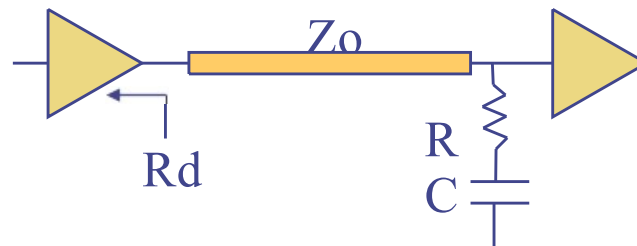
At any point along the TL, looking back towards the source, there's a drive impedance Z_d . With a capacitive load, we have a simple RC low-pass filter with a time constant of

$$\tau = RC = Z_d C$$

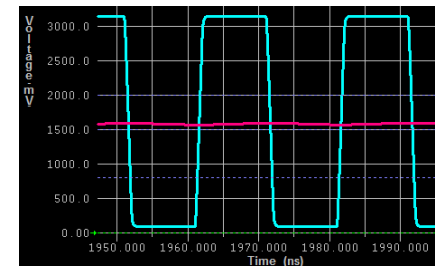
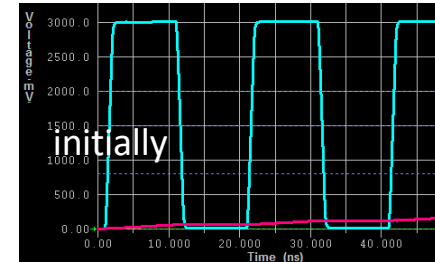
the rise time degradation is

$$t_{r(10-90)} = 2.2 Z_d C$$

Termination – AC termination



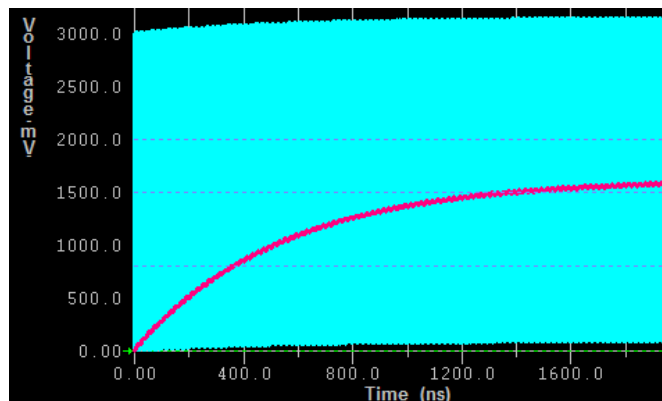
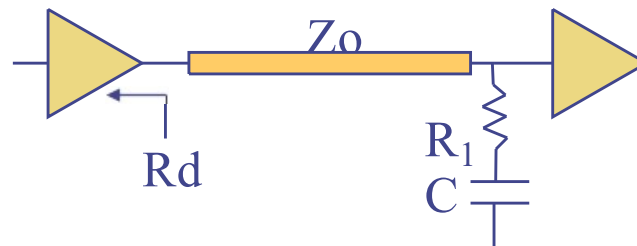
Voltage across capacitor “charges up”



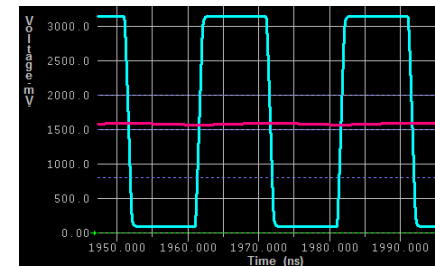
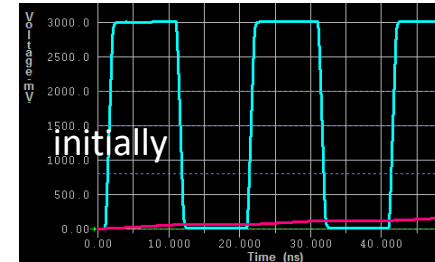
A few time constants later
 $50\ \Omega$ 10 nF $\sim$ 1000 nsec

Capacitor blocks low-frequency signals
 while passing high-frequency signals

Termination – AC termination



Voltage across capacitor “charges up”



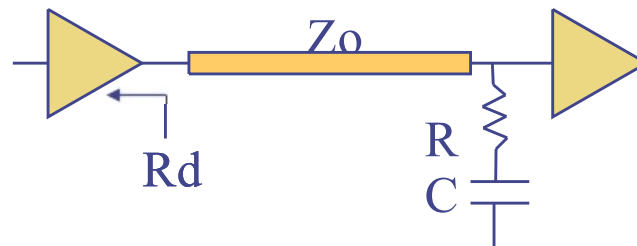
A few time constants later
 50Ω 10 nF $\sim$ 1000 nsec

$$P = \frac{1}{2} \left(\frac{\Delta V_{lo}^2}{R} + \frac{\Delta V_{hi}^2}{R} \right)$$

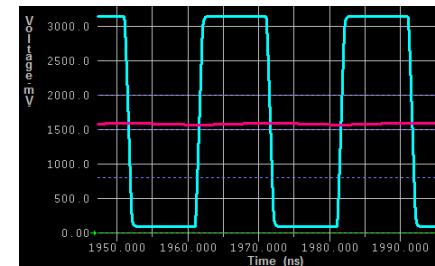
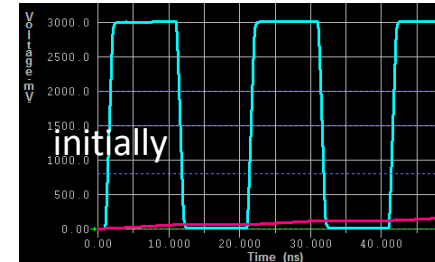
Power consumed in AC termination is
 1/2 as much as far-end single-resistor

$$P = \frac{1}{2} \left(\frac{(V_R/2)^2}{R_1} + \frac{(V_R/2)^2}{R_1} \right) = \frac{1}{2} \left(\frac{1.65^2}{50} + \frac{1.65^2}{50} \right) = 50mW$$

Termination – AC termination



- ◆ Advantage:
 - Power saving
- ◆ Disadvantage:
 - C is not easy to design
 - May slow down high-speed signals
- ◆ Application
 - Battery-driven systems
 - Backplanes, cables, distributed loads, and clocks drivers



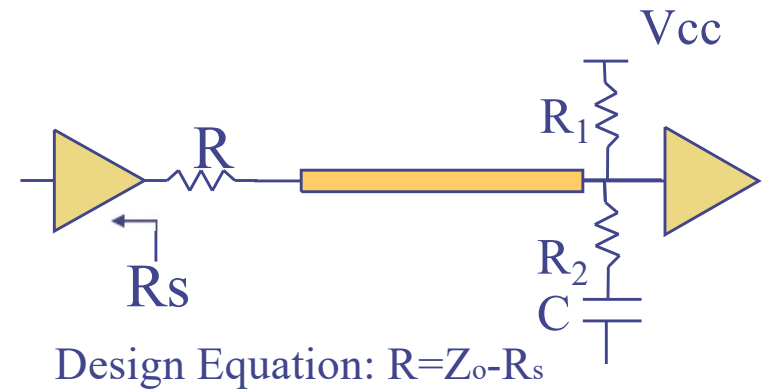
A few time constants later
 $50\ \Omega\ 10\ \text{nF} \sim 1000\ \text{nsec}$

$$P = \frac{1}{2} \left(\frac{\Delta V_{lo}^2}{R} + \frac{\Delta V_{hi}^2}{R} \right)$$

Power consumed in AC termination is
 1/2 as much as far-end single-resistor

$$P = \frac{1}{2} \left(\frac{(V_R/2)^2}{R_1} + \frac{(V_R/2)^2}{R_1} \right) = \frac{1}{2} \left(\frac{1.65^2}{50} + \frac{1.65^2}{50} \right) = 50\text{mW}$$

Termination – Dual termination



Advantages:

- 1) Both forward and reverse traveling waves are terminated

Disadvantages:

- 1) The voltage level that is delivered to the load is $\frac{1}{2}$ of what the driver outputs.
- 2) Requires two termination resistors.

Example: Reflections with double termination

500ps rise time w/ 10pF load capacitor in a double terminated system. Estimate the reflection coefficient.

$$Z_c = \frac{V}{I} = \frac{V}{C \cdot \frac{dV}{dt}} \approx \frac{V_{0-100}}{C \cdot \frac{V_{0-100}}{t_{rise}}} = \frac{t_{rise}}{C}$$

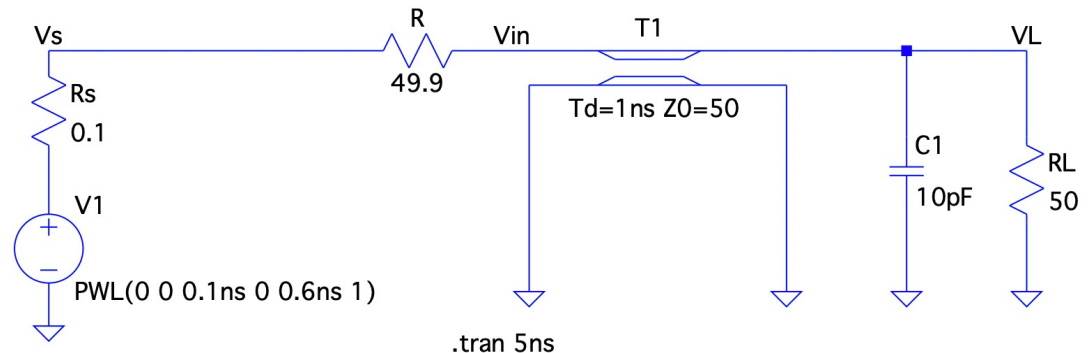
$$Z_c = \frac{t_{rise}}{C} = \frac{500p}{10p} = 50\Omega$$

R and C in parallel

$$Z_{Load} = 50\Omega // 50\Omega = 25\Omega$$

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{25 - 50}{25 + 50} = -0.333 = -33\%$$

-33% represents the maximum magnitude of the reflection that will be seen.



Double_termination.asc

Example: Reflections with double termination

500ps rise time w/ 10pF load capacitor in a double terminated system. Estimate rise time of the system.

- the resultant system risetime is increased.
- the load risetime is found using: $2.2 \cdot \tau$

Sum-of-Squares method

$$t_{rise} = \sqrt{t_{Tx}^2 + t_{Load}^2}$$

$$t_{rise} = \sqrt{t_{Tx}^2 + (2.2 \cdot \tau)^2}$$

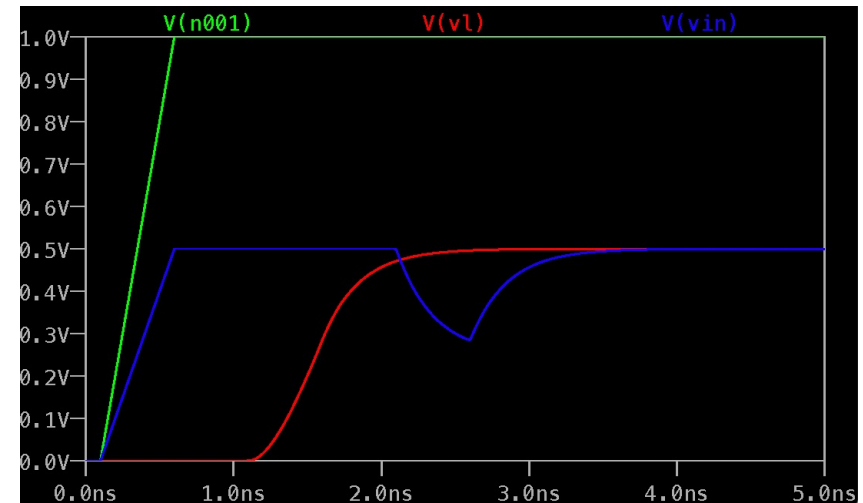
t_{Tx} : rise time of input voltage

- In this example, the load time constant is the capacitance times the parallel combination of the 50 ohm load resistor and the 50 ohm transmission line:

$$\tau = ZC = (50 // 50) \cdot (10p) = 250p$$

$$t_{rise} = \sqrt{(500p)^2 + (2.2 \cdot 250p)^2}$$

$$t_{rise} = 743ps \quad \text{rise time of overall system}$$



Which Termination to Use?

- Often times many “correct” answers
- If power is most important
 - ✓ source series termination
- If a clock net, lowest power, and minimum complexity:
 - ✓ RC termination
- If low duty cycle control line, mostly lo or mostly hi, lowest power if:
 - ✓ Far end termination to V_{GND} or V_{CC}
- Good balance between: lower power, higher noise margin, higher bandwidth, but higher cost:
 - ✓ Far end V_t termination
- But for the highest data rate:
 - ✓ It's the routing topology that sets the maximum supported data rate, not the termination strategy
 - ✓ You cannot “terminate away” reflections from poor routing topologies



Termination schemes for differential link

