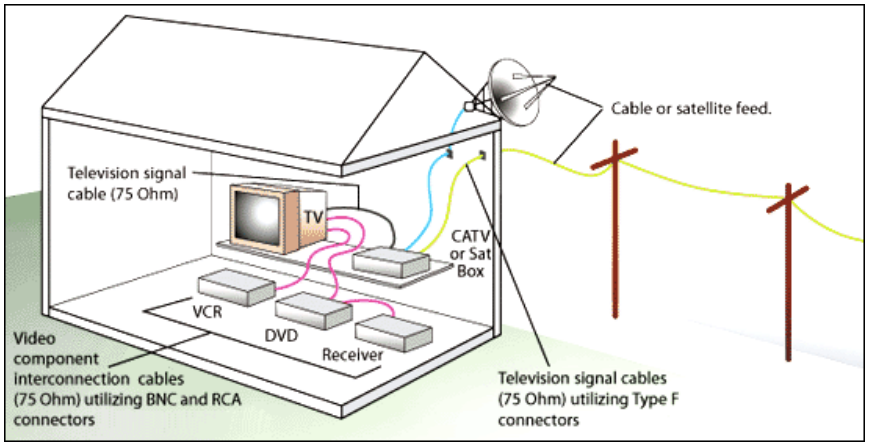
ILLINOIS
Electrical & Computer Engineering
GRAINGER COLLEGE OF ENGINEERING



Transmission Line Basics

Prof. Victoria Shao

Outlines

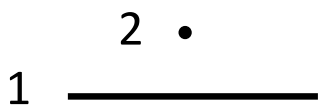
- Transmission Lines in Planar structure.
- Key Parameters for Transmission Lines.
- Transmission Line Equations.
- Per unit length parameters
- Analysis approach for Z_o and T_d
- Loss of Transmission Lines
- Example I: Connector Performance
- Example II: Transmission line on non-ideal GND
- Example III: Rambus and RIMM Module design
- Example IV: EMI resulting from a trace near a PCB edge

3.1 Transmission Lines

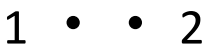
Travelling waves on transmission lines has Transverse ElectroMagnetic (TEM) field structure between conductors.

- Cross section shape doesn't change.
- electrical length of the line is long compared with wavelength.
- Cross sectional dimensions are small compared to wavelength.

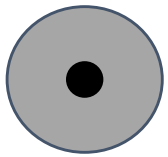
Example of structures (cross sections) that can support TEM fields given below.



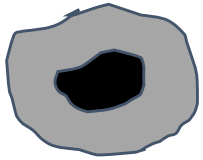
Wire above conducting plane



Parallel conductors

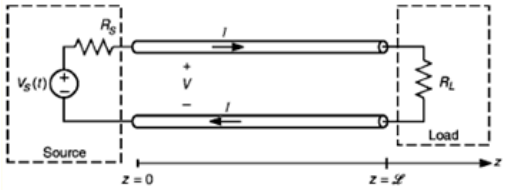


Coaxial cable

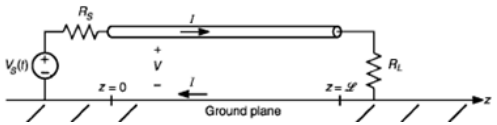


A generic coaxial structure

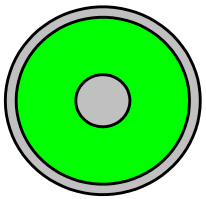
Transmission Lines in Planar structure

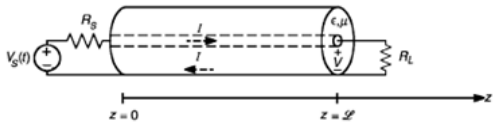


(a) Two wires



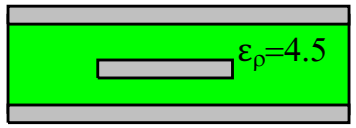
(b) One wire above an infinite ground plane



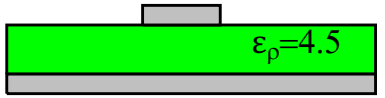


(c) Coaxial cable

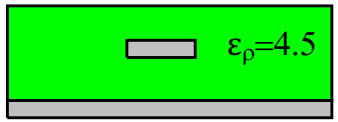
Typical wire-type transmission lines



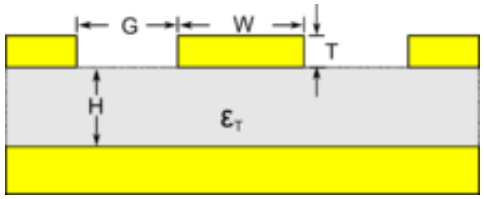
Stripline



Microstrip line



Embedded Microstrip line



Coplanar

Typical printed circuit board (PCB) structures

3.2 Key Parameters for Transmission Lines

1. Relation of V / I : Characteristic Impedance Z_0 → **Reflection** Γ
2. Velocity of Signal: Effective dielectric constant ε_r → **Time delay** T_D
3. Attenuation: Conductor loss α_c → **Loss**

   Dielectric loss $\epsilon_r = \epsilon_r' - j\epsilon_r''$

Lossless case

air

- Speed $c_o = \frac{1}{\sqrt{\epsilon_o \mu_o}} = \frac{1}{\sqrt{lc}}$
- Characteristic impedance $Z_o = \sqrt{\frac{l}{c}}$

dielectric ⇨ Speed $v_p = \frac{c}{\sqrt{\epsilon_r \mu_r}} = \frac{1}{\sqrt{lc}}$

Time delay in various mediums

$$T_d = \frac{\mathcal{L}}{v_p}$$

$\mathcal{L}$ → Total Length

v_p → velocity of propagation

1. Free space

$$v_0 = \frac{1}{\sqrt{\mu_0 \varepsilon_0}} = 3 \times 10^8 \, \mathrm{m}/s$$

Td per meter: $3.3ns / \mathrm{m}$

2. PCB (FR-4)

$$v = \frac{v_0}{\sqrt{\mu_r \varepsilon_r}} = \frac{v_0}{\sqrt{\varepsilon_r}} \approx 1.38 \times 10^8 \, \mathrm{m}/s$$

$\varepsilon_r = 4.7$

Td per meter: $7.2ns / \mathrm{m}$

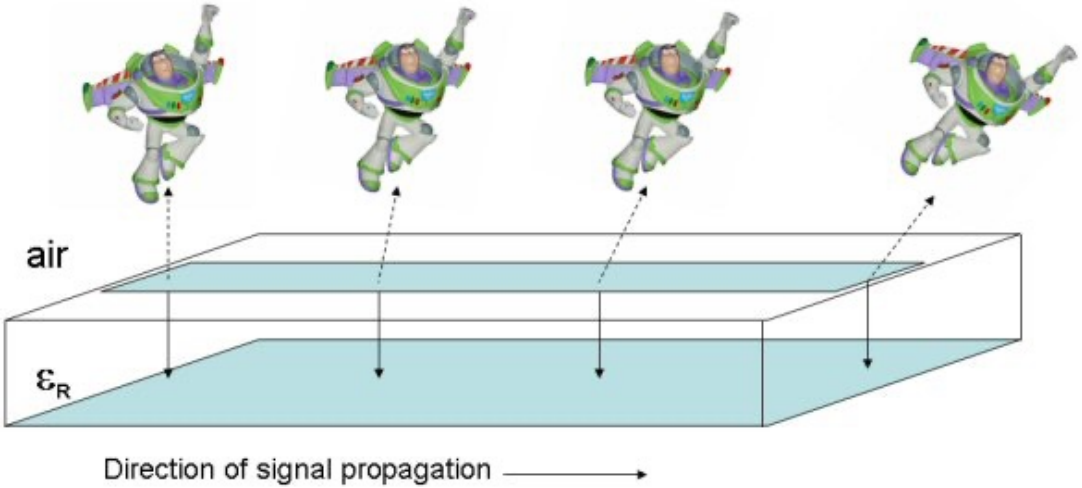
3. Microstrip Line

$$v \approx \frac{v_0}{\sqrt{\mu_r \varepsilon_r}} = \frac{v_0}{\sqrt{\varepsilon_r}} \approx 1.78 \times 10^8 \, m/s$$

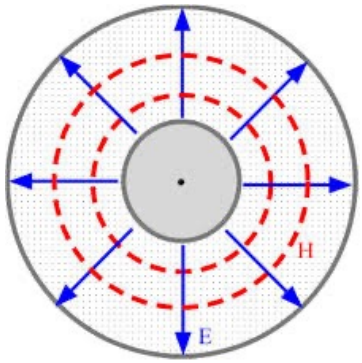
Td per meter: $5.6ns / m$

$$\varepsilon_r \approx (1 + 4.7)/2 = 2.85$$

3.3 Transmission Line Equations



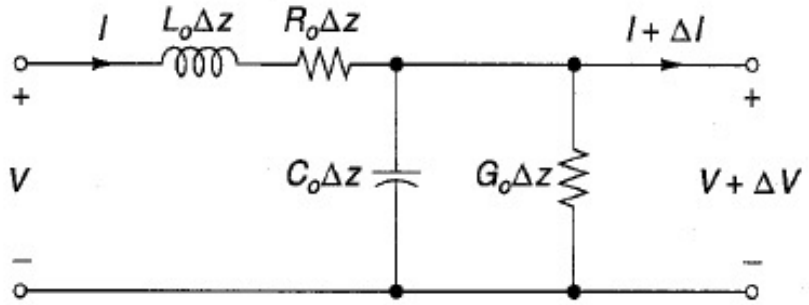
Quasi-TEM in microstrip



TEM in coaxial cable

How to calculate ϵ_{eff}?

Transmission Line Equations



R_0 = resistance per unit length(Ohm/ cm)

G_0 = conductance per unit length (S/ cm)

L_0 = inductance per unit length (H / cm)

C_0 = capacitance per unit length (F/ cm)

KVL : $\dfrac{dV}{dz} = -(R_0 + j\omega L_0)I$

KCL : $\dfrac{dI}{dz} = -(G_0 + j\omega C_0)V$

Telegrapher's equations

Solve 2nd order D.E. for V and I

Transmission Line Equations

In Lossless TL $R = 0, G = 0$

$$\frac{\partial V}{\partial z} = -L_o \frac{\partial I}{\partial t}$$
$$\frac{\partial I}{\partial z} = -C_o \frac{\partial V}{\partial t}$$

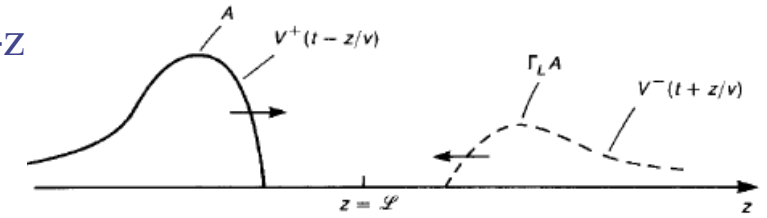
$$\Rightarrow \quad \frac{1}{L_o C_o}\frac{\partial^2 \mathrm{V}}{\partial z^2} = \frac{\partial^2 V}{\partial t^2}$$ Wave equation

The above wave equation has a solution of the form $V(z,t) = V(0, t \mp \frac{z}{v})$, which represent a wave travelling in forward direction (z direction) and a wave travelling in backward direction (-z direction), without attenuation ($R = 0$) and distortion ($G = 0$).

$v^2 \frac{\partial^2 \mathrm{V}}{\partial z^2} = \frac{\partial^2 V}{\partial t^2}$ Wave equation. Comparing, we get $v = \frac{1}{\sqrt{L_o C_o}}$

Transmission Line Equations with Loss

Two wave components with amplitudes
V+ and V- traveling in the direction of +z and -z



$$V = V^+ e^{-rz} + V^- e^{+rz}$$

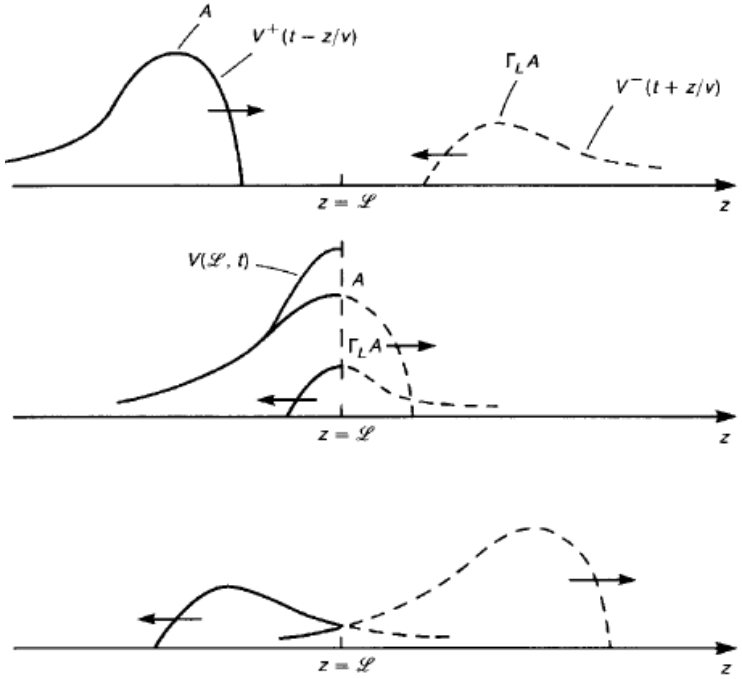
$$I = \frac{1}{Z_0}\left(V^+ e^{-rz} - V^- e^{+rz}\right) = I^+ + I^-$$

Where propagation constant and characteristic impedance are

$$\gamma = \sqrt{(R_0 + j\omega L_0)(G_0 + j\omega C_0)} = \alpha + j\beta$$

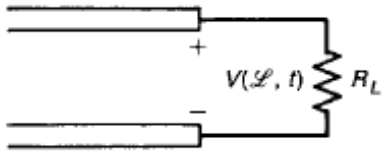
$$Z_0 = \frac{V^+}{I^+} = \frac{V^-}{I^-} = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}}$$

Reflection



Reflection of waves at a termination

When?



Mismatched lines
i.e., $\mathbf{R_L \neq Zc}$

Major aspect of degrading signal integrity!

3.4 The per-unit-length Parameters

Homogeneous structure

TEM wave structure is like the DC (static) field structure

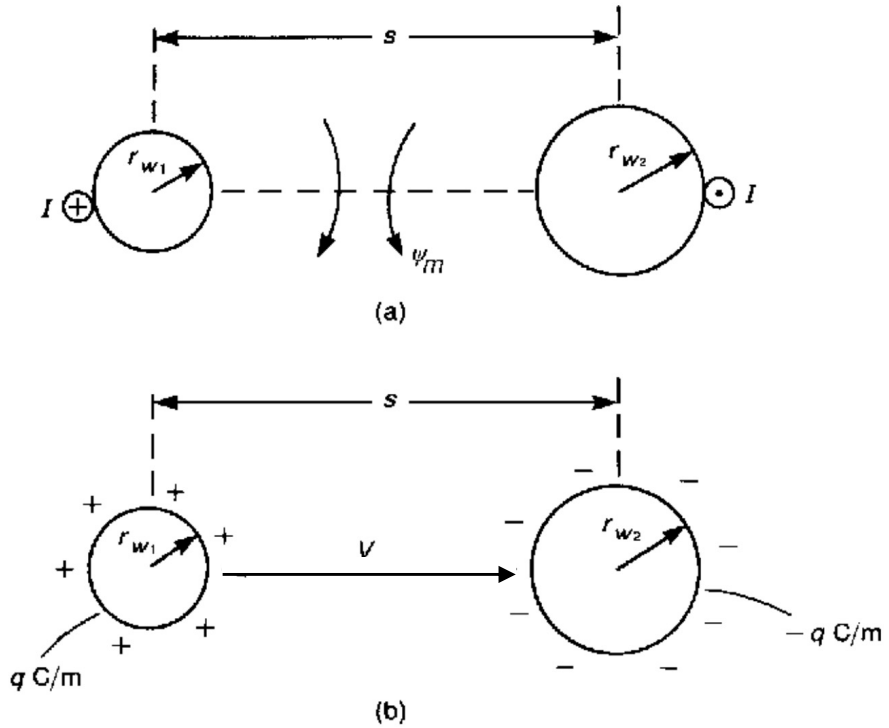
$$lc = \mu\varepsilon$$

$$lg = \mu\sigma$$

homogeneous surrounding medium

So, if you can derive how to get the *l*, *g* and *c* can be obtained by the above two relations.

Analysis approach (Wires in air)



L = ? (by L=Ψ/I)

C = ? (by C=Q/ V)

Determination of the per-unit-length parameters of a two-wire line
(a) inductance; (b) capacitance

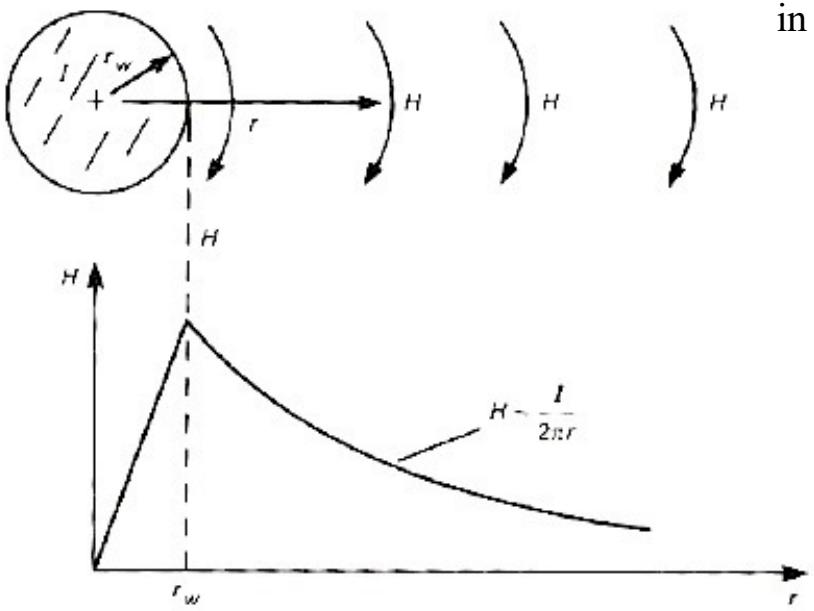
3.4.1 The per-unit-length Parameters (l)

Ampere's Law for H field

$$\oint_c H \cdot dl = \int_S J \cdot ds + \frac{d}{dt}\int_S D \cdot ds$$

in the transverse plane,

$$\oint_{c_{xy}} H_T \cdot dl = \int_{S_{xy}} J_z \cdot ds + \frac{d}{dt}\int_{S_{xy}} D_z \cdot ds$$



The magnetic field about a current-carrying wire.

Conduction current I

$$I = \int_S J \cdot ds$$

Displacement current I_d

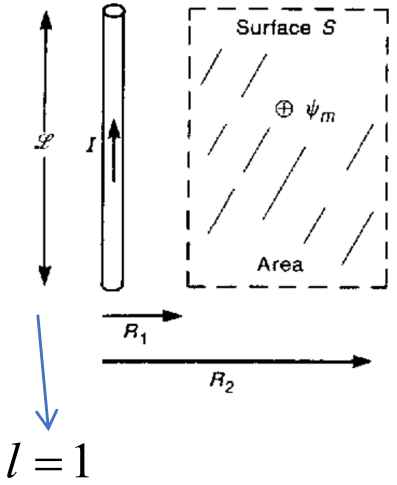
$$I_d = \frac{d}{dt}\int_S D_z \cdot ds = 0$$

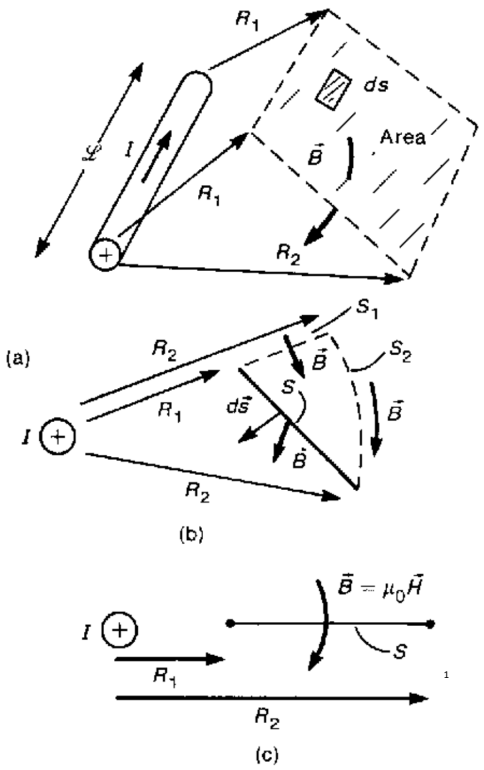
$$\Downarrow$$

$$H_T(r) = \frac{I}{\oint_c dl} = \frac{I}{2\pi r}$$

$$B_T = \mu_0 H_T$$

3.4.1 The per-unit-length Parameters (l)





$$\Psi_m = \int_S \bar{B}_T \cdot d\bar{s}$$

Gauss's Law for H field

$$= \int_{S_1} \bar{B}_T \cdot d\bar{s} + \underbrace{\int_{S_2} \bar{B}_T \cdot d\bar{s}}_{0} + \underbrace{\int_{S_{end}} \bar{B}_T \cdot d\bar{s}}_{0}$$

$$= \int_{r=R_1}^{R_2} \frac{\mu_0 I}{2\pi r} dr$$

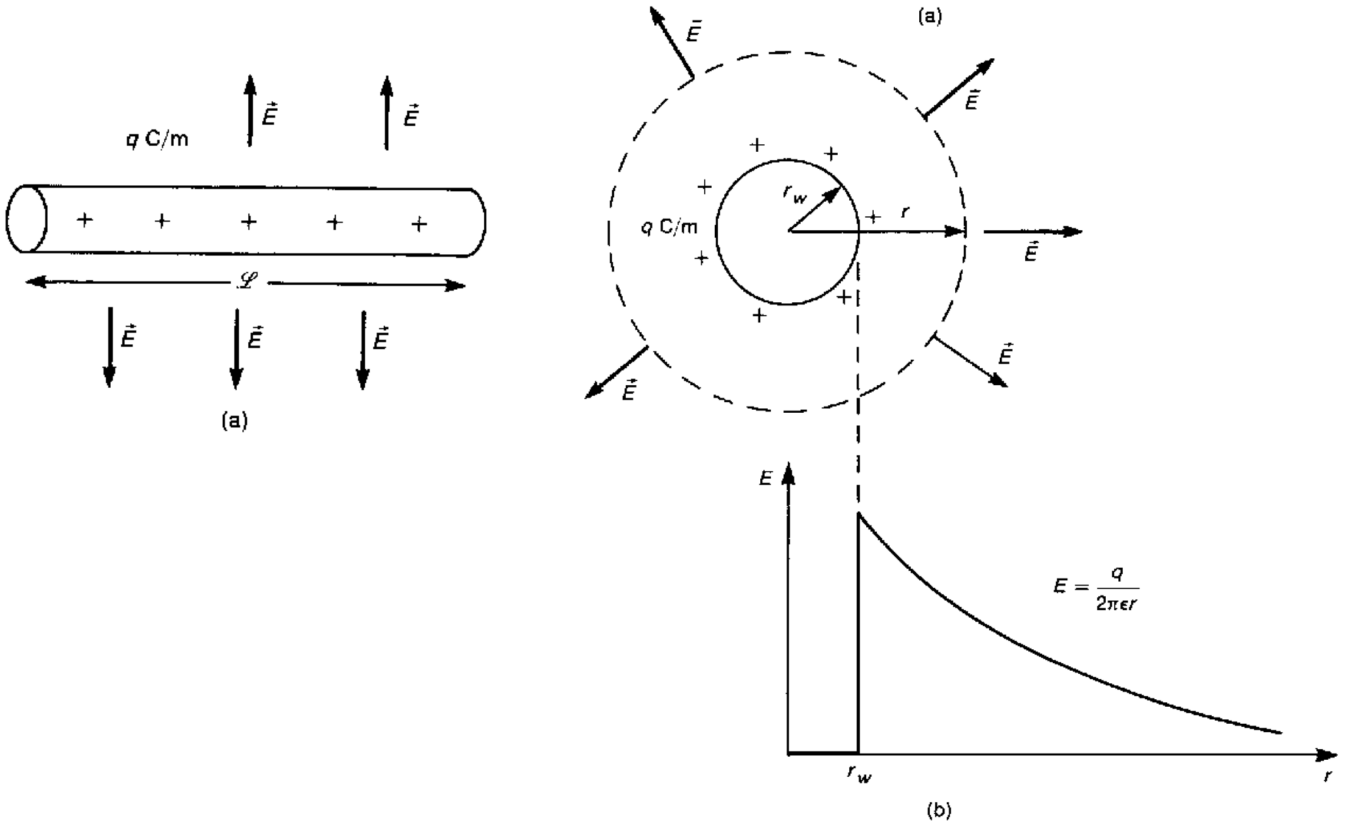
$$= \frac{\mu_0 I}{2\pi} \ln\left(\frac{R_2}{R_1}\right) \quad (\text{in Wb})$$

$$l = \frac{\psi_m}{I} = \frac{\mu_0}{2\pi} \ln\left(\frac{R_2}{R_1}\right)$$

Per unit length

Illustration of a basic subproblem of determine magnetic flux of a current through a surface: (a) dimension of the problem; (b) use of Gauss' law; (c) an equivalent but simpler problem

3.4.2 The per-unit-length Parameters (c):



The electric field about a charge-carrying wire

1) from Gauss's law

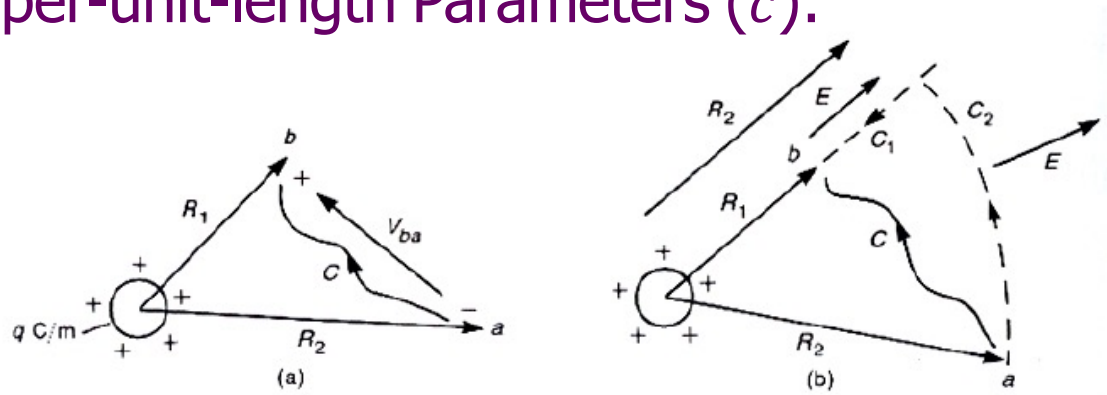
Gauss's Law for E field

$$\int_S D \cdot ds = \int_v \rho_v \, dv$$

$$\oint_s \varepsilon_0 \vec{E}_T \cdot d\vec{s} = Q_{total}$$

$$\therefore \quad \vec{E}_T = \frac{q \times 1m}{\varepsilon_0 \oint_s ds} = \frac{q}{2\pi\varepsilon_0 r}$$

3.4.2 The per-unit-length Parameters (c):



Determining the voltage between two points: (a) dimensions of the problem; (b) an equivalent but simpler problem

$$V = -\int_C \bar{E}_T \cdot d\bar{l}$$

$$= -\int_{C_1} \bar{E}_T \cdot d\bar{l} - \underbrace{\int_{C_2} \bar{E}_T \cdot d\bar{l}}_{0}$$

$$= -\int_{r=R_2}^{R_1} \frac{q}{2\pi\varepsilon_0 r} dr$$

$$= \frac{q}{2\pi\varepsilon_0} \ln\left(\frac{R_2}{R_1}\right) \quad (\text{in V})$$

$$c = \frac{q}{V} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{R_2}{R_1}\right)}$$

Example: Determine the L.C.G. of the two-wire line.

(note: homogeneous medium)

Inductance:

$$l = \frac{\Psi_m}{I}$$

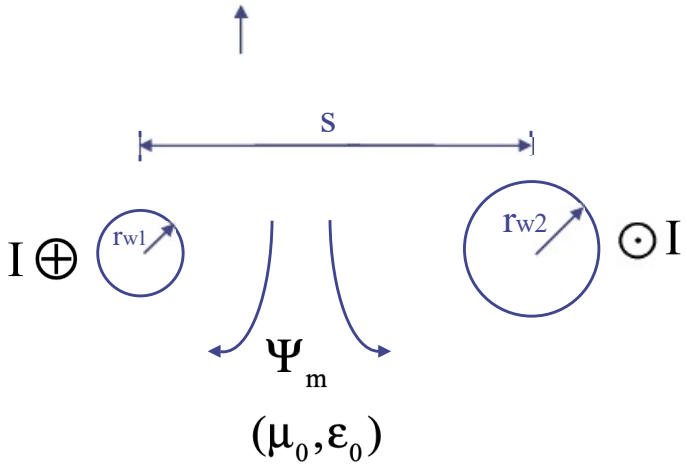
Where

$$\Psi_m = \frac{\mu_0 I}{2\pi}\ln\left(\frac{s-r_{w2}}{r_{w1}}\right) + \frac{\mu_0 I}{2\pi}\ln\left(\frac{s-r_{w1}}{r_{w2}}\right)$$

$$= \frac{\mu_0 I}{2\pi}\ln\left(\frac{(s-r_{w2})(s-r_{w1})}{r_{w1}r_{w2}}\right)$$

assume $s \gg r_{w1}, r_{w2}$

$$\Rightarrow \quad l = \frac{\mu_0}{2\pi}\ln\left(\frac{s^2}{r_{w1}r_{w2}}\right)$$



$$\psi_m = \frac{\mu_o I}{2\pi}\ln\left(\frac{R_2}{R_1}\right) \quad (R_2 > R_1) \text{ for single wire}$$

A special case, both wires have same radii

$$l = \frac{\mu_0}{\pi}\ln\left(\frac{s}{r_w}\right), \quad r_{w1} = r_{w2} = r_w$$

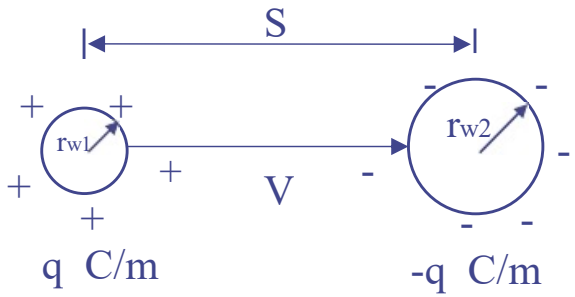
$$= 0.4\ln\left(\frac{s}{r_w}\right) \quad (\text{in } \mu\text{H/m})$$

$$= 10.16\ln\left(\frac{s}{r_w}\right) \quad (\text{in nH/in.})$$

Capacitance:

Method 1) $lc = \varepsilon\mu \qquad l = \frac{\mu_0}{2\pi}\ln\left(\frac{s^2}{r_{w1}r_{w2}}\right) \qquad (s >> r_w)$

$$\Rightarrow c = \frac{2\pi\varepsilon_0}{\ln\left(\frac{s^2}{r_{w1}r_{w2}}\right)} \qquad (\text{in F/m})$$



Method 2)

$$V = \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{s-r_{w2}}{r_{w1}}\right) + \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{s-r_{w1}}{r_{w2}}\right)$$

$$= \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{(s-r_{w2})(s-r_{w1})}{r_{w1}r_{w2}}\right)$$

$$\cong \frac{q}{2\pi\varepsilon_0}\ln\left(\frac{s^2}{r_{w1}r_{w2}}\right) \qquad \text{if } s \gg r_{w1}, r_{w2}$$

$$\Rightarrow c = \frac{q}{V} = \frac{2\pi\varepsilon_0}{\ln\left(\frac{s^2}{r_{w1}r_{w2}}\right)} \qquad (\text{in F/m})$$

← the same with 1st method

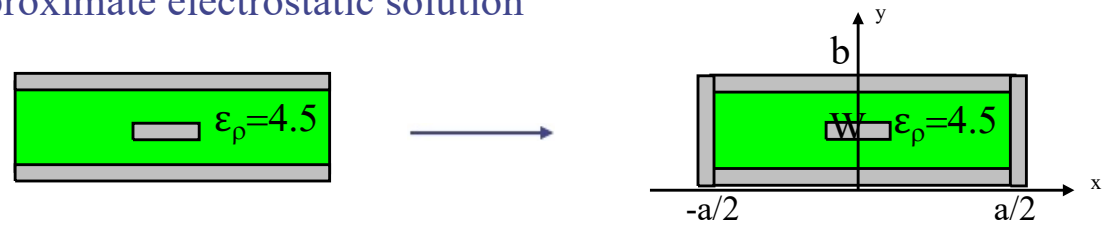
$$V = \frac{q}{2\pi\epsilon_o}\ln\left(\frac{R_2}{R_1}\right) \quad (R_2 > R_1)$$
for single wire

A special case, both wires have same radii

$$c = \frac{\pi\epsilon_o}{\ln\left(\frac{s}{r_w}\right)}, \qquad r_{w1} = r_{w2} = r_W$$

3.5 Analysis approach for Z_0 and Td (Stripline)

Approximate electrostatic solution

1. 

Homogeneous medium

2. The fields in TEM mode must satisfy Laplace equation

$$\nabla^2 \Phi_t\ (x,y) = \frac{\partial^2 \phi_x}{dx^2} + \frac{\partial^2 \phi_y}{dy^2} + \cancel{\frac{\partial^2 \phi_y}{dy^2}} = 0$$

where Φ is the electric potential

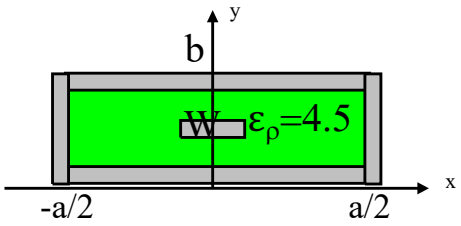
The boundary conditions are

$$\Phi(x,y) = 0 \quad at\ x = \pm\frac{a}{2}$$
$$\Phi(x,y) = 0 \quad at\ y = 0, b$$

$$\sinh(x) = \frac{e^{x} - e^{-x}}{2}$$

Analysis approach for Z_0 and Td

3. Since the center conductor will contain the surface charge, so



$$\Phi(x,y) = \begin{cases} \sum_{\substack{n=1 \\ odd}}^{\infty} A_n \cos\frac{n\pi x}{a}\sinh\frac{n\pi y}{a} & \text{for } 0 \le y \le b/2 \quad \text{(bottom half)} \\ \sum_{\substack{n=1 \\ odd}}^{\infty} B_n \cos\frac{n\pi x}{a}\sinh\frac{n\pi}{a}(b-y) & \text{for } b/2 \le y \le b \quad \text{(top half)} \end{cases}$$

Why?

4. The unknowns A_n and B_n can be solved by two known conditions:

The potential at $y = b/2$ must continuous

The surface charge distribution for the strip: $\rho_s = \begin{cases} 1 & \text{for } |x| \le W/2 \\ 0 & \text{for } |x| \ge W/2 \end{cases}$

Analysis approach for Z_0 and Td

5. $$\begin{cases} V = -\int_0^b E_y(x=0,y)dy = -\int_0^b -\partial\Phi(x,y)/\partial y(x=0,y)dy \\ Q = \int_{-w/2}^{w/2} \rho_s(x)dx = W(C/m) \end{cases}$$

6. $$C = \frac{Q}{V} = \frac{W}{\sum_{\substack{n=1 \\ odd}}^{\infty} \frac{2a\sin(n\pi W/2a)\sinh(n\pi b/2a)}{(n\pi)^2 \varepsilon_0 \varepsilon_r \cosh(n\pi b/2a)}}$$

$$Z_0 = \frac{1}{v_p C} = \frac{\sqrt{\varepsilon_r}}{cC}$$ Characteristic impedance

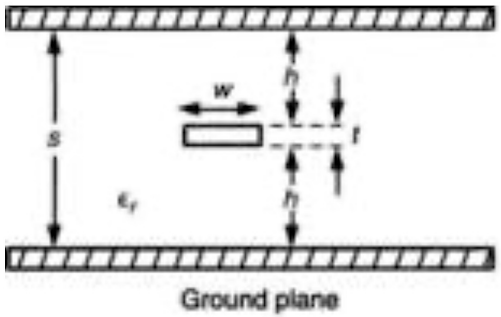
Answers!!

7. $$T_d = \frac{1}{v_p} = \frac{\sqrt{\epsilon_r}}{c}$$ Time delay

Approximate Solution for Z_0 and Td

Assume a zero thickness strip, $t = 0$

$$Z_c = \frac{30\pi}{\sqrt{\epsilon_r}} \frac{1}{\left[\frac{w_e}{s} + 0.441\right]}$$



Stripline

Where the effective width of the center conductor is

$$\frac{w_e}{s} = \begin{cases} \frac{w}{s} & \frac{w}{s} \geq 0.35 \\ \frac{w}{s} - \left(0.35 - \frac{w}{s}\right)^2 & \frac{w}{s} \leq 0.35 \end{cases}$$

$$Z_o = \frac{1}{V_p C} = \frac{\sqrt{\epsilon_r}}{cC}$$

$$C = \frac{\sqrt{\epsilon_r}}{cZ_o}$$

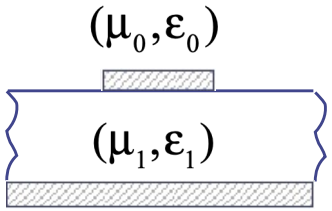
Per-unit-length capacitor

$$T_d = \frac{1}{v_p} = \frac{\sqrt{\epsilon_r}}{c}$$

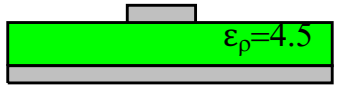
Time delay

c: speed of light

d. How to determine L,C for microstrip-line.



1) This is inhomogeneous medium.
2) Numerical method should be used to solve the capacitance C of this structure, such as Finite element, Finite Difference...
3) But L can be obtained by

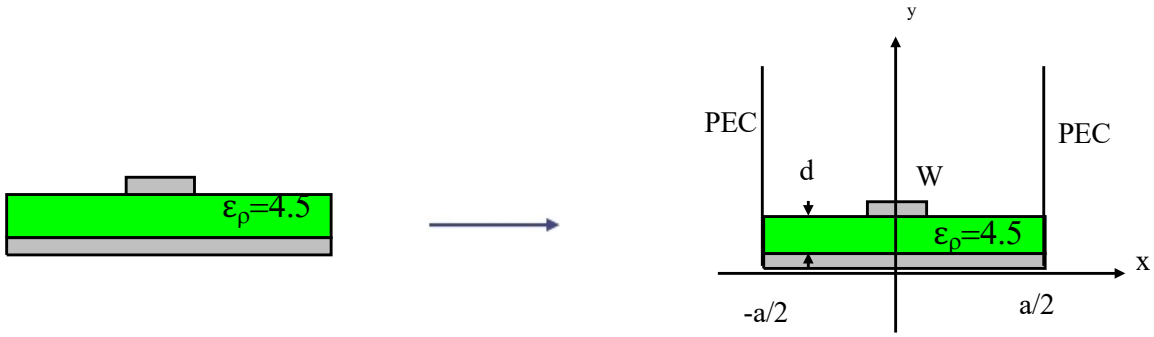


$$LC = \mu\epsilon_e \qquad \Longrightarrow \qquad L = \frac{\mu\epsilon_e}{C}$$

where ϵ_e is effective permittivity of medium 0 and medium 1.

Analysis approach for Z_0 and Td (Microstrip Line)

1.



2.

The fields in Quasi-TEM mode must satisfy Laplace equation

$$\nabla_t^2 \Phi(x,y) = 0$$

where Φ is the electric potential

The boundary conditions are

$$\Phi(x,y) = 0 \quad \text{at } x = \pm a/2$$

$$\Phi(x,y) = 0 \quad \text{at } y = 0, \infty$$

Analysis approach for Z_0 and Td (Microstrip Line)

3. Since the center conductor will contain the surface charge, so

$$\Phi(x,y)=\begin{cases}\displaystyle\sum_{\substack{n=1\\ odd}}^{\infty} A_n \cos\frac{n\pi x}{a}\sinh\frac{n\pi y}{a} & \text{for } 0\le y\le d \quad \text{(in dielectric)}\\ \displaystyle\sum_{\substack{n=1\\ odd}}^{\infty} B_n \cos\frac{n\pi x}{a}e^{-n\pi y/a} & \text{for } d\le y\le\infty \quad \text{(in air)}\end{cases}$$

4. The unknowns A_n and B_n can be solved by two known conditions and the orthogonality of *cos* function :

The potential at $y = d$ must continuous

The surface charge distribution for the strip: $\rho_s=\begin{cases}1 & \text{for } |x|\le W/2\\ 0 & \text{for } |x|\ge W/2\end{cases}$

Analysis approach for Z_0 and Td (Microstrip Line)

5. $$\begin{cases} V = -\int_0^{b/2} E_y(x=0,y)dy = -\int_0^{b/2} -\partial\Phi(x,y)/\partial y(x=0,y)dy = \sum_{\substack{n=1 \\ odd}}^{\infty} A_n \sinh\frac{n\pi d}{a} \\ Q = \int_{-w/2}^{w/2} \rho_s(x)dx = W(C/m) \end{cases}$$

6. $$C = \frac{Q}{V} = \frac{W}{\sum_{\substack{n=1 \\ odd}}^{\infty} \frac{4a\sin(n\pi W/2a)\sinh(n\pi d/2a)}{(n\pi)^2 W\varepsilon_0[\sinh(n\pi d/a)+\varepsilon_r\cosh(n\pi d/a)]}}$$

Analysis approach for Z_0 and Td (Microstrip Line)

7.

To find the effective dielectric constant ε_e, we consider two cases of capacitance

1. C = capacitance per unit length of the microstrip line with the dielectric substrate $\varepsilon_r \neq 1$
2. C_0 = capacitance per unit length of the microstrip line with air, $\varepsilon_r = 1$

$$\varepsilon_e = \frac{C}{C_0}$$

8.

Characteristic impedance

$$Z_0 = \frac{1}{v_p C} = \frac{\sqrt{\varepsilon_e}}{cC}$$

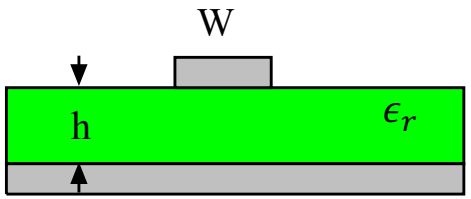
Time delay

$$T_d = \frac{1}{v_p} = \frac{\sqrt{\epsilon_e}}{c}$$

Approximate approach for Z_0 and Td (Microstrip Line)

The characteristic impedance is given as*

$$Z_C = \begin{cases} \dfrac{60}{\sqrt{\epsilon_r'}} \ln\left[\dfrac{8h}{w} + \dfrac{w}{4h}\right] & \dfrac{w}{h} \le 1 \\ \dfrac{120\pi}{\sqrt{\epsilon_r'}\left[\dfrac{w}{h} + 1.393 + 0.667 \ln\left(\dfrac{w}{h} + 1.444\right)\right]^{-1}} & \dfrac{w}{h} \ge 1 \end{cases}$$



The effective relative permittivity is

$$\epsilon_r' = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 10h/w}}$$

Then, Velocity of propagation $v = c/\sqrt{\epsilon_r'}$

per-unit-length parameters $l = \frac{Z_c}{v}, c = \frac{1}{vZ_c}$

Time delay per unit length $T_d = \frac{1}{v} = \sqrt{\epsilon_r'}/c$

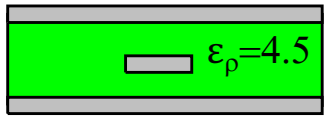
A simpler (less accurate) approximation

$$\epsilon_r' \approx \begin{cases} \epsilon_r & h \ll w \\ \dfrac{\epsilon_r + 1}{2} & h \gg w \end{cases}$$

$$Z_c = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

*Cohn, Problems in strip TL, 1955

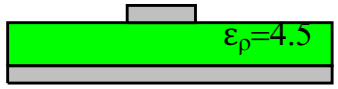
Tables for Z_0 and Td (Stripline)



$Z_0(\Omega)$	20	28	40	50	75	90	100
ε_{eff}	4.5	4.5	4.5	4.5	4.5	4.5	4.5
L (nH/mm)	0.141	0.198	0.282	0.353	0.53	0.636	0.707
C (pF/mm)	0.354	0.252	0.171	0.141	0.094	0.078	0.071
T_d (ps/mm)	7.09	7.09	7.09	7.09	7.09	7.09	7.09

Fr4 : dielectric constant = 4.5
Frequency: 1GHz

Tables for Z_0 and Td (Microstrip Line)



$Z_0(\Omega)$	20	28	40	50	75	90	100
ε_{eff}	3.8	3.68	3.51	3.39	3.21	3.13	3.09
L (nH/mm)	0.119	0.183	0.246	0.320	0.468	0.538	0.591
C (pF/mm)	0.299	0.233	0.154	0.128	0.083	0.067	0.059
T_d (ps/mm)	6.54	6.41	6.25	6.17	5.99	5.92	5.88

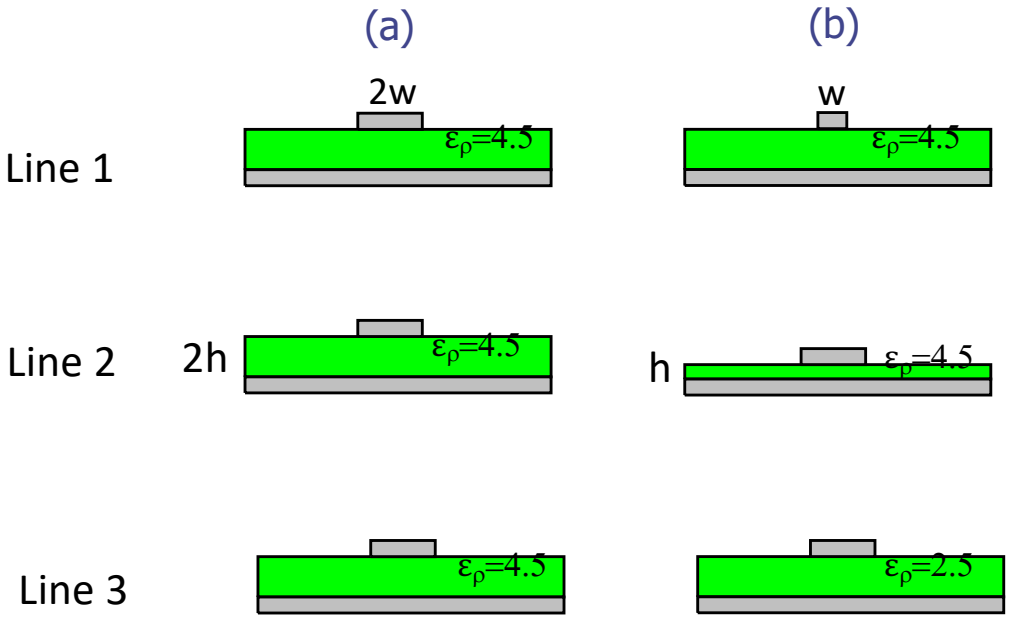
Fr4 : dielectric constant = 4.5
Frequency: 1GHz

Analysis approach for Z_o and T_d (EDA/Simulation Tool)

1. Cadence AWR Microwave Office
    - Free academic access available to students
    - RF/microwave circuit, transmission-line, and layout design
2. Ansys Electronics Desktop (HFSS)
    - Free Student version; EWS access may also be available
    - 3D full-wave electromagnetic field solver
3. SIMULIA CST Studio Suite
    - Free Learning Edition available to students
    - 3D electromagnetic simulation with multiple solver types
4. Other commercial EDA / EM simulation tools

Concept Test for Planar Transmission Lines

- Poll: Please compare their Z_0 and T_d



$$C = \epsilon \frac{A}{d}$$

$$Z_0 = \frac{1}{v_p C} = \frac{\sqrt{\varepsilon_e}}{cC}$$

$$T_d = \frac{\sqrt{\epsilon_e}}{c}$$

c: speed of light
C: Capacitance

3.6 Loss of Transmission Lines

Typically, dielectric loss is quite small -> $G_0 = 0$. Thus

$$r = \sqrt{(R_0 + j\omega L_0)(G_0 + j\omega C_0)} = \alpha + j\beta$$

$$Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} = \sqrt{\frac{L_0}{C_0}}\sqrt{1 - jx}$$

where

$$x = \frac{R_0}{\omega L_0}$$

- Lossless case : $x = 0$
- Near Lossless: $x << 1$
- Highly Lossy: $x >> 1$

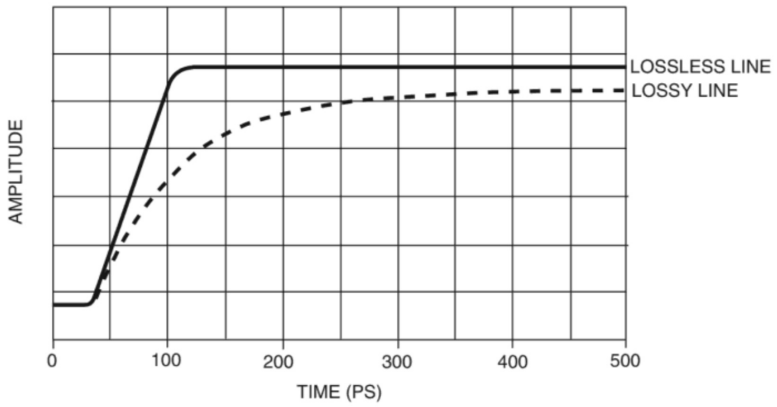


FIGURE 5-21. Time domain response of a square wave on a lossy transmission line, showing both amplitude and rise time degradation.

Example: Loss of Transmission Lines

Example of RC transmission line: AWG 24 telephone line in home, where

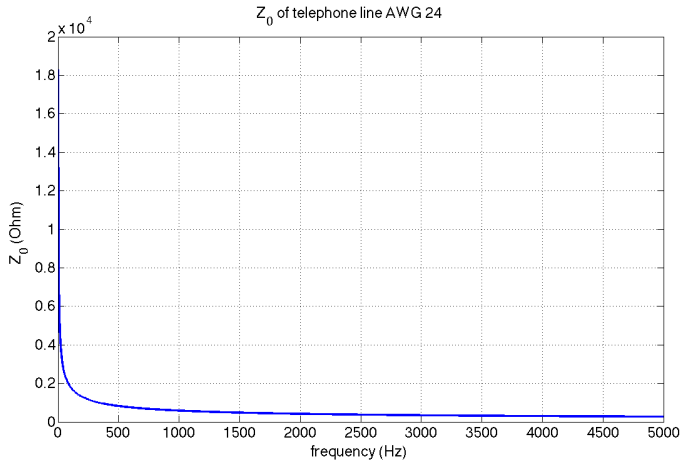
$$R = 0.0042\Omega / \text{in}$$
$$L = 10\text{nH} / \text{in}$$
$$C = 1\text{pF} / \text{in}$$
$$\omega = 10{,}000\text{rad} / \text{s}(1600\text{Hz})$$

voice band

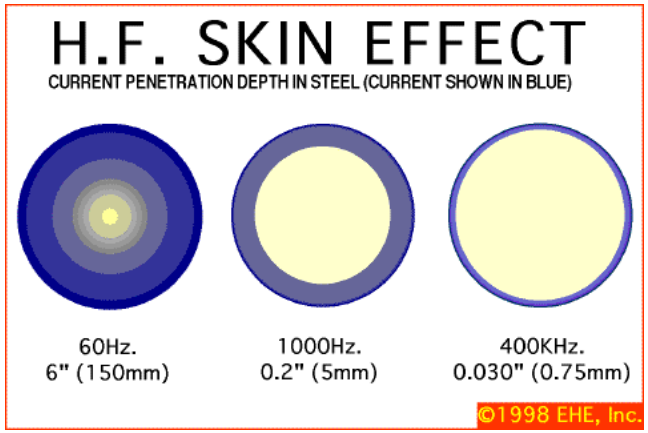
Calculate the characteristic impedance of the line.

$$Z_0(\omega) = \sqrt{\frac{R + j\omega L}{j\omega C}} = 648(1 + j)$$

That's why telephone company terminate the lines with 600 ohm



Loss of Transmission Lines (Skin Effect)



Skin depth $\delta = \sqrt{\dfrac{2}{\omega\mu\sigma}}$

$$R(\omega) = \frac{L}{\sigma A} \propto \sqrt{\omega}$$

NOTE: In the near lossless region (R / ωL << 1), the characteristic impedance Z_0 is not much affected by the skin effect

$$\because R(\omega) \propto \sqrt{\omega}$$
$$\therefore R(\omega)/\omega L \propto \left(1/\sqrt{\omega}\right) << 1$$

Loss of Transmission Lines

- Skin Effect

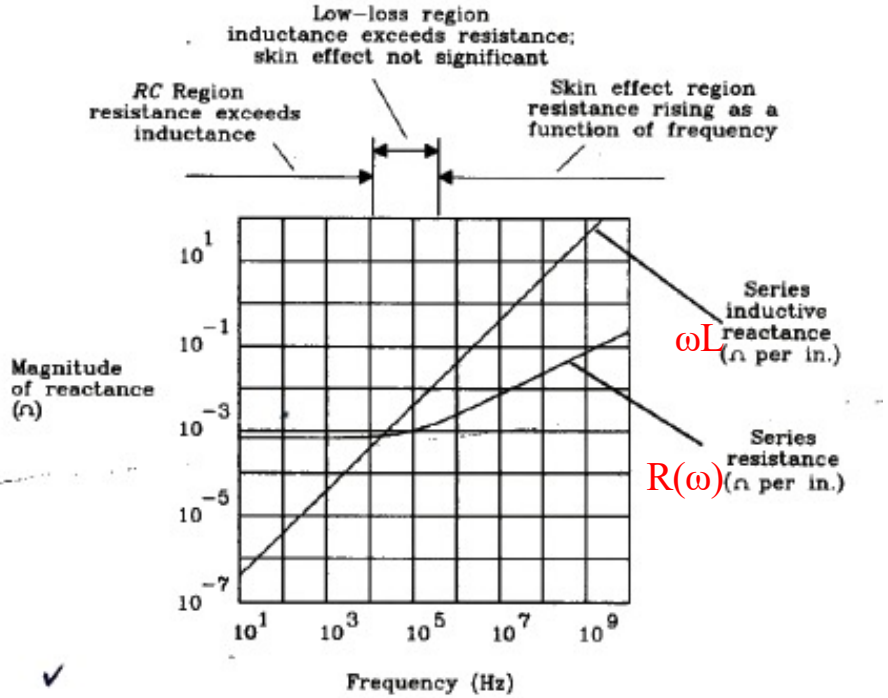
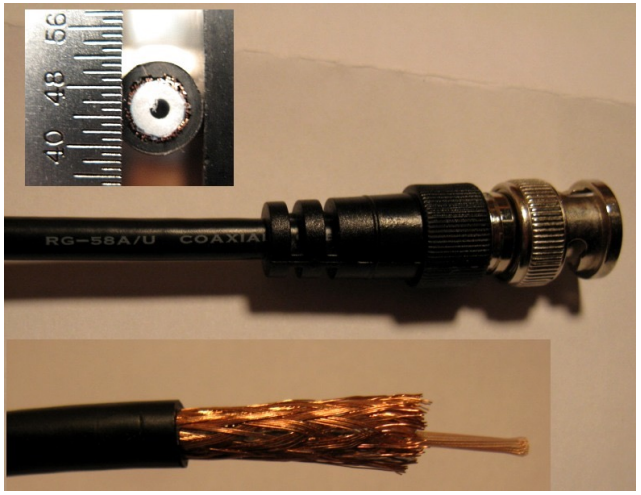


Figure 4.10 Series resistance and series inductive reactance of RG-58/U coax versus frequency.



Example: Loss of Transmission Lines (Skin Effect)

f	MHz	100	200	400	800	1200	1600	2000	4000
$\delta_s = \sqrt{\frac{1}{\pi f \mu \sigma}}$	μm	6.6	4.7	3.3	2.4	1.9	1.7	1.5	1.0
Rs	$m\Omega$/mm	2.6	3.7	5.2	7.4	9.0	10.8	11.6	16.5
Trace Resistance (60cm)	Ω	1.56	2.22	3.12	4.44	5.4	6.48	7.0	9.9

Skin depth resistance $R_s = \sqrt{\frac{\pi \mu f}{\sigma}} \times \frac{1}{2(w+h)}$ Ω

$\mu = 4\pi \times 10^{-7}$ H / m

$\sigma(\text{Cu}) = 5.8 \times 10^{7}$ S / m

Length of trace = 60cm

Loss of Transmission Lines (Dielectric Loss)

The loss of dielectric loss is described by the loss tangent

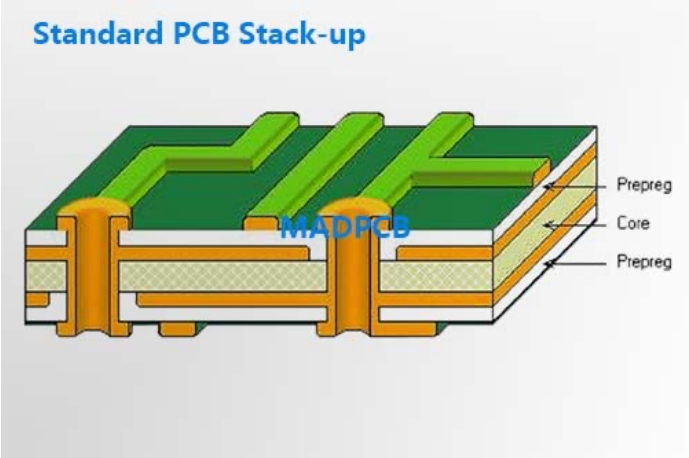
$$\epsilon_r = \epsilon_r' - j\epsilon_r''$$

$$\tan\theta = \frac{\varepsilon_r''}{\varepsilon_r'}$$

FR4 PCB $\tan\theta = 0.0035$

Material	tan δ
Ceramics	
Al_2O_3	0.0002–0.01
SiO_2	0.00038
$BaTiO_3$	0.0001–0.02
Mica	0.0016
Pyrex glass	0.006–0.025
Steatite ($2SiO_2 \cdot MgO$)	0.0002–0.004
Forsterite ($2MgO \cdot SiO_2$)	0.0004
Cordierite ($2MgO \cdot 2Al_2O_3 \cdot 5SiO_2$)	0.004–0.012
Polymers	
Phenol formaldehyde (Bakelite)	0.06–0.10
Silicone rubber	0.001–0.025
Epoxy	0.002–0.010
Nylon 6,6	0.01
Polycarbonate	0.0009
Polystyrene	0.0001–0.0006
High-density polyethylene	< 0.0001
Polytetrafluoroethylene	0.0002
Polyvinylchloride	0.007–0.020

Loss Example: Gigabit differential transmission lines



Standard Multi-layer PCB Stack-ups

For comparison: (Set Conditions)

1. Differential impedance = 100
2. Trace width fixed to 8mil
3. Coupling coefficient = 5%
4. Metal : 1 oz Copper

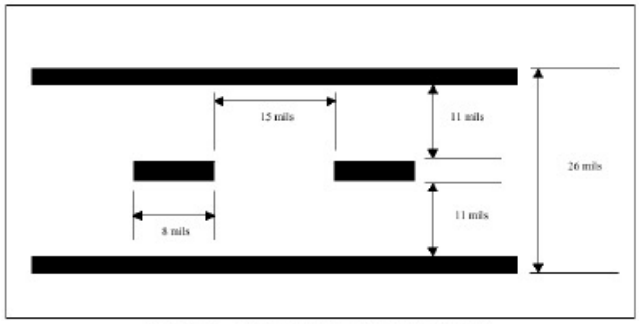


Figure 14 - Single Stripline Coplanar Geometry

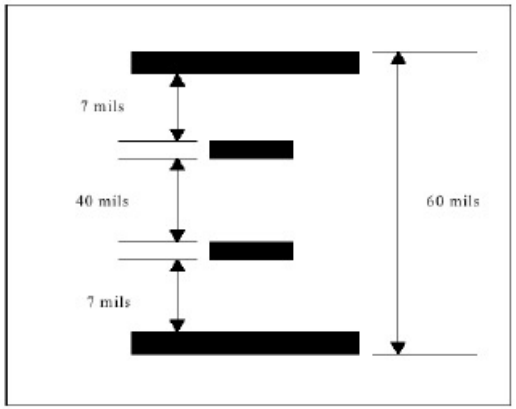


Figure 15 - Dual Stripline Geometry

1. For common-mode signals, which one has larger conductor loss by skin effect?
2. Which one has larger dielectric loss?

Loss Example: Gigabit differential transmission lines

Skin effect loss

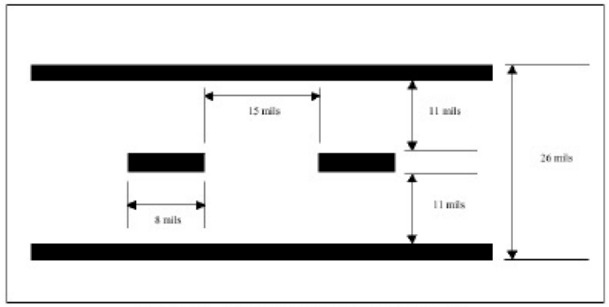


Figure 14 - Single Stripline Coplanar Geometry

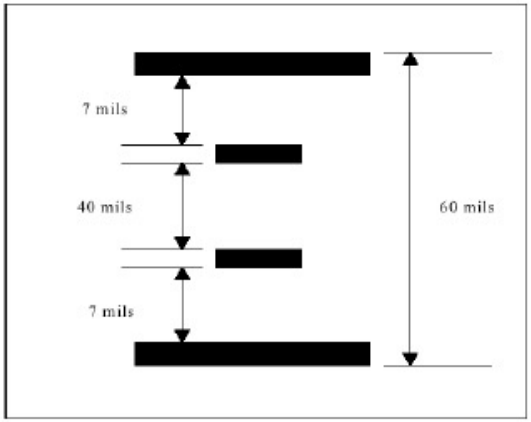


Figure 15 - Dual Stripline Geometry

Frequency	Stripline Resistance Ω / feet	Dual Stripline Resistance Ω / feet	Percent Difference
500 MHz	6.144	6.648	8.2%
1.5 GHz	10.668	11.508	7.9%
2.5 GHz	13.728	14.832	8.0%

Table 3 - Simulated Results of Skin Effect Losses

Loss Example: Gigabit differential transmission lines

Skin effect loss

Why?

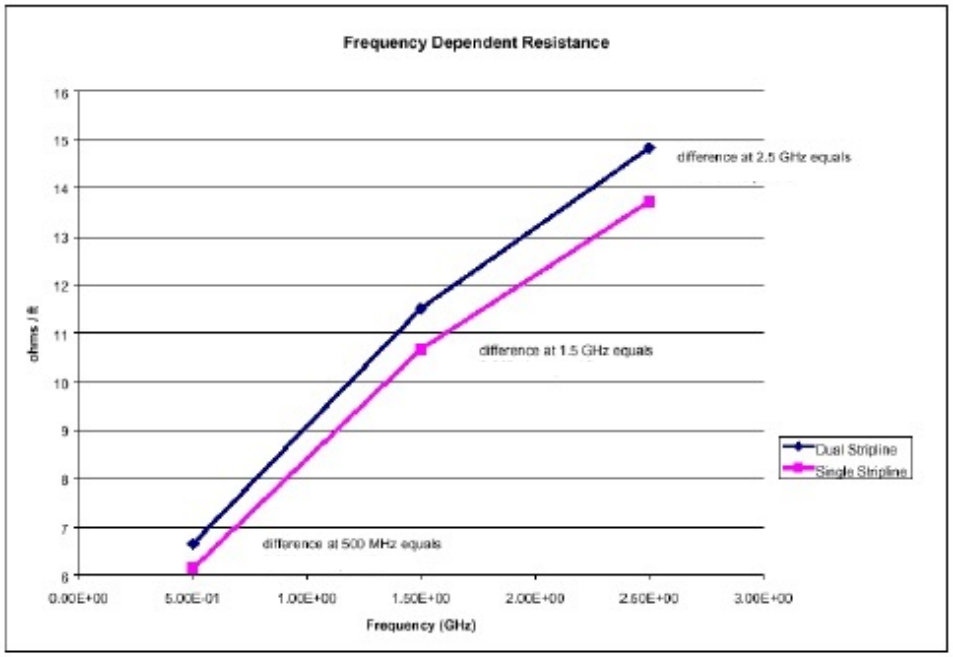


Figure 18 - Graph of Simulated Results of Skin Effect Losses

Loss Example: Gigabit differential transmission lines

Look at the field distribution of the common-mode coupling

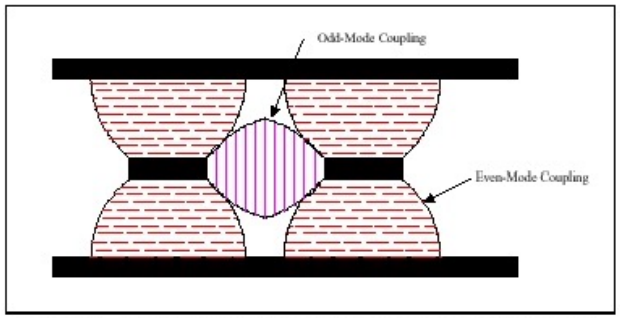


Figure 11 - Coplanar Differential Single Stripline Routing Geometry

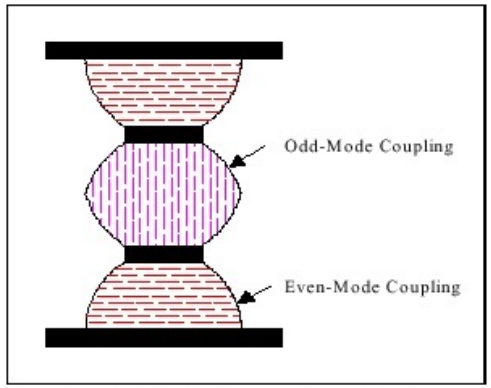


Figure 12 - Differential Routing in a Dual Stripline Geometry

Coplanar structure has more surface for current flowing → Dual stripline has larger common-mode resistance

Poll: Which structure has smaller differential mode resistance?

Loss Example: Gigabit differential transmission lines

How about the dielectric loss ? Which one is larger?

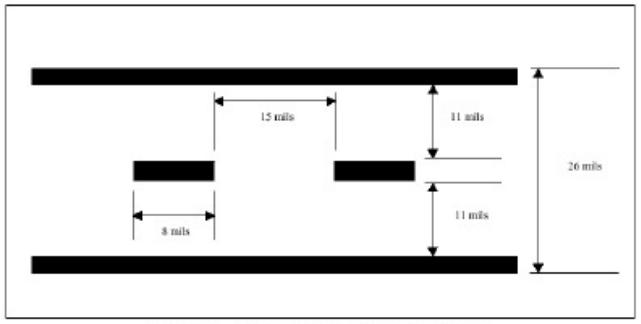


Figure 14 - Single Stripline Coplanar Geometry

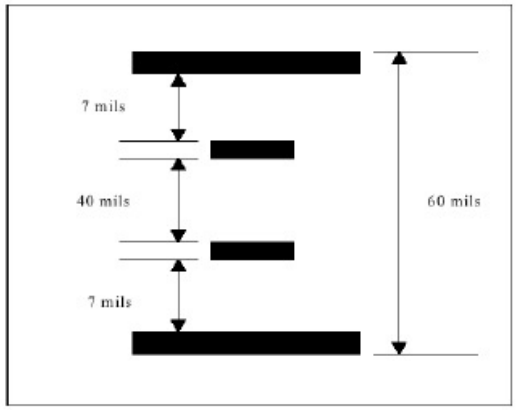


Figure 15 - Dual Stripline Geometry

Loss Example: Gigabit differential transmission lines

The answer is dual stripline has larger loss. Why ?

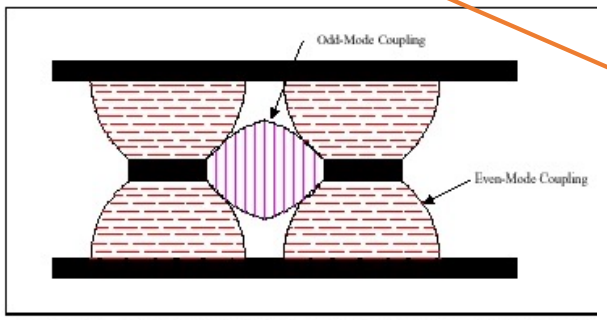


Figure 11 - Coplanar Differential Single Stripline Routing Geometry

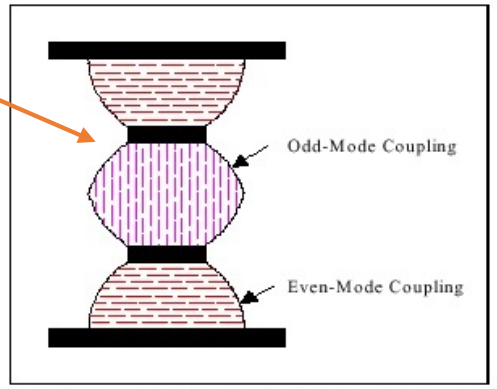


Figure 12 - Differential Routing in a Dual Stripline Geometry

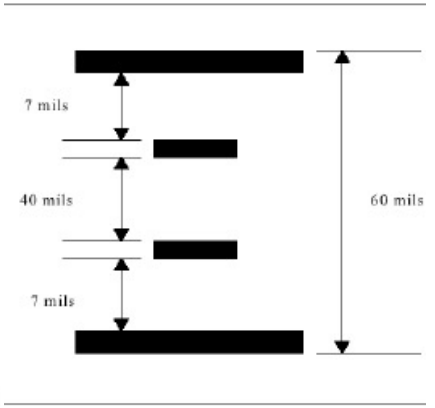
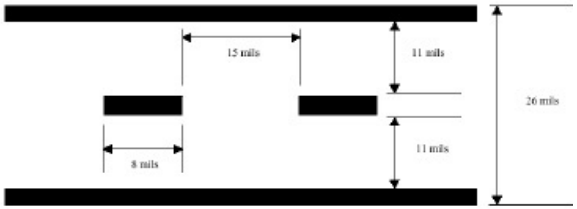


Figure 15 - Dual Stripline Geometry



Loss Example: Gigabit differential transmission lines

Which one has higher ability of rejecting common-mode noise ?

The answer is coplanar stripline. Why ?

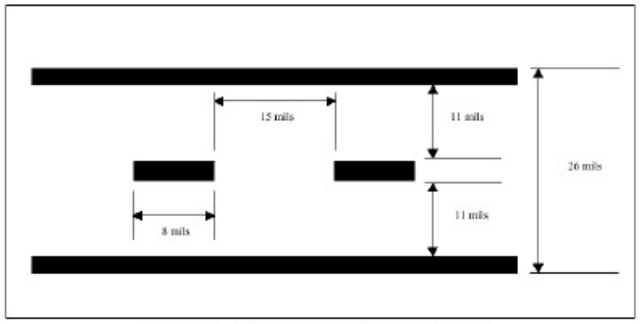


Figure 14 - Single Stripline Coplanar Geometry

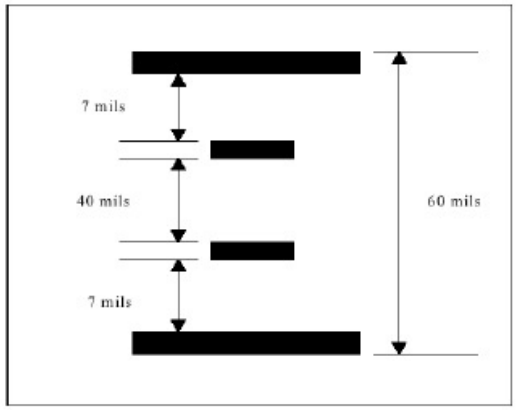
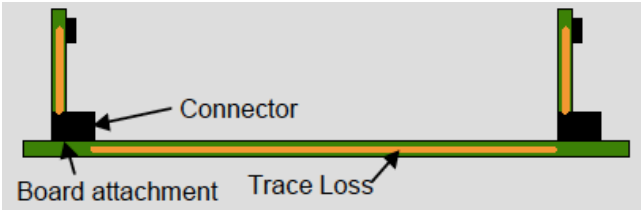
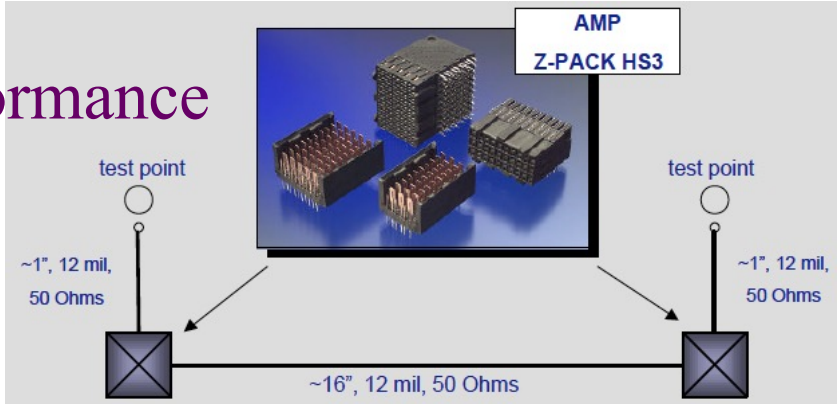
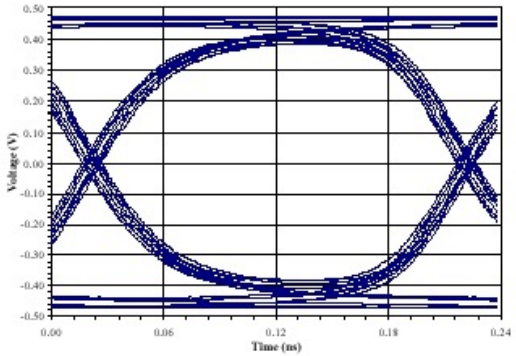


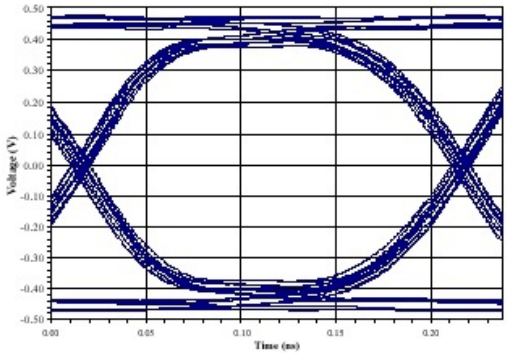
Figure 15 - Dual Stripline Geometry

3.7 Example I: Connector Performance







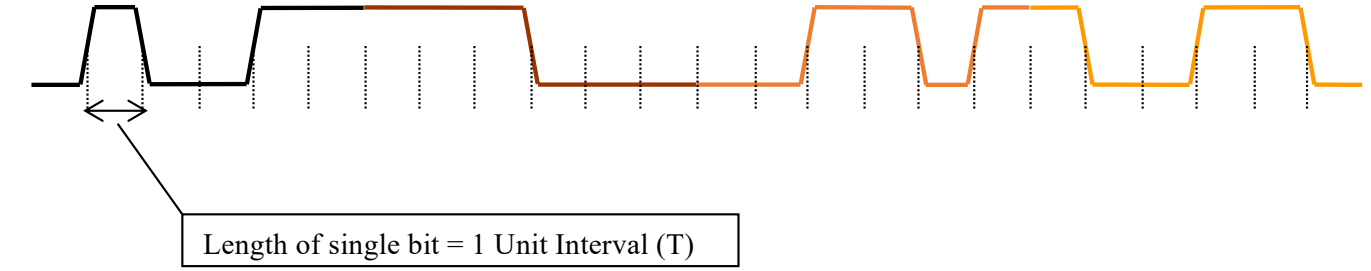


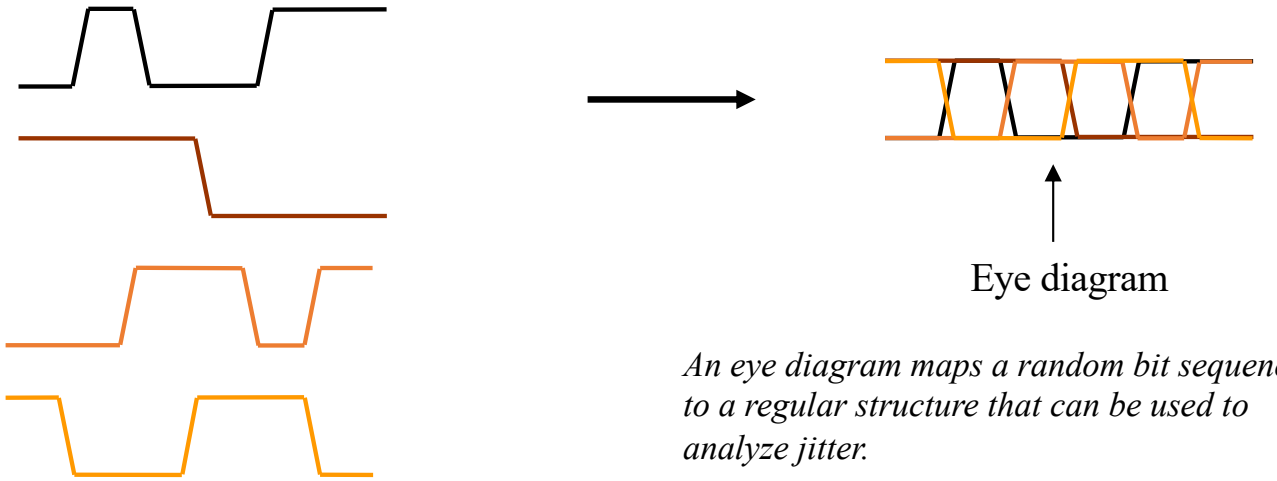
769 mV Opening, 6.25% Jitter

754 mV Opening, 6.25% Jitter

Comparison of HS3 connector to trace

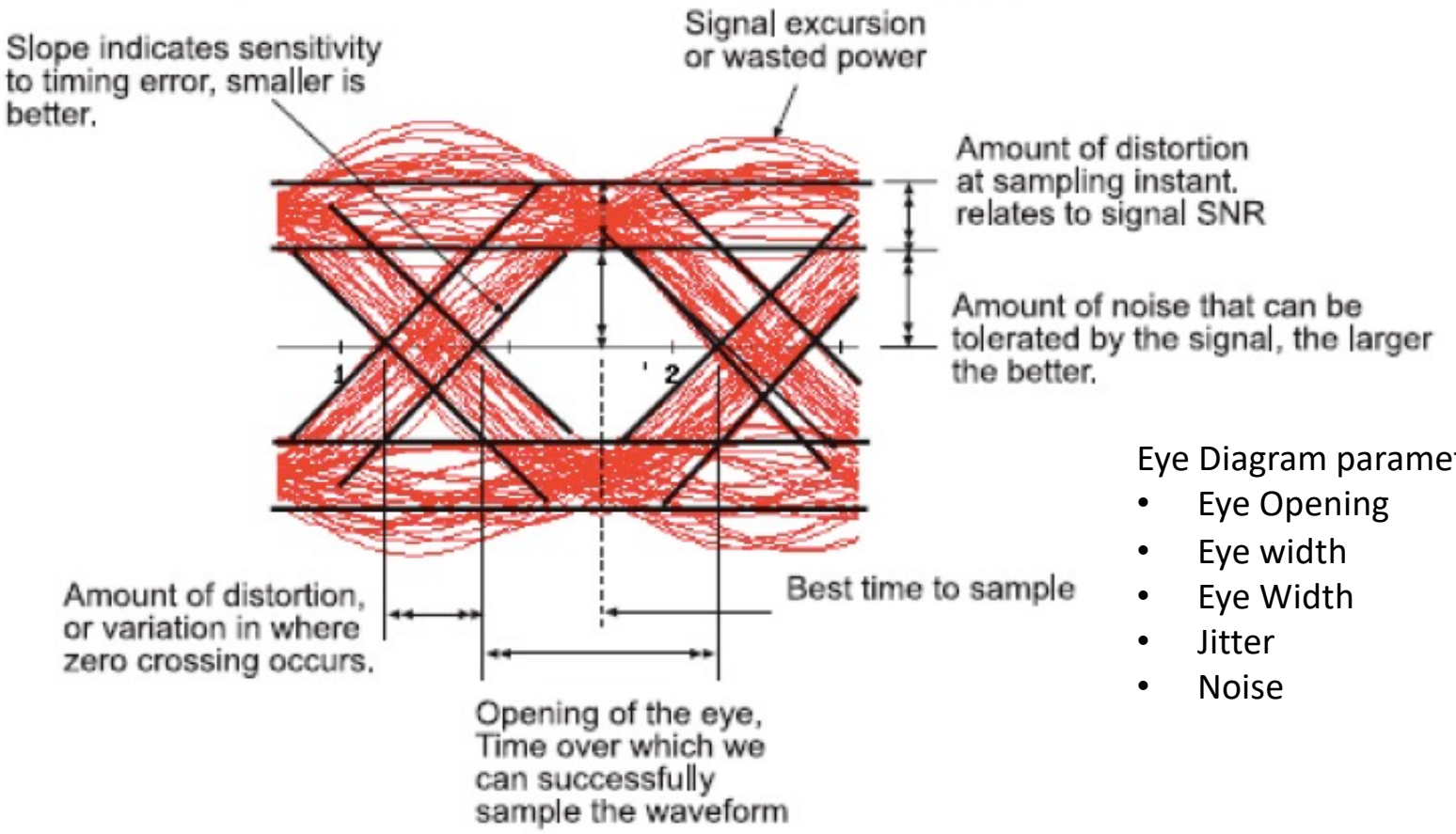
Typical data signal waveform:





An eye diagram maps a random bit sequence to a regular structure that can be used to analyze jitter.

Review: Eye Diagram



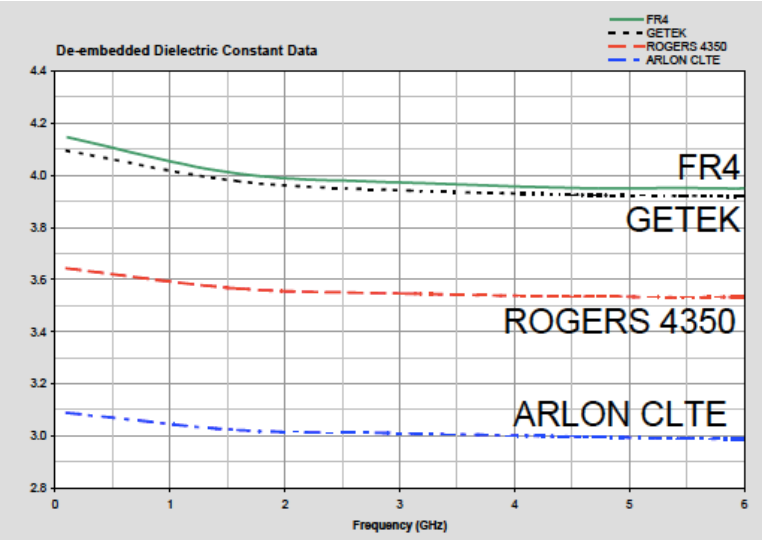
Eye Diagram parameters:

- Eye Opening
- Eye width
- Eye Width
- Jitter
- Noise

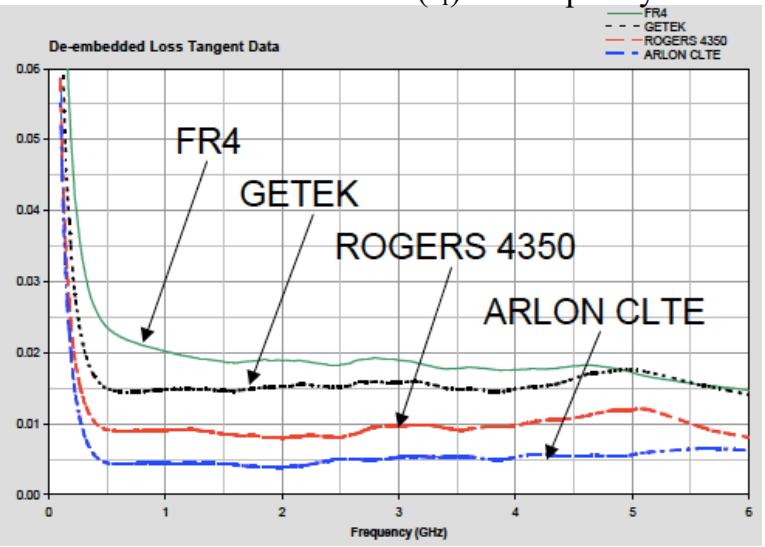
Material Review

Material	ε_{r}* @ 1 MHz	ε_{r}* @ 1 GHz	tanδ* @ 1 GHz	Relative Cost**
FR4	4.30	4.05	0.020	1
GETEK	4.15	4.00	0.015	1.1
ROGERS 4350/4320	3.75	3.60	0.009	2.1
ARLON CLTE	3.15	3.05	0.004	6.8

* Measured from test data
**Cost factor derived from 10" by 20", 12-layer backplane



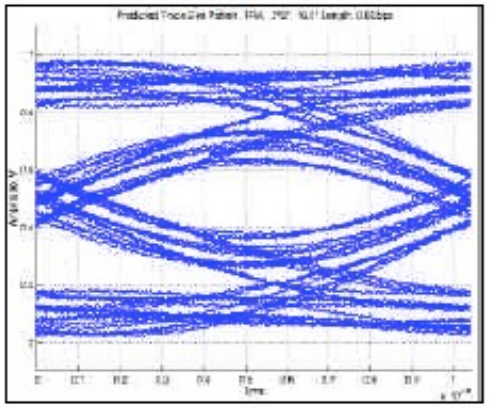
Dielectric constant (ε_r) vs. frequency



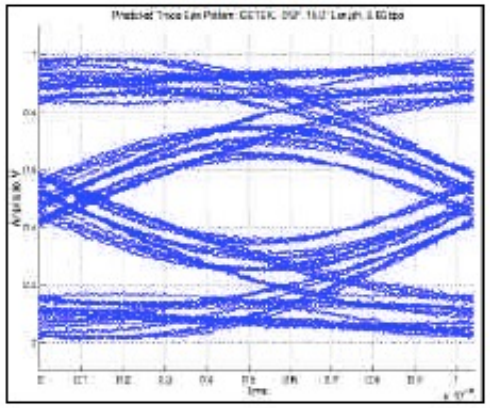
Loss tangent (tan δ) vs. frequency

Trace Eye Patterns (9.6Gbps, 18”)

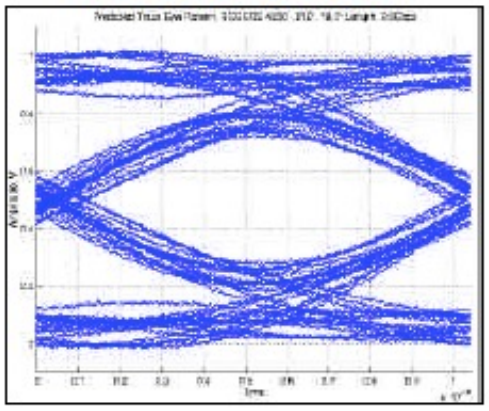
FR4



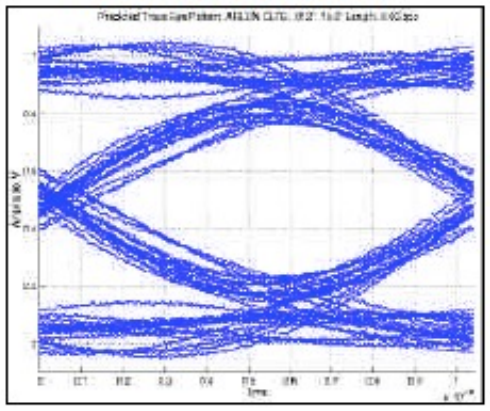
GETEK



ROGERS 4350



ARLON CLTE



FR4:
Jitter = 0.30 UI
Opening = 238 mV

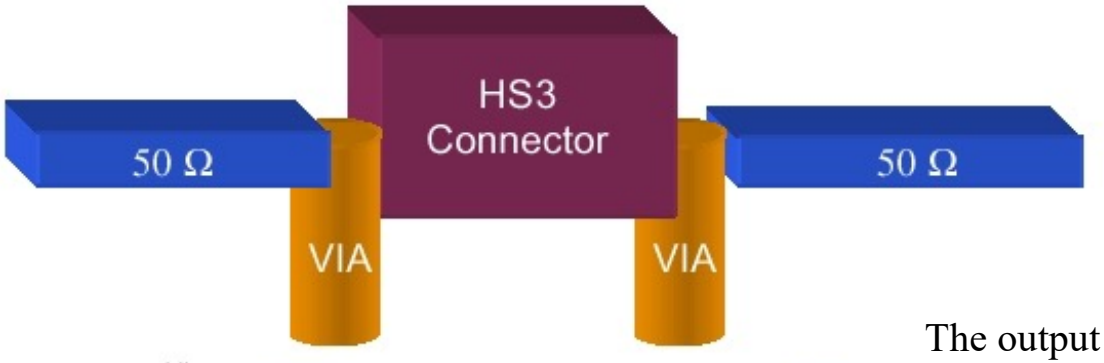
GETEK:
Jitter = 0.28 UI
Opening = 268 mV

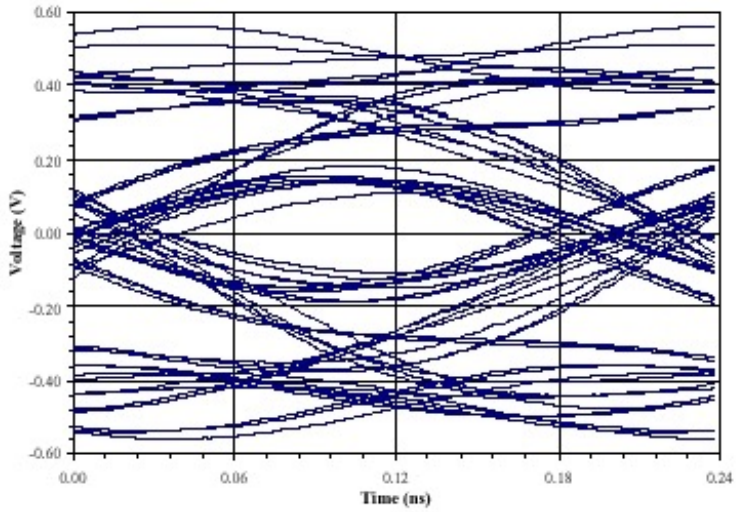
ROGERS 4350:
Jitter = 0.20 UI
Opening = 426 mV

ARLON CLTE:
Jitter = 0.19 UI
Opening = 520 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (9.6 Gbps, 60ps edges) that is applied to a 12 mil, 50 Ohm stripline trace that is 18" long.

Adding the Via



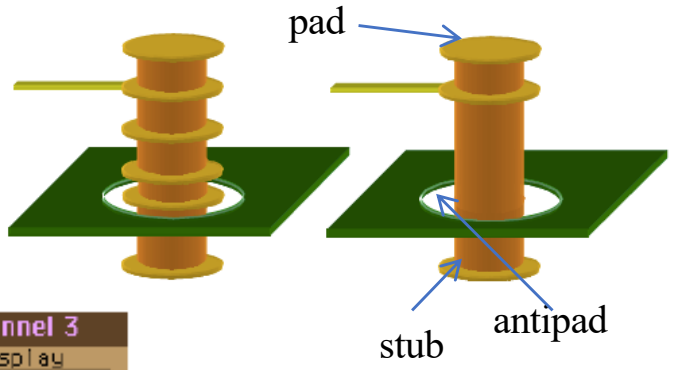


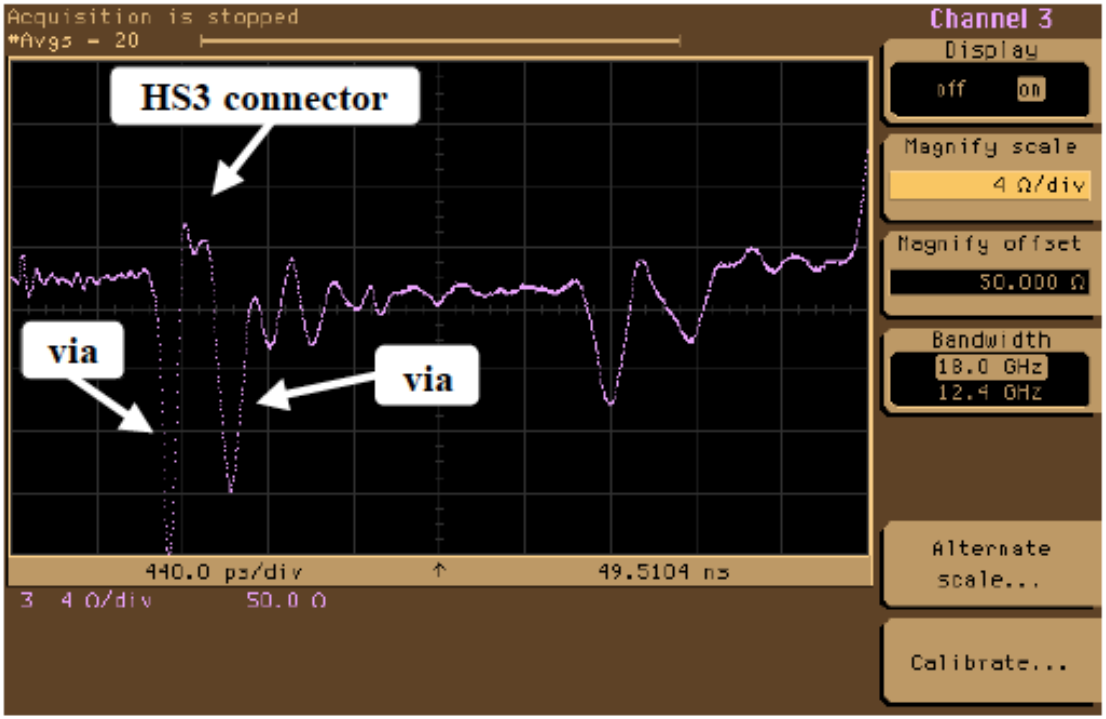
218 mV Opening, 34.4% Jitter

The output waveform shown results from a 1-volt, 32-bit inverting K28.5 input bit pattern (5 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12mil, 50 Ohm stripline trace that is ~18” long.

Challenge: The Via Culprit

- Vias introduce capacitive discontinuities
- Connector and traces are about 50 Ω



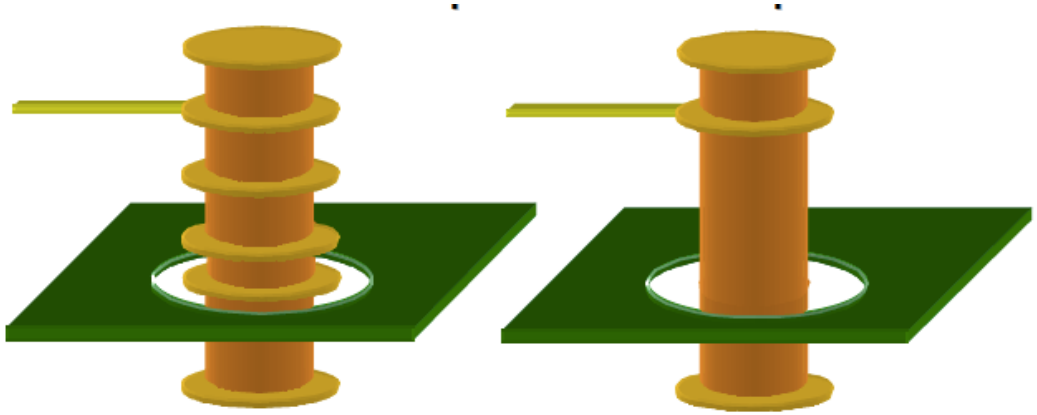


Test parameters

- All traces 12 mils
- 6" backplane trace (ROGERS 4350 dielectric)
- 3" daughtercard traces (FR4 dielectric)
- HS3 6 row connectors

Remove Non-Functional Pads

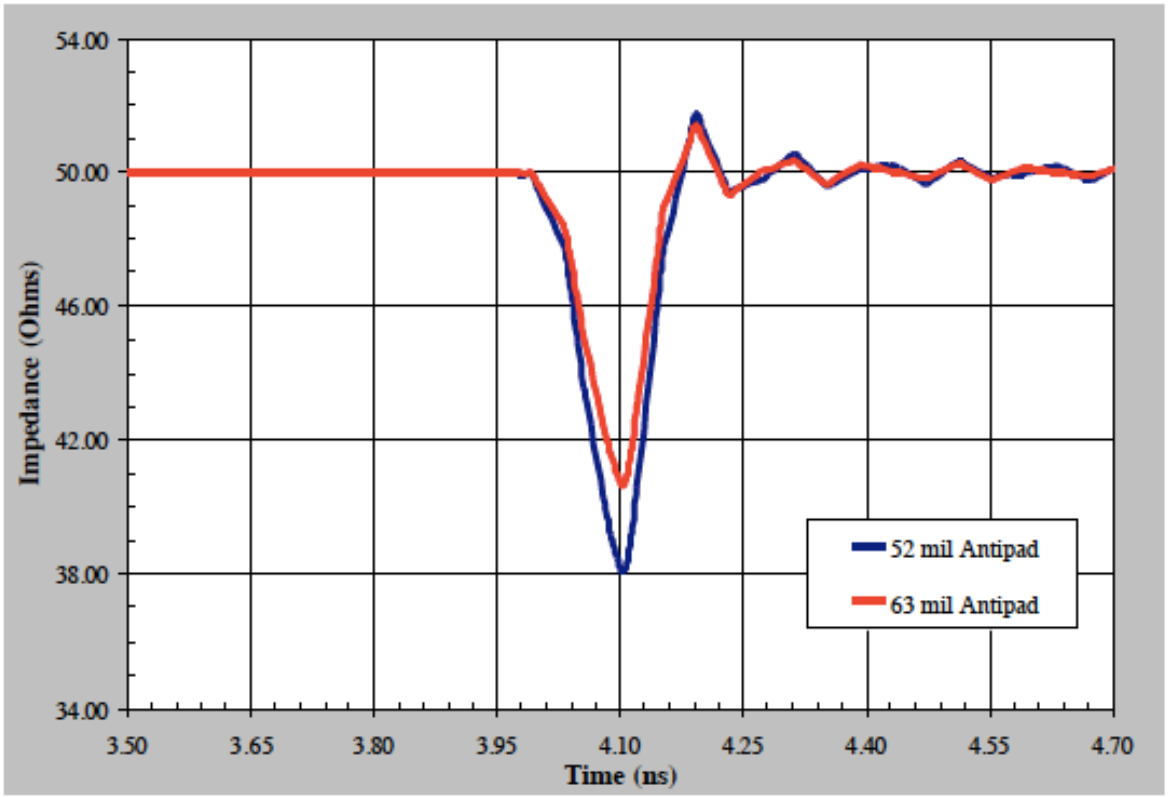
- Non-functional pads are not necessary
  - Surface pads required
  - Keep internal pad for trace connection
- Removal can improve via capacitance



pads kept pads removed

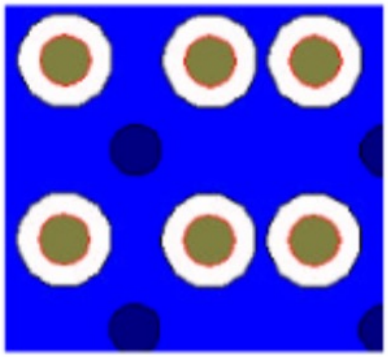
Antipad Capacitance Effect

- Capacitance of via decreases as antipad grows

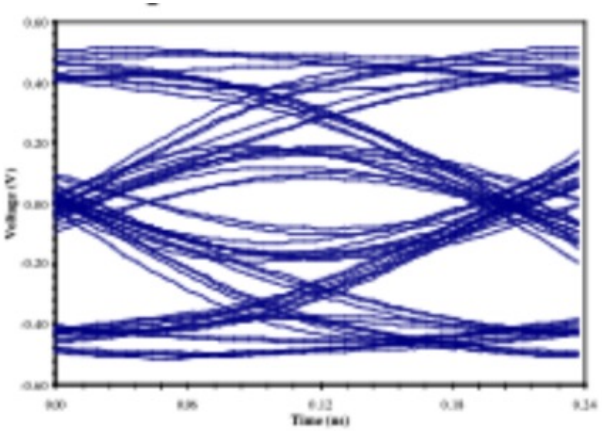


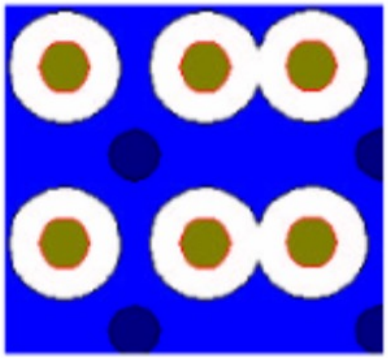
Simulation parameters
•HS3 pinfield
•Via only (no connector)
•60 ps edge

Antipad Capacitance Effect

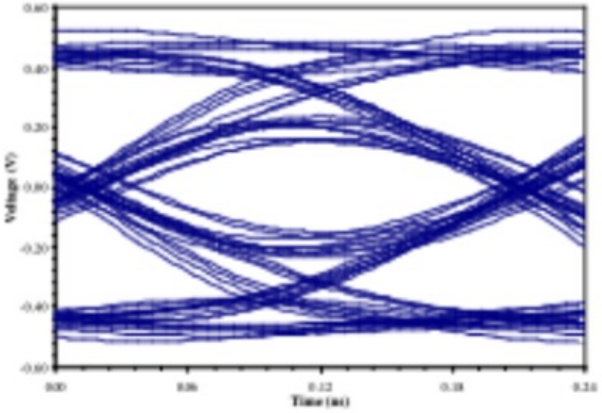


- 52 mil antipad diameter
- 166.1 mV opening
- 25% jitter





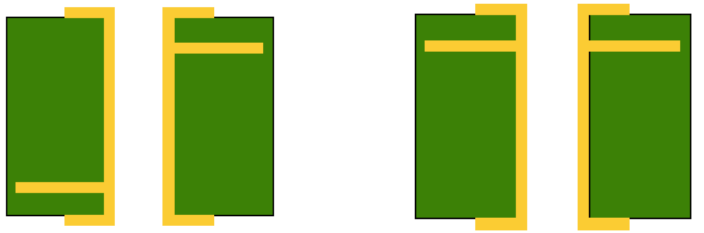
- 63 mil antipad diameter
- 301.6 mV opening
- 18.75% jitter



Simulation parameters: 5Gbps signal, K28.5 pattern, Backplane: 12” ROGERS 4350 (200 mil thick), Daughtercard: 3” FR4 (100 mil thick), HS3 6 row connectors

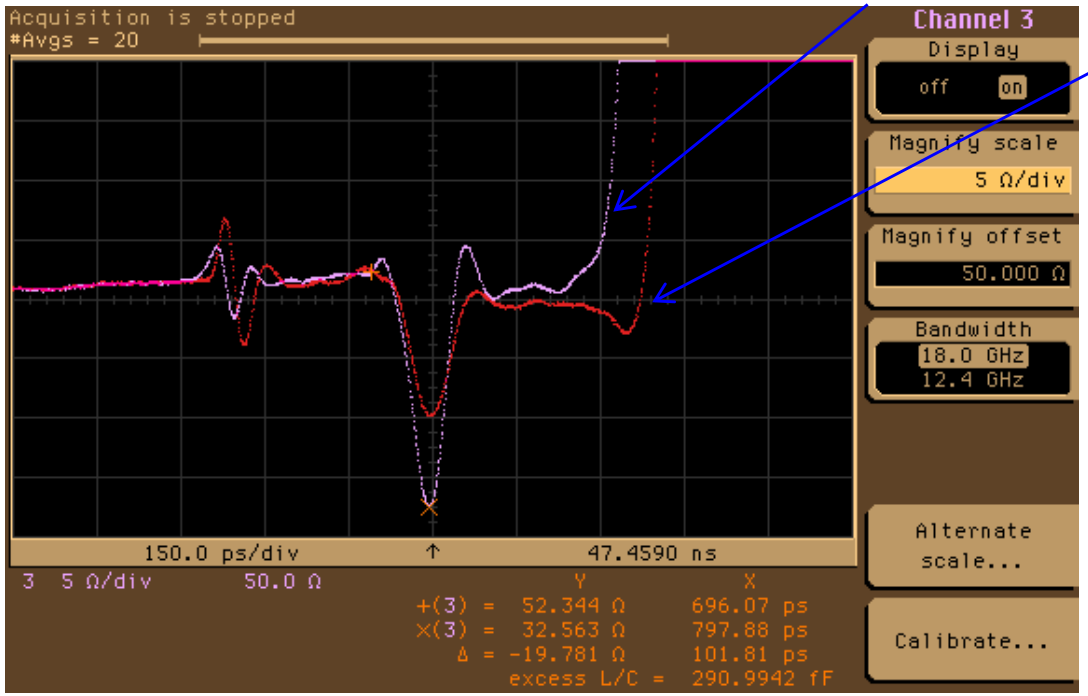
Stub Via Performance

- Layer Attachment Location



Transmitting through the via

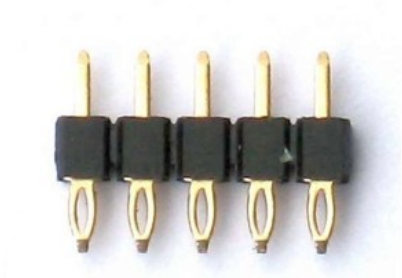
Transmitting across the via



Test parameters
- HS3 pinfield
- Optimized antipad
- Via only (no connector)

Transmitting across the via introduces the largest discontinuity

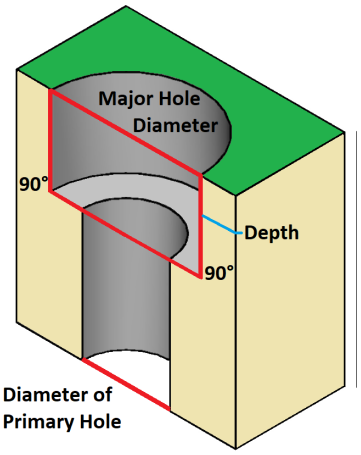
Stub Removal Techniques - to eliminate the stub capacitance



5-pin press-fit header strip

Blind vias

Counterbore



- **Pros**
  - Via stub is completely removed
- **Cons**
  - Can double fabrication cost of bare board
  - May not support pin-in-hole soldering techniques

- **Pros**
  - Via stub is almost completely removed
- **Cons**
  - Can add 25% to bare board fabrication cost

Counterbore Performance

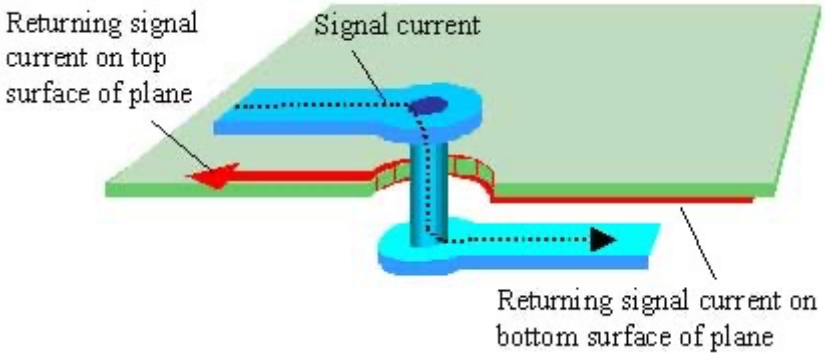
Transmitting across the counterbore via now introduces almost no discontinuity

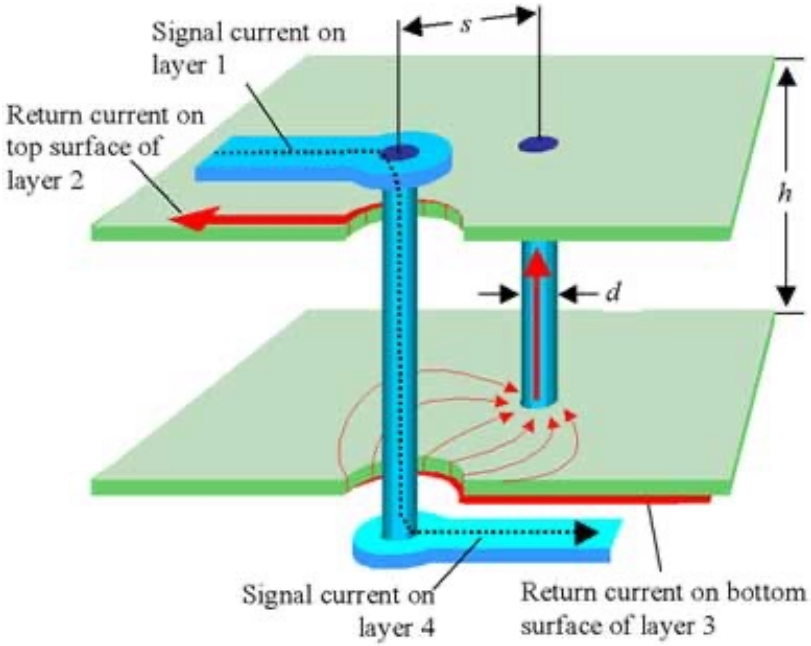
Test parameters
- HS3 pinfield
- Optimized antipad
- Via only (no connector)

Via Design Technique Summary

- Remove unused pads
- Antipad size
  - Decreases excess capacitance
  - No added cost
  - Limited by trace routing considerations
- Stub removal
  - Significantly decreases excess capacitance
  - At least two techniques can be used
  - Adds additional costs

3.8 Example II: Transmission line on non-ideal GND

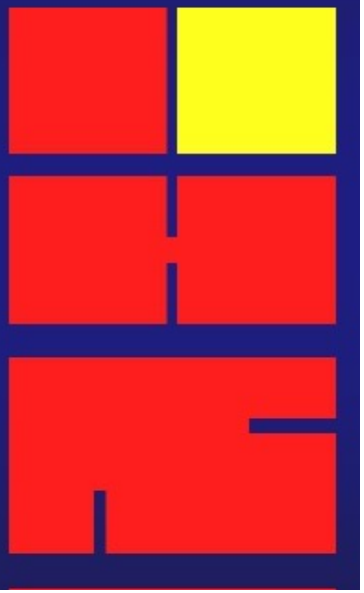




3.8 Example II: Transmission line on non-ideal GND

Reasons for splits or slits on GND planes

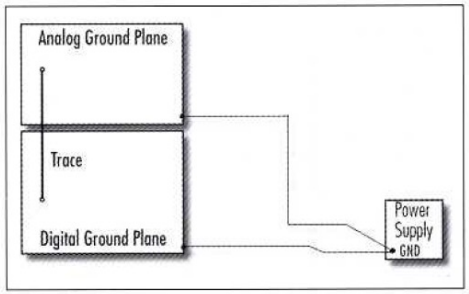
- DC isolation between different supply voltages.
- AC isolation of digital from low noise analog circuits.
- Low cost method of removing unwanted resonances from the power distribution system.



Example II: Transmission line on non-ideal GND

Disadvantages of Image Plane Slits and Splits

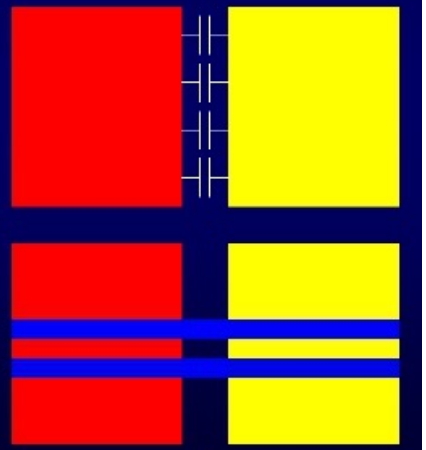
- Transverse slits in the image planes present a discontinuity to the flow of AC currents.
- Result in significant signal degradation.
- Help generate common mode currents that result in significant radiation.



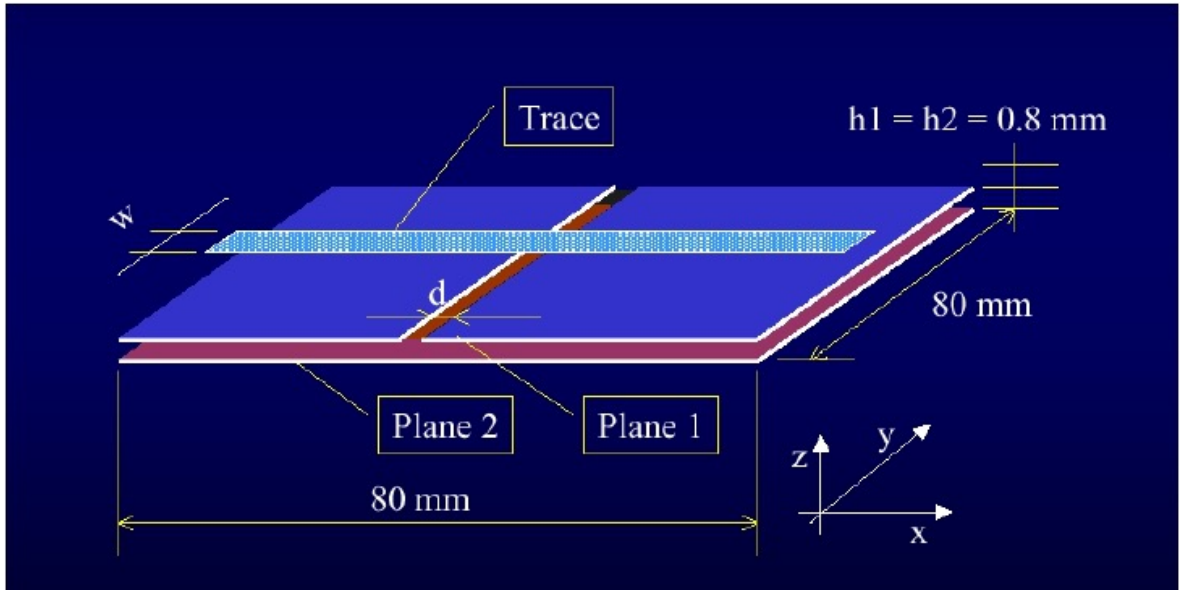
Example II: Transmission line on non-ideal GND

Two most commonly used:

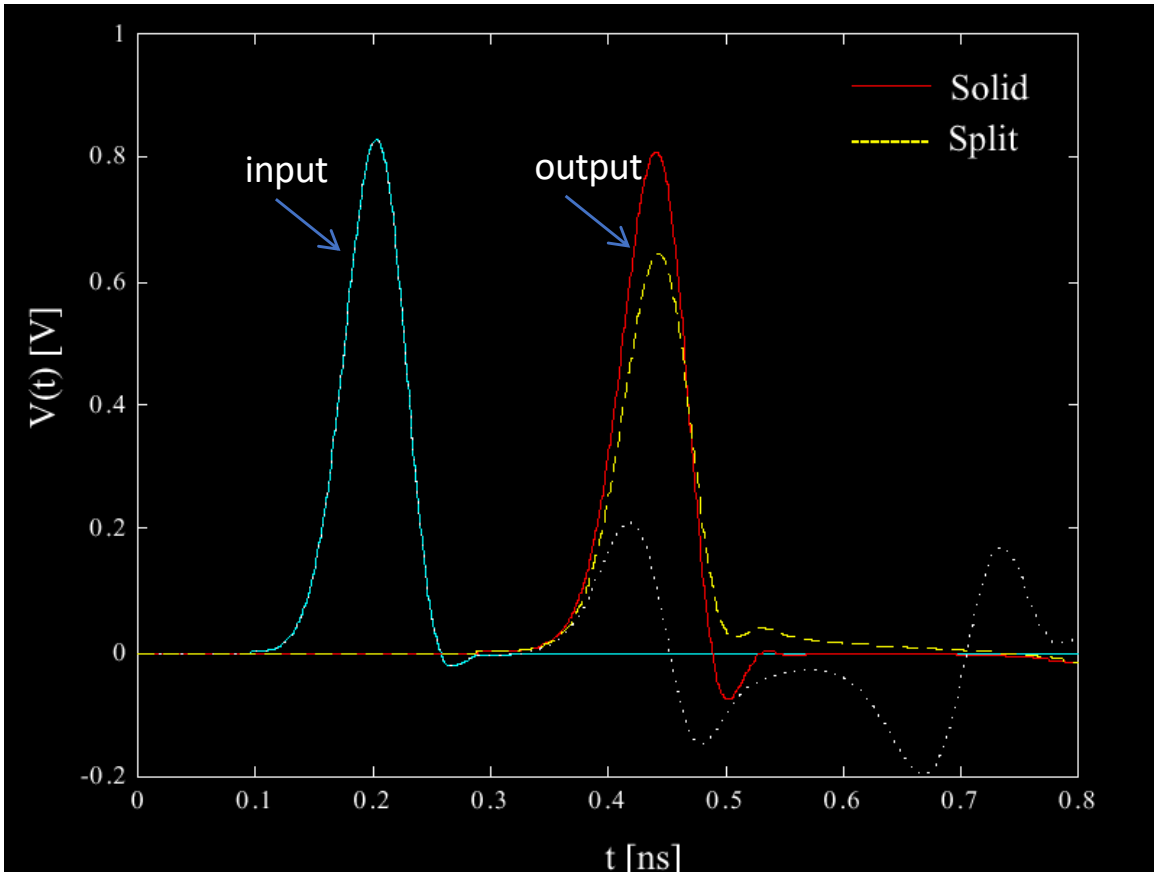
- AC shorting (stitching) the two separated planes with capacitors.
- Using differential lines to cross the split.



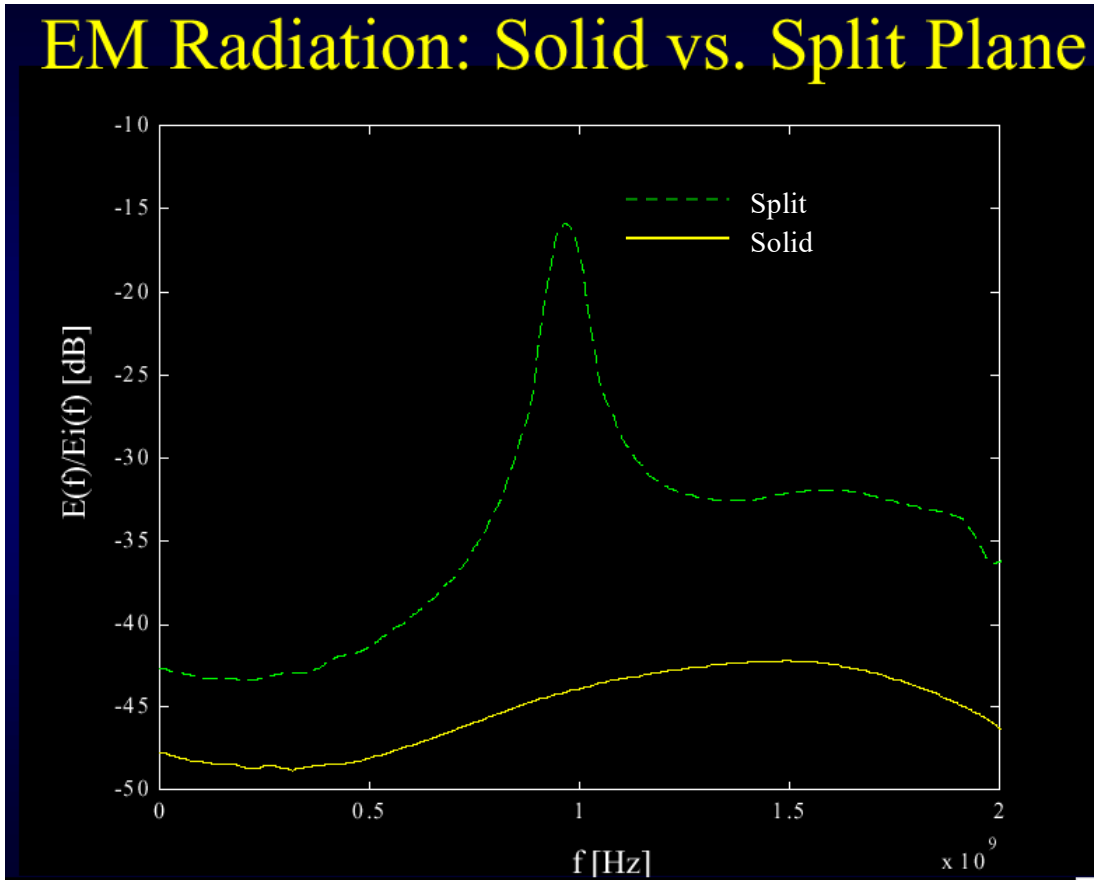
Example II: Transmission line on non-ideal GND



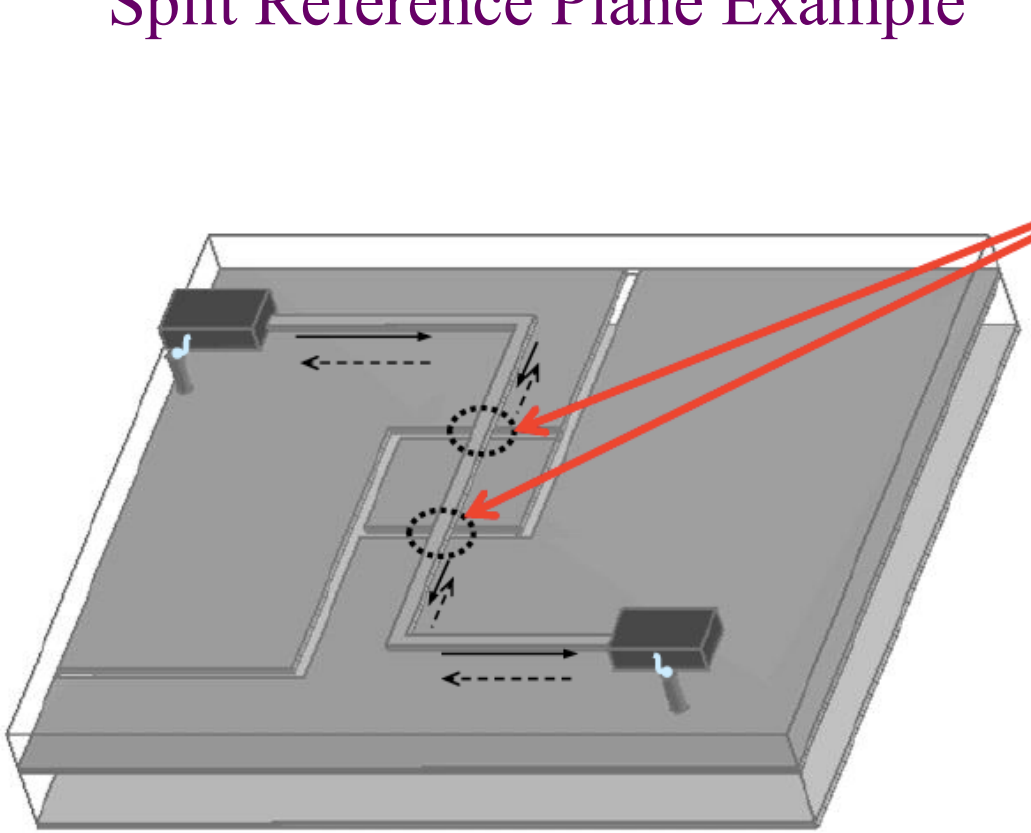
Example II: Transmission line on non-ideal GND

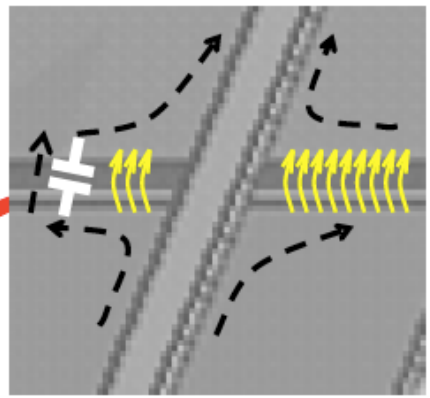


Example II: Transmission line on non-ideal GND



Split Reference Plane Example





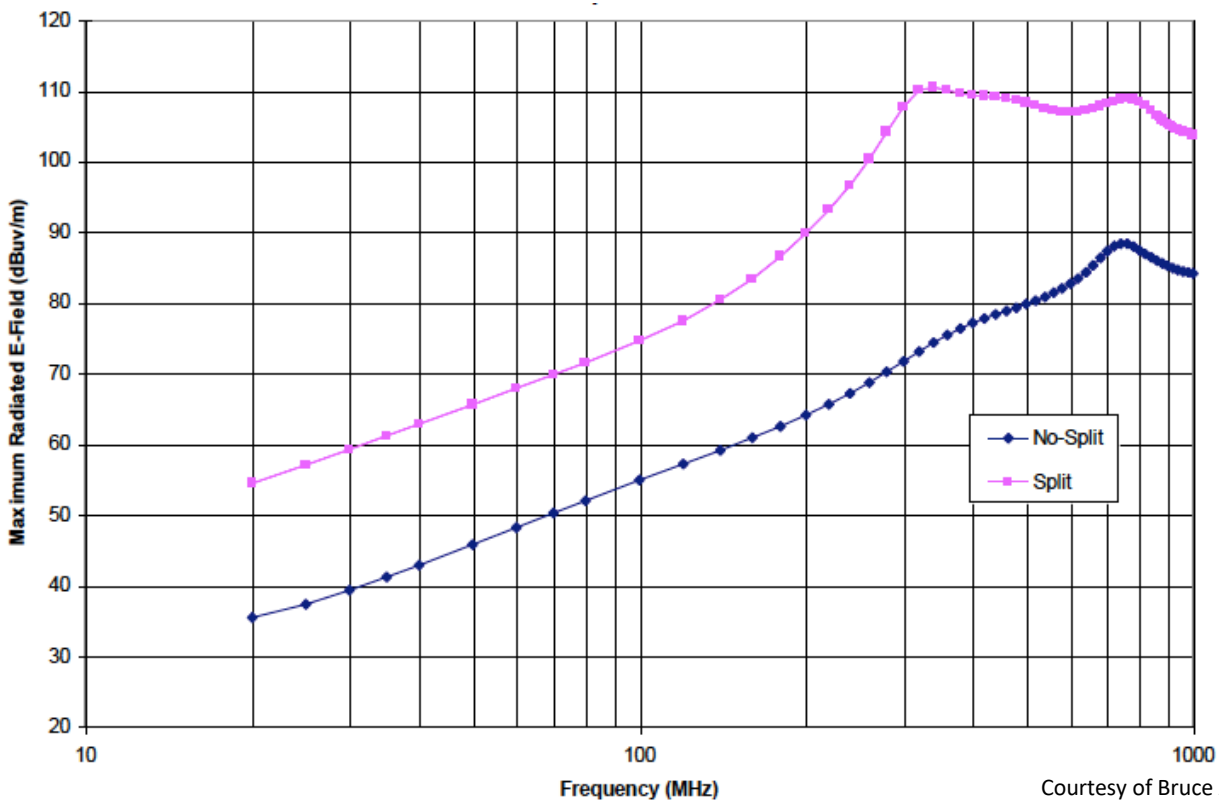
Stitching capacitors allow return currents to cross split

???

Really?

Near Field Radiation from Microstrip on Board with Split in Reference Plane

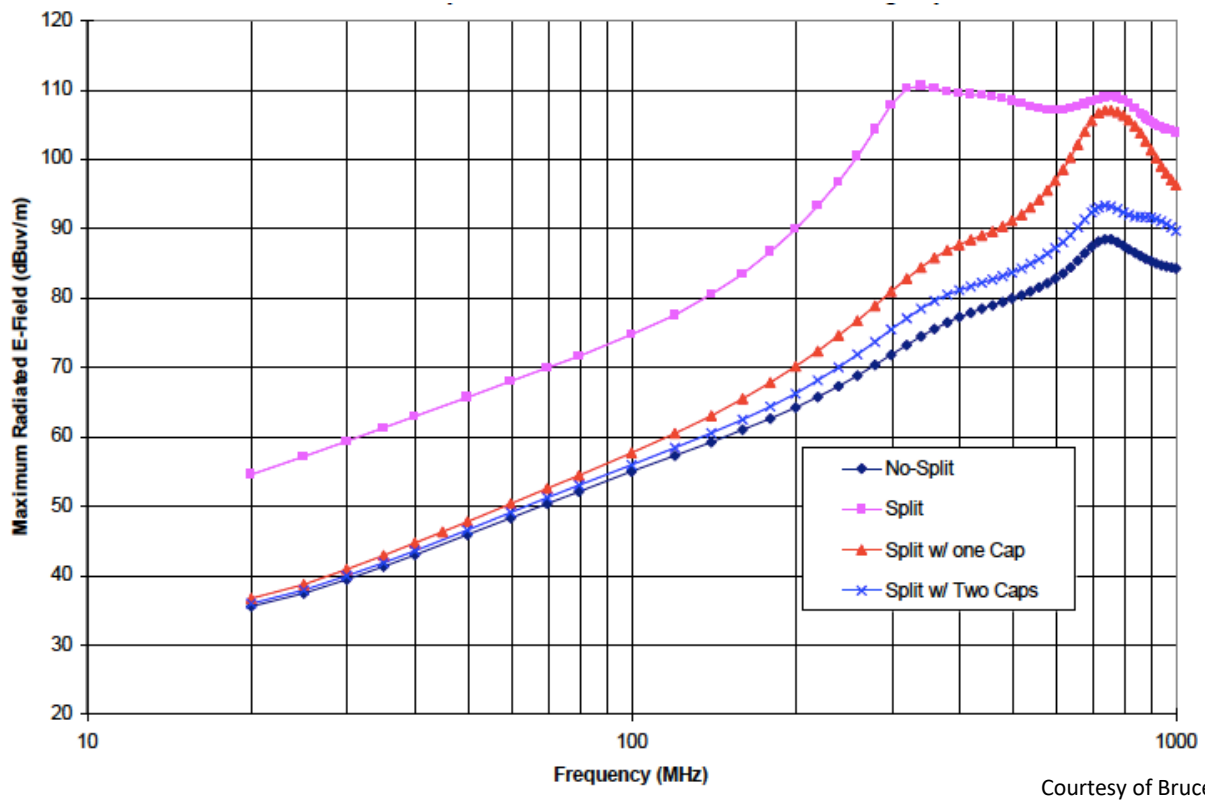
Comparison of Maximum Radiated E-Field for Microstrip with and without Split Ground Reference Plane



Courtesy of Bruce Archambeault

With "Perfect" Stitching Capacitors Across Split

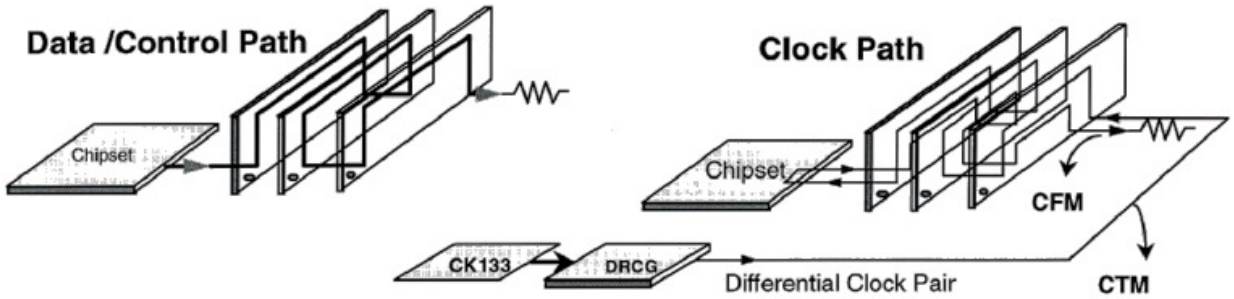
Comparison of Maximum Radiated E-Field for Microstrip with and without Split Ground Reference Plane

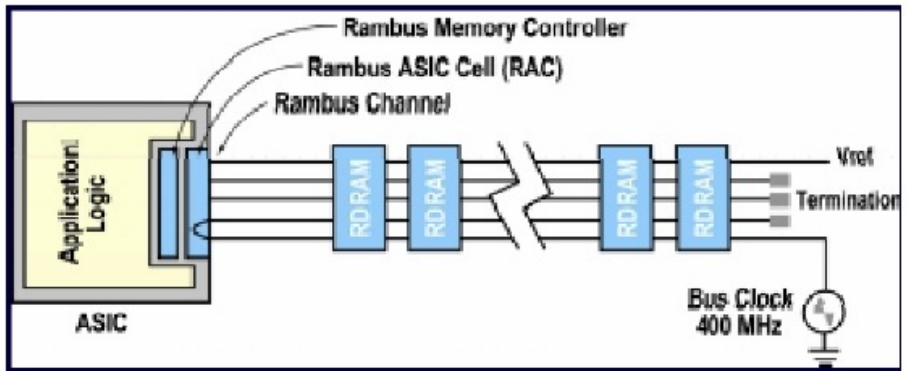


Courtesy of Bruce Archambeault

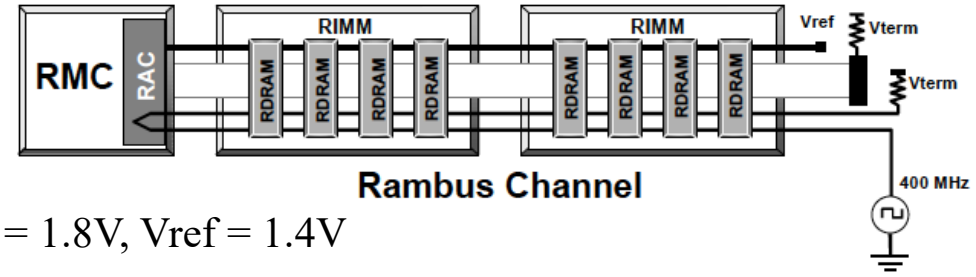
3.9 Example III: Rambus RDRAM and RIMM Design

RDRAM Signal Routing





Example III: Rambus RDRAM and RIMM Design



- Power:

  VDD = 2.5V, Vterm = 1.8V, Vref = 1.4V

- Signal:

  0.8V Swing: Logic 0 -> 1.8V, Logic 1 -> 1.0V
  2x400MHz CLK: 1.25ns timing window, 200ps rise/fall time
  Timing Skew: only allow 100ps - 150ps

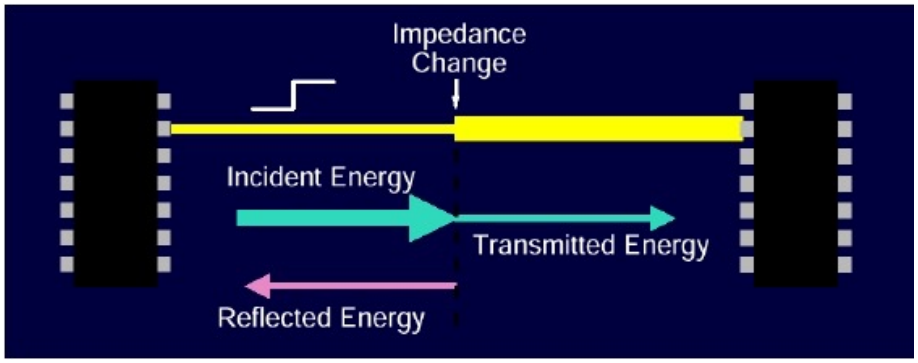
- Rambus channel architecture:

  (30 controlled impedance and matched transmission lines)

  - Two 9-bit data buses
  - A 3-bit ROW bus
  - A 5-bit COL bus
  - CTM and CFM differential clock buses

Example III: Rambus RDRAM and RIMM Design

- RDRAM Channel is designed for 28 Ω +/- 10%
- Impedance mismatch causes signal reflections
- Reflections reduce voltage and timing margins
- PCB process variation -> Z_0 variation -> Channel error
- AC Timings are tight!
  - 2X clock @ 400MHz Operation = 1.25ns window
  - Only 100 - 150 ps allowed for total channel timing error

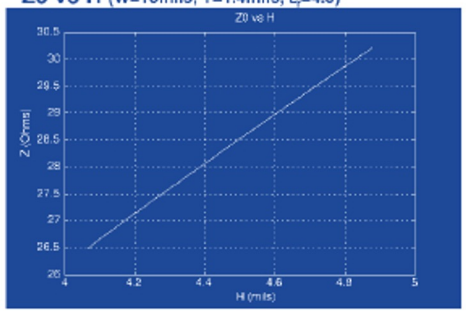


Example III: Rambus RDRAM and RIMM Design

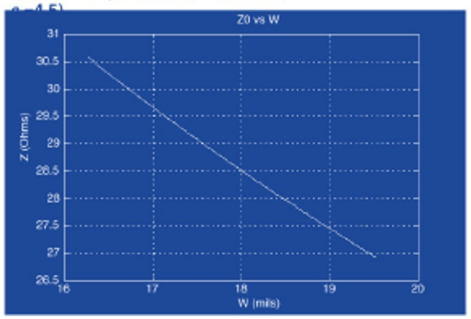
PCB Parameter sensitivity:

- H tolerance is hardest to control
- T have less impact on Z_0 due to wider trace

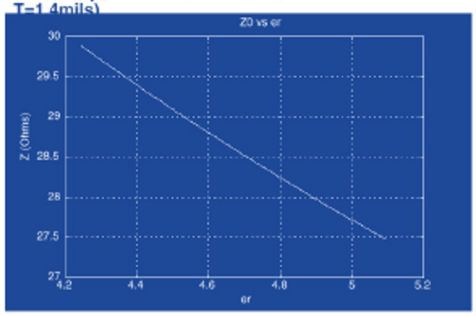
Z0 vs H (W=18mils, T=1.4mils, ε_r=4.5)



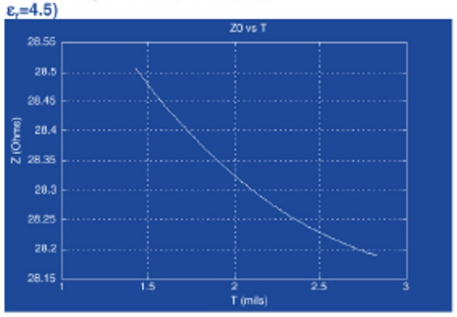
Z0 vs W (H=4.5mils, T=1.4mils,

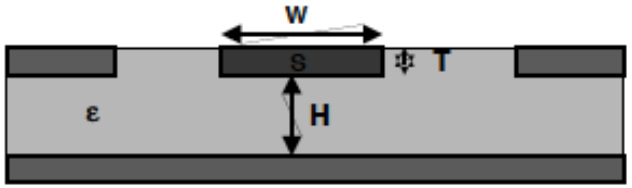


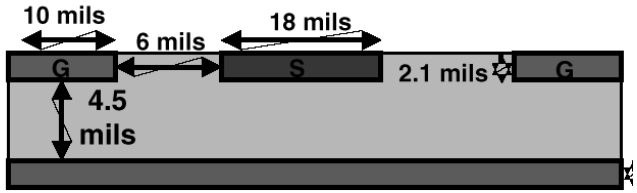
Z0 vs ε_r (H=4.5mils, W=18mils, T=1.4mils)



Z0 vs T (H=4.5mils, W=18mils, ε_r=4.5)



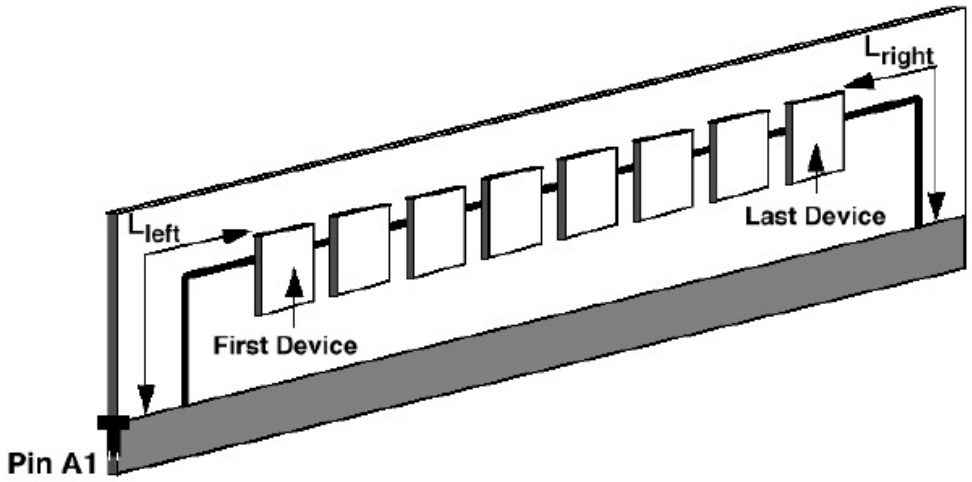




Intel suggested coplanar structure

Example III: Rambus RDRAM and RIMM Design

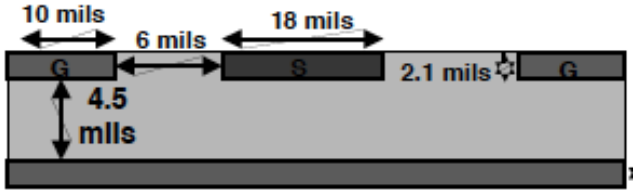
- How to design Rambus channel in RIMM Module with uniform Z_0 = 28 ohm ??
- How to design Rambus channel in RIMM Module with propagation delay variation in +/- 20ps ??



Example III: Rambus RDRAM and RIMM Design

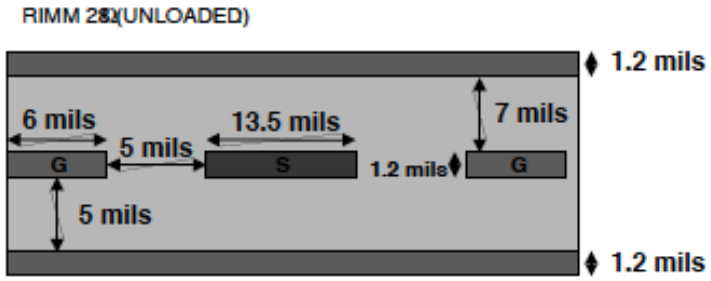
Recommended Stackup

Outer Layer Routing



W=18mil, H=4.5mil, T=2.1mil, 1 ply 2116 prepreg

Inner Layer Routing



W=13.5mil, H1=7mil, H2=5mil, T=1.2mil

Example III: Rambus RDRAM and RIMM Design

Impedance Control:

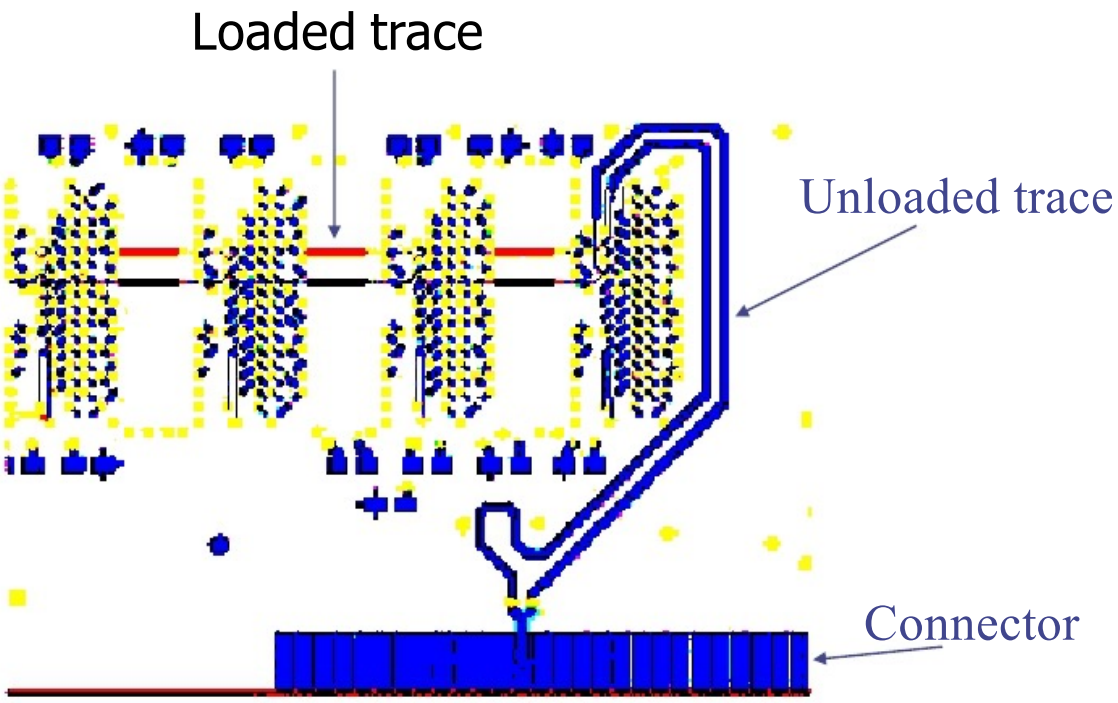
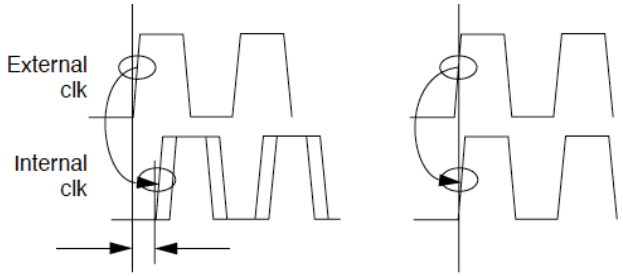


Figure 5-12: High-Speed CMOS Signal Routing

Example III: Rambus RDRAM and RIMM Design

- Controlling propagation delay:
  - Bend compensation
  - Via Compensation
  - Connector compensation



Uncompensated vs compensated clocks.

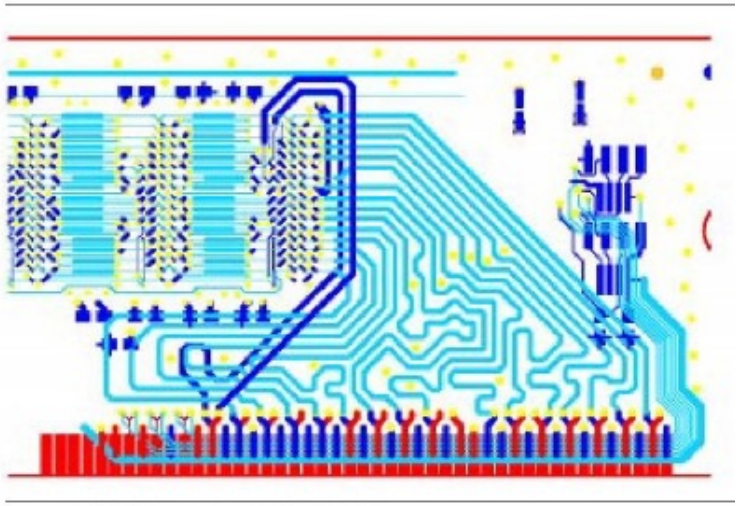


Figure 5-11: Delay Matching (Right Side)

Bend Compensation

Rule of thumb: 0.3ps delay of every bend

Solving strategies:

1. Using same numbers of bends for those critical traces(difficult)
2. Compensate each bend by a 0.3ps delay line.

Example III: Rambus RDRAM and RIMM Design

Via Compensation (delay)

For an 8 layers PCB, a via with 50mil length can be modeled as (L, C) = (0.485**nH**, 0.385**pF**).

so Delay $T_0 = \sqrt{LC} = 13.7$ psec

Impedance $Z_0 = \sqrt{\frac{L}{C}} = 38\Omega$

$$C_{via} \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1} \quad *$$

$$L_{via} \approx 0.58h\left[\ln\left(\frac{4h}{d}\right)+1\right] \quad *$$

Rule of thumb: delay of a specific via depth can be calculated by scaling the inductance value which is proportional to via length.

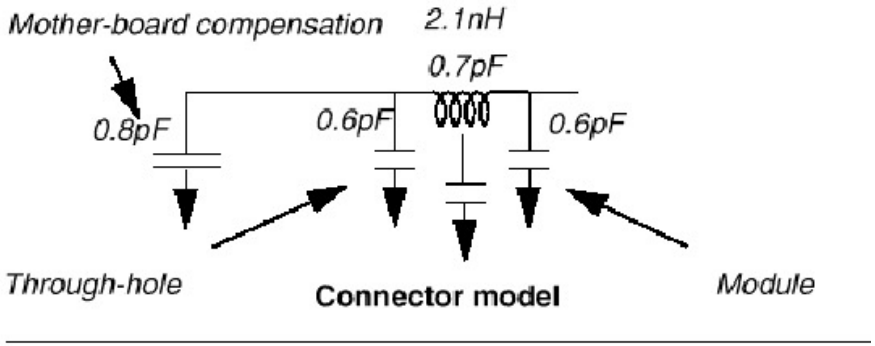
so 30mil via has delay = $13.7 \times \sqrt{\frac{30\text{mil}}{50\text{mil}}} = 10.6p\text{sec}$

This delay difference can be compensated by adding a 1.566mm to the unloaded trace (56 Ω)

* Johnson and Graham, 1993

Example III: Rambus RDRAM and RIMM Design

Connector Compensation



$C_{pin} = 0.7\ pF, C_{via} = 0.6\ pF, C_{pad} = 0.6\ pF, C_{mb} = 0.8\ pF \Rightarrow C_{total} = 2.7pF$

$L_{pin} = 2.1\ nH$

$Z = \sqrt{L_{pin} / C_{total}} = 27.9\Omega$