

## Lab 6. Voltage-Controlled Oscillator

In this lab exercise, we will construct a voltage-controlled oscillator with surface-mounted components on a PCB which was laid out for that purpose. We will then measure the VCO, characterize its performance across its tuning range, and compare it to the Xtal oscillator.

### Active Buffer Design

In order to drive a low-impedance load such as  $50\ \Omega$ , we need to add an impedance matching device that converts the low impedance load to a high impedance that the oscillator can drive. We could use a simple L-net to transform the load impedance, but this would only work for one frequency and not as suitable for tuning the frequency of oscillation. For this reason, we will use another CC amplifier, acting as a broadband active impedance match or buffer. As you may recall, a CC amplifier has high input impedance and relatively low output impedance. Thus, we can drive a  $50\ \Omega$  load with the addition of this buffer stage, as shown in Figure 5.1.

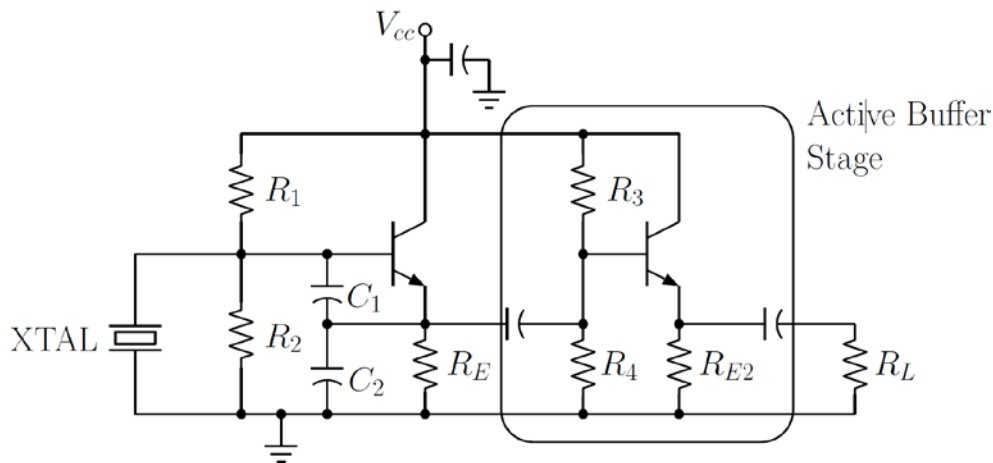


Figure 5.1: XTAL oscillator with active buffer

### Biasing the emitter follower buffer stage

Consider the DC and AC load lines for an emitter follower, as shown in Figure 5.2

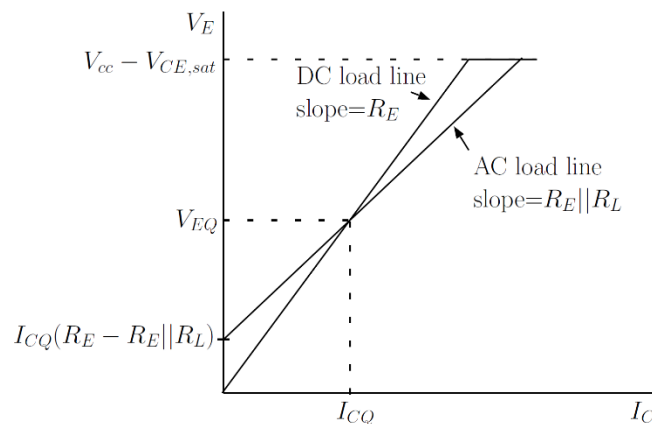


Figure 5.2: DC and AC load lines for the emitter follower amplifier

The emitter voltage is plotted against the collector current,  $I_C$ , which is assumed to be approximately equal to the emitter current. When the circuit is excited with a time-varying input signal, or when the circuit is oscillating, the instantaneous emitter voltage and current will be related by the AC load line.

Notice that the instantaneous emitter voltage can swing between a minimum value  $V_{E,min} = I_{CQ}(R_E - R_E || R_L)$  and a maximum value  $V_{E,max} = V_{CC} - V_{CE,sat}$ . Typically, the collector-emitter saturation voltage is taken to  $V_{CE} \approx 0.1V$  so that  $V_{E,max} = V_{CC} - 0.1V$ . At the upper limit, the emitter voltage is limited at  $V_{CC} - 0.1V$ . due to transistor saturation. At the lower limit,  $V_{E,min}$  corresponds to transistor cutoff, since the corresponding instantaneous collector current is zero. For the minimum and maximum emitter voltage swings to be symmetrical around the quiescent point, we require:

$$V_{CC} - 0.1 - V_{EQ} = V_{EQ} - I_{CQ}(R_E - R_E || R_L)$$

Using  $I_{CQ} \approx V_{EQ}/R_E$  and solving for  $V_{EQ}$  yields an expression for the quiescent emitter voltage under conditions of maximum symmetrical emitter voltage swing:

$$V_{EQ,ss} = (V_{CC} - 0.1) \frac{R_E + R_L}{R_E + 2R_L}$$

When the transistor is biased at this quiescent point, the maximum undistorted zero-to-peak voltage swing across the load will be:

$$V_{0-p,ss} = (V_{CC} - 0.1) \frac{R_L}{R_E + 2R_L}$$

If  $V_{EQ}$  is less than  $V_{EQ,ss}$  then the output voltage swing will be limited on negative excursions by transistor cutoff. In this case, the maximum undistorted 0-peak swing will be

$$V_{0-p} = V_{CC} \frac{R_L}{R_E + R_L}$$

If  $V_{EQ}$  is greater than  $V_{EQ,ss}$  then the output voltage swing will be limited on positive excursions by transistor cutoff. In this case, the maximum undistorted 0-peak swing will be

$$V_{0-p} = V_{CC} - 0.1 - V_{EQ}$$

The power dissipation limits of the transistor and the emitter resistor must be considered as well. The DC power dissipated in the transistor is  $\approx (V_{CC} - V_{EQ})I_{EQ}$ . The power dissipated in the emitter resistor will be the sum of the DC power ( $V_{EQ}I_{EQ}$ ) and the AC power, which depends on the drive level.

To save you some time, we will tell you that your best bet is to choose an emitter resistor  $R_E \approx 300 \Omega$  and a quiescent emitter current  $I_{EQ} \approx 20 mA$ . This means that  $V_{EQ} \approx 6V$ . With these values, and assuming  $V_{CC} = 12 V$ , the value of  $V_{EQ,ss} = 10.4 V$ . Since  $V_{EQ} < V_{EQ,ss}$ , the output voltage swing will be limited on negative excursions by transistor cutoff. The maximum undistorted 0-peak emitter voltage swing will be 0.86 V. This is also the 0-peak voltage across the load, so the maximum output power without significant waveform distortion will be  $0.86^2 / (2 * 50) = 7.4mW$ , adequate to drive the mixer.

With  $V_{EQ} = 6V$ , the DC power dissipated in the transistor will be approximately  $5.9 V * 0.02 A = 118 mW$ , which is within the maximum dissipation limit (200 mW) of a 2N5179 transistor. The DC power dissipated in the emitter resistor will be approximately  $6 V * 0.02 A = 120 mW$ , also within the dissipation limits of a 1/4 Watt resistor. If you decide to choose a different quiescent point, be sure to check the power dissipated in the transistor and in the emitter resistor. You may obtain larger output voltage swing, and smaller power dissipated in the transistor by raising  $V_{EQ}$ . On the other hand, power dissipated in the

emitter resistor will increase if  $V_{EQ}$  is raised, in which case it may become necessary to use something larger than a 1/4 Watt resistor for  $R_E$ .

Choose value for  $R_3$  and  $R_4$  that set the bias point to the desired value. Note that  $R_E = R_3 \parallel R_4$  will have to be significantly smaller here than it was for the oscillator stage. With  $R_E = 300 \Omega$  and  $\beta_{min} = 25$ , we need to keep  $R_B$  much smaller than 7.8 k $\Omega$ .

To avoid significant output waveform distortion you will need to make sure that the buffer amplifier is not overdriven by the oscillator. If your oscillator output is too high, two ways to decrease the drive level to the buffer amp are (i) decrease the loop gain of the oscillator to decrease the steady-state oscillation amplitude. This can be done by inserting a resistance in series with the  $C_1 - C_2$  junction and the emitter of the transistor; or (ii) use an attenuator in between the oscillator and the emitter follower. A simple resistive L network (voltage divider network) will suffice. Design the network so that the impedance presented to the oscillator is high and the impedance presented to the emitter follower is (relatively) low. This means that the series arm of the resistive L-net connects to the oscillator, and the shunt arm connects to the emitter follower.

## Voltage-Controlled Oscillator Design

The VCO will be constructed by replacing the crystal with an LC tank in which a varactor diode serves as a tunable capacitor, as shown in Figure 5.3.

### Varactor

The varactor is a variable capacitor derived from the junction capacitance of a reverse-biased diode. As the tuning voltage increases, the varactor is increasingly reverse-biased, leading to a larger depletion region and thus a smaller capacitance. This gives us control over the frequency of oscillation. Notice that, in our design, we use two varactor diodes back-to-back, to simplify biasing. The two back-to-back varactors help to ensure that neither varactor diode is driven into forward bias. With the dual-diode scheme, half the tank voltage appears across each diode. If the voltage swing is large enough to drive a diode into conduction, the other diode will be strongly reverse biased. So the impedance across the tank will always be high. If only a single diode was used, then when the diode is driven into conduction, the low diode impedance would appear across the tank circuit, and will quickly drain the energy from the tank, dramatically reducing the effective Q of the tank.

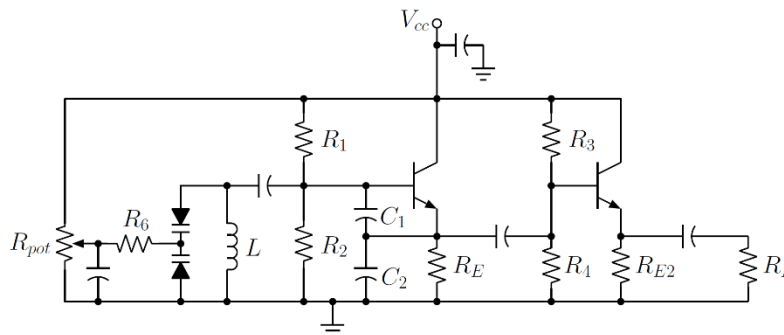
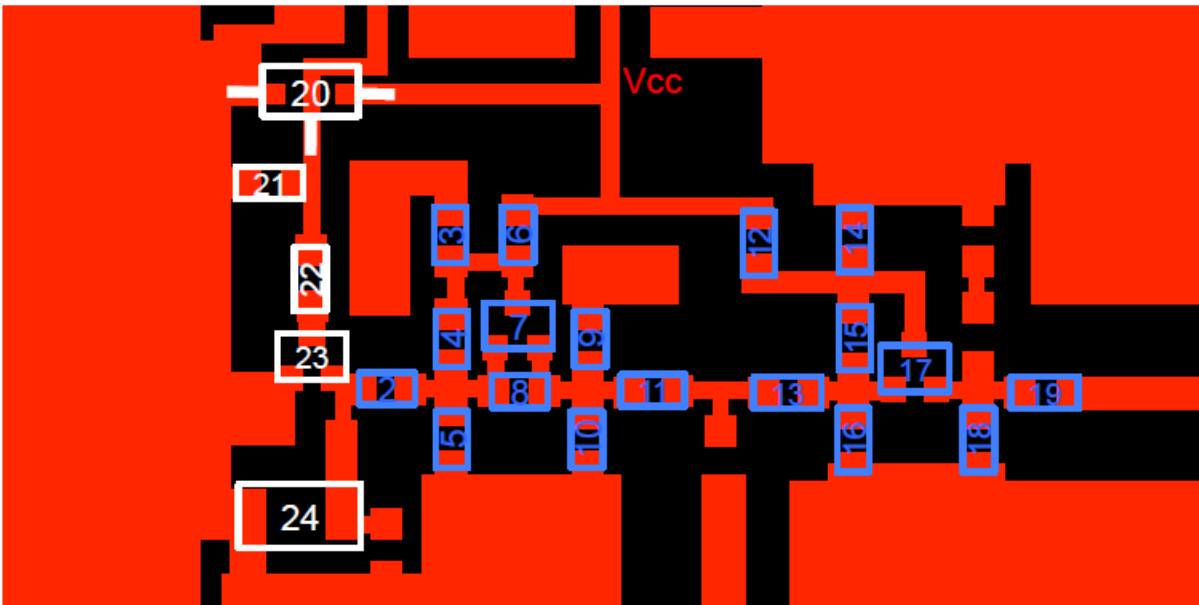


Figure 5.3: Voltage-controlled oscillator with tuning potentiometer

## VCO Construction Guideline



- 2 – Coupling capacitor
- 3 – Bypass capacitor
- 4 – R1
- 5 – R2
- 6 – Rv
- 7 – npn BJT
- 8 – C1
- 9 – C2
- 10 – Re
- 11 – Coupling capacitor
- 12 – Rv
- 13 – Coupling capacitor
- 14 – Bypass capacitor
- 15 – R3
- 16 – R4
- 17 – npn BJT
- 18 – Re2
- 19 – Coupling capacitor
- 20 – Potentiometer
- 21 – Bypass capacitor
- 22 – R6
- 23 – varactor
- 24 – Air core inductor

## Measurements for Oscillator Characterization

- Tune the VCO to 100 MHz
- Measure the output power (in dBm) and frequency of the fundamental harmonic. Compare this to what you observed on the oscilloscope.
- Record the frequencies and output powers of the first seven harmonics. Capture a screenshot of the MXA for your report. Estimate the total harmonic distortion (THD) from the output spectrum. Use the first five harmonics to estimate THD. THD (in percent) can be calculated as follows:

$$\text{THD (percent)} = \frac{\text{total power of all harmonics above fundamental}}{\text{total output power of signal}} \times 1$$

- How stable is the output at the fundamental frequency (i.e. is there any frequency drift over time)? Adjust the span and RBW, then set a fixed marker on the MXA at the peak of the fundamental. Then set up a delta marker to observe drift over time.  
Observe for one minute and record the frequency drift. The upper right hand corner should display the delta marker value—the frequency drift observed over the 1 minute time interval. Save a screenshot for your report.
- How susceptible is the output frequency to stray capacitance (e.g. hand capacitance)? Repeat the previous steps to set a fixed marker and a delta marker. Observe the effects of hand capacitance on the frequency drift. Save a screenshot for your report.
- Measure the phase-noise spectral density of the oscillator at an offset of 1 kHz from the carrier. For an explanation of Phase Noise, see Chapter 5 of the text, or, even better, read an Agilent application note. Essentially, phase noise is caused by random processes which make the frequency of your oscillator change like  $f_{inst} = f_0 + \frac{1}{2\pi} \frac{d\phi}{dt}$ . Phase noise can be combatted by using a phase-locked loop (a feedback technique) and a narrow output filter (as seen on the function generators).
  - [Mode] → [Phase Noise]
  - [Meas.] → [Log Plot]
  - Use [Auto-Tune] to tune in to your fundamental frequency
  - Set [Tracking] → [Span] to 20 kHz, if needed
  - Set a marker to display the value corresponding to a 1 kHz offset
  - Save a screenshot for your report
- Use the EXG signal generator to produce a 100 MHz signal. (Use the same power level as your VCO). Measure the phase noise at an offset of 1 kHz from the carrier. Record this value (no screenshot needed). Compare the phase noise of the VCO to that of the EXG.

## Tuning Table for VCO

Adjust the potentiometer while monitoring the DMM to obtain  $V_{pot}$  voltages from 0 V to 12 V (0.500 V increments). At each voltage, record  $f_{peak}$  and  $P_{peak}$  of the fundamental observed on the MXA.

For each voltage, compute  $C_{total}$  and  $C_{varactor}$ .  $C_{total}$  is calculated by assuming a 47 nH tank inductor.  $C_{varactor}$  is calculated by subtracting the C1/C2 series combination.

Generate a tuning table from the data above. The columns of the tuning table are:  $V_{pot}$ ,  $f_{peak}$ ,  $P_{peak}$ ,  $C_{total}$ ,  $C_{varactor}$

## **Report Guidelines**

1. Brief description of the lab (2 pts)
2. Include a circuit diagram of complete oscillator with component values (5 pts)
3. Include a picture of the constructed VCO (2 pts)
  
4. Provide the spectrum and table of 5-7 peaks. (MXA screenshot w/peak table OK) (3 pts)
5. Calculate the THD, show calculation (2 pts)
6. Describe the drift measurement and MXA settings (2 pts)
7. MXA screenshot of drift, over 1 minute interval (2 pts)
8. MXA screenshot of drift, based on hand effect (2 pts)
9. MXA screenshot of phase noise (2 pts)
10. Measured phase noise value at 1 kHz offset, for both VCO and EXG (2 pts)
11. Include the VCO tuning table, explain calculations (4 pts)
12. Include  $f$  vs.  $V_{\text{tune}}$  plot (2 pts)
13. Include  $C_{\text{var}}$  vs.  $V_{\text{tune}}$  plot (2 pts)
14. Include  $P$  vs.  $f$  plot, comment on uniformity (2 pts)
15. Compare VCO and  $X_{\text{tal}}$  oscillator: (drift, tunability) (2 pts)
  
16. One paragraph reflections from each lab partner (include name). (3 pts)

General report formatting, organization, clarity. (5 pts)

Total: 44 pts

Expected length of report is 4-8 pages, depending on graph format, line spacing, etc.