1. Introduction

1.1 Problem Statement

Designing power electronics, such as boost converters, traditionally requires bridging a significant gap between high-level natural language design requirements and complex physics-based hardware realization. This design process is often time-consuming, requires extensive domain expertise, and relies on disjointed tools for calculation, simulation, and troubleshooting. Currently, the industry lacks an intelligent, automated closed-loop workflow. There is a critical need for an agent, which can autonomously plan and decompose the design workflow for users, seamlessly translating high-level requirements into verified component parameters, guiding physical assembly, and executing automated hardware diagnostics.

1.2 Solution Overview & Visual Aid

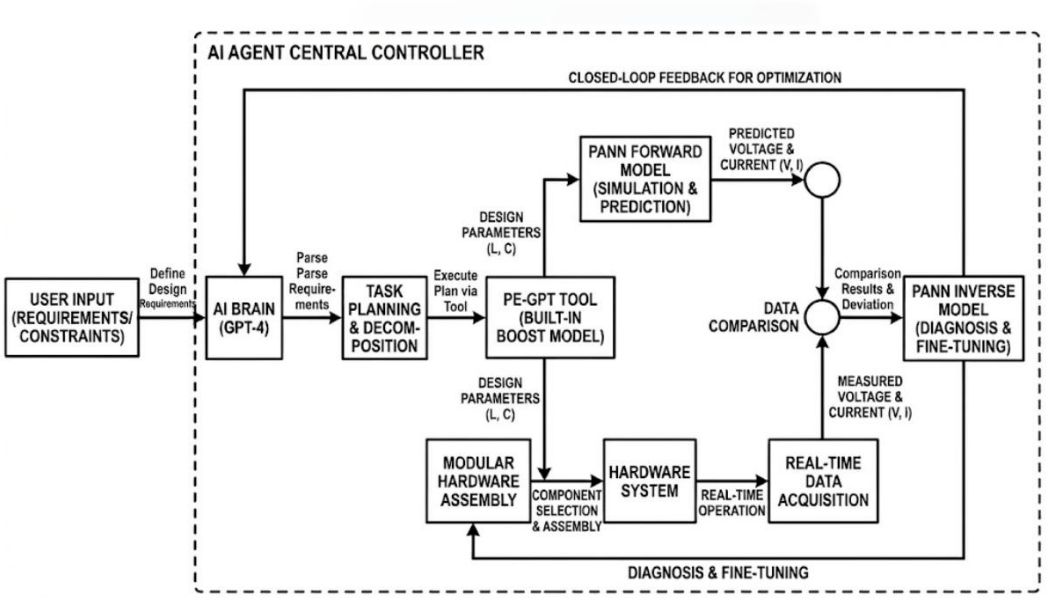

Figure 1: Visual aid diagram

The proposed PE-GPT + PANN boost converter design framework is a closed-loop, intelligent automated design system aimed at bridging the gap between high-level natural language design requirements and complex physical hardware implementation. The overall system primarily consists of an AI agent and interactive planning subsystem, a PANN simulation and diagnosis subsystem, a modular hardware assembly subsystem, and a real-time data acquisition subsystem.

The system first utilizes a GPT-4-based Brain module to receive and interpret natural language requests containing specific design constraints. Subsequently, the Planning module employs chain-of-thought reasoning to decompose the complex design task into sequentially executable steps. During the hardware parameter design phase, the system invokes the built-in boost model within the PE-GPT's Tool section to perform calculations based on specific user requirements, thereby determining the appropriate key circuit parameters (such as inductance L and capacitance C).

Upon obtaining the circuit parameters, the system utilizes the Physics-Aware Neural

Network (PANN) forward model to conduct dynamic simulations, generating dynamic response predictions for voltage and current. The pre-validated design is then directly mapped to the modular hardware assembly, guiding the actual component selection and plug-and-play PCB construction. Finally, the hardware system operates in a real-world environment. The measured real-time output voltage and current are compared with the predictive data generated by the PANN forward model to rigorously verify whether the hardware circuit responds correctly. If deviations are detected, the data is fed back into the PANN inverse model for automated deviation diagnosis and parameter fine-tuning. The AI agent acts as a central controller orchestrating all processes, enabling the system to dynamically adjust parameters in real-time and self-optimize, thereby providing users with a seamless, efficient, and fully automated closed-loop power electronics design experience.

1.3 High-Level Requirements List

	Requirement	Target Specification	Verification Method
1	The AI Agent shall generate a complete boost converter design plan from natural language input.	Design plan generated in **< 60 seconds**	Measure system response time during user interaction
2	The AI Agent shall compute valid boost converter parameters including inductance L, capacitance C, and duty cycle D.	Calculated parameters match analytical design equations within **±10%**	Compare agent output with theoretical calculations
3	The PANN forward simulation shall predict converter waveforms accurately.	Voltage and current waveform error **< 5%** compared with circuit simulation	Compare PANN output with LTspice / PLECS results
4	The hardware boost converter shall achieve the target output voltage.	Output voltage regulation within **±5% of target value**	Measure output voltage under nominal load
5	The system shall perform automated diagnostic analysis based on experimental data.	Detect parameter deviation **≥10%** in inductance or capacitance	Inject known parameter variations and test diagnosis
6	The hardware data acquisition system shall collect real-time voltage and current signals.	Sampling rate **≥10 kHz** and measurement error **<3%**	Validate measurement using oscilloscope reference

2. Design

2.1 Block Diagram

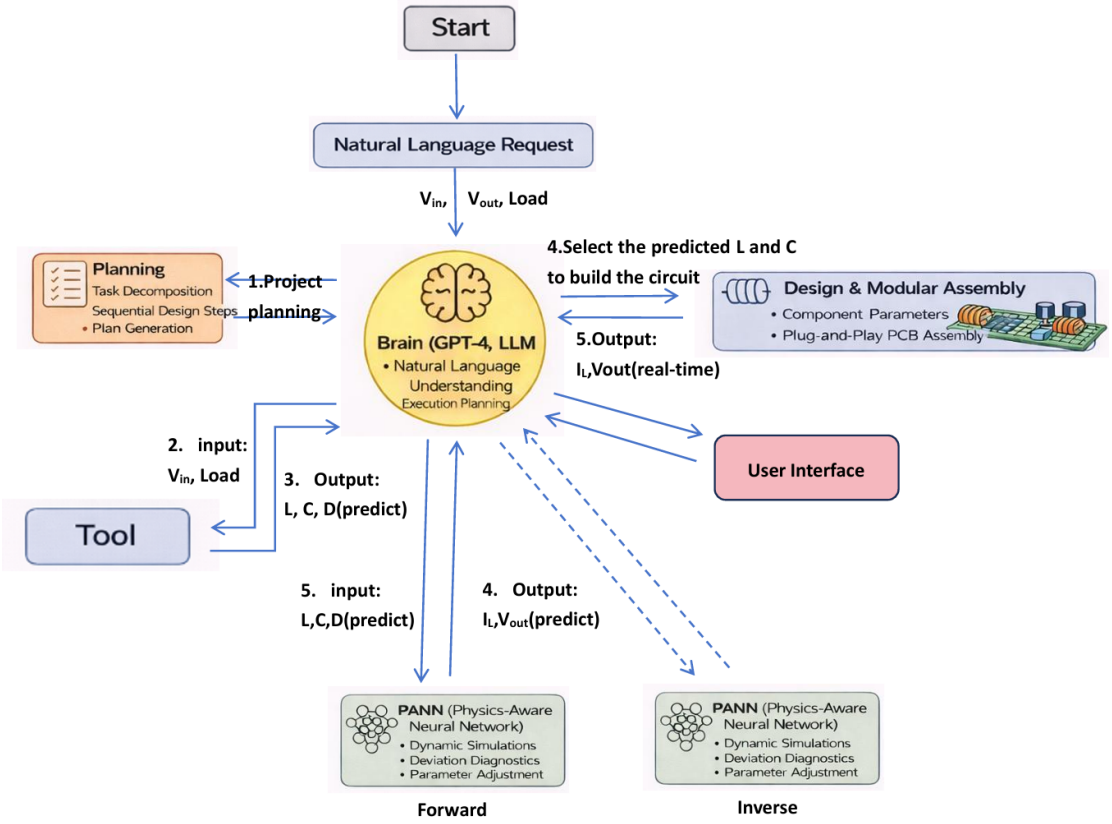

Figure 2: Block Diagram

2.2 AI Agent & Interactive Planning Subsystem

2.2.1 LLM Core (GPT-4) & RAG Module

Functional Positioning

This module serves as the semantic parsing and knowledge provision core of the AI Agent. It undertakes critical responsibilities including natural language requirement interpretation, domain knowledge retrieval, and enhanced generation. It acts as the key bridge connecting high-level user demands with executable engineering design workflows. The core objective is to eliminate the semantic gap between natural language descriptions and professional power electronics design specifications. Meanwhile, Retrieval-Augmented Generation (RAG) is adopted to mitigate inherent LLM hallucinations, providing accurate and reliable domain knowledge for subsequent planning and execution.

Core Capabilities

1. Natural Language Understanding (NLU) & Intent Parsing: The module processes natural language design requests for boost converters (e.g., design a 12 V input, 48 V output boost converter with 200 W rated power, efficiency$\geqslant$95%, and output voltage ripple$\leqslant$1%). Powered by GPT-4 contextual reasoning and entity extraction, it completes three layers of parsing:

- Hard Parameter Extraction: Structuring key specifications such as input voltage V_{in}, output voltage V_{out}, rated load power $\mathrm{P_{load}}$, target efficiency η, and output voltage ripple ΔV_{ripple}.

- Constraint Identification: Capturing physical limits (device voltage/current ratings) and application constraints (operating temperature range, volume limitations).
- Ambiguity Resolution: Converting vague expressions (e.g. high power density) into quantified metrics supported by domain knowledge.

2. Domain Knowledge Retrieval & RAG Enhancement: A dedicated vector knowledge base for power electronics and boost converter design is established to enable precise knowledge retrieval:

- Retrieve fundamental design formulas for inductance L, capacitance C, switching frequency calculation, and standard component selection guidelines for MOSFETs, inductors, and capacitors.
- Fetch practical engineering cases, failure mode analysis, and empirical design experience for similar power-level converters.
- Integrate retrieved knowledge into LLM generation to calibrate design parameters and provide reliable references for the workflow planner.

Implementation Details

- Adopt GPT-4 with function calling enabled to standardize parameter parsing and knowledge retrieval outputs for downstream compatibility.
- Apply hybrid BM25 and vector search strategies to ensure high accuracy in technical formulas and document retrieval.
- Maintain session-level context caching to preserve historical design parameters and support multi-round interactive adjustments.

2.2.2 Workflow Planner (CoT Reasoning Controller)

Functional Positioning

This module acts as the process scheduling and logic control center of the AI Agent. Based on parsed user requirements and retrieved domain knowledge, it decomposes high-level design goals into atomic executable tasks via Chain-of-Thought (CoT) reasoning. It dynamically schedules underlying tools including RAG and PANN, handles exceptions, and supports iterative optimization to achieve fully autonomous closed-loop boost converter design.

Core Capabilities

1. CoT-Based Task Decomposition & Workflow Arrangement: High-level objectives are recursively split into structured sequential tasks following standard power electronics design pipelines:

- Primary stages: requirement calibration → parameter calculation → simulation validation → component selection → modular configuration → experimental diagnosis.
- Sub-task refinement for each design phase with clear dependency management to guarantee correct execution order.

2. Tool Scheduling & State Management: The planner centrally invokes underlying functional modules:

- Trigger RAG for formula lookup during parameter calculation and call PANN forward mode for dynamic simulation evaluation.

- Maintain a finite state machine to track task status: pending, running, completed, or abnormal, supporting breakpoint recovery and rollback.
- Apply timeout retry mechanisms for unstable tool calls during simulation and computation.

3. Iterative Optimization & Feedback Handling: When PANN simulation results fail to meet performance thresholds (efficiency, ripple, stability), the planner performs root-cause analysis via CoT reasoning, generates adjustment strategies for L, C, or switching frequency, and initiates redesign iterations. User manual feedback is also integrated to update workflows dynamically.

Implementation Details

- Deploy structured CoT prompt templates specialized for power converter design to ensure explainable and consistent reasoning.
- Adopt priority queues for task scheduling to prioritize core computation and simulation tasks.
- Predefine standardized exception handling for simulation divergence, parameter overflow, and tool invocation failures.

2.2.3 Requirements & Verification Table

Functional Positioning

This module defines the quantitative baseline and quality checkpoint throughout the entire design pipeline. It establishes systematic evaluation criteria to validate parsed requirements, calculated parameters, PANN simulation results, and final design deliverables, ensuring full compliance with user specifications and engineering standards.

Core Capabilities

1. Standardized Requirement Baseline Definition

A unified evaluation table covers both explicit user demands and implicit industrial constraints: electrical performance indicators, physical limitations, thermal margins, and reliability thresholds. All metrics are quantified with clear tolerance ranges.

2. Full-Pipeline Multi-Layer Validation

- Validate the integrity and logical rationality of parameters extracted by the LLM core.
- Check calculated component parameters against physical boundaries and empirical engineering ranges.
- Compare PANN simulated waveforms and efficiency data against target values with quantified deviation rates.
- Perform final comprehensive verification for BOM recommendations and modular hardware configuration.

3. Automatic Report Generation & Feedback Loop: Structured validation reports are generated automatically, including target values, achieved values, deviation percentages, pass/fail labels, and actionable optimization suggestions. Critical failures block the workflow and trigger recalculation; minor deviations provide optional tuning recommendations for iterative improvement.

Implementation Details

- Embed computable rule sets and standard verification formulas for automatic numerical evaluation.
- Support configurable threshold adjustment for different application scenarios such as industrial power supplies and consumer electronics.
- Connect validation results directly to the workflow planner to form a closed-loop design – evaluation – optimization pipeline.

2.3 Simulation & Diagnostic Subsystem (PANN)

The Simulation and Diagnostic Subsystem is built upon a Physics-Architecture Neural Network (PANN), which is a general physics-embedded modeling framework originally proposed by Li et al[1]. Based on that, we have integrated and trained a dedicated Boost converter model *EulerCell_Boost*. Unlike conventional black-box neural networks, PANN embeds the circuit's state-space equations directly into the network architecture as hard constraints, ensuring that every prediction strictly adheres to Kirchhoff's laws. This "Structure-as-Physics" paradigm gives the model intrinsic interpretability: each learnable weight corresponds directly to a physical circuit parameter, rather than an abstract statistical coefficient.

2.3.1 PANN Architecture: The EulerCell_Boost

The core computational unit of the PANN is the EulerCell_Boost, implemented as a recurrent cell based on the Explicit Euler discretization method. The cell encodes the two-governing state-space equations of the Boost converter directly into its forward propagation path:

$$\frac{di_L}{dt} = \frac{V_{in} - (1-D)(V_{out} + V_d) - i_L \cdot r_L}{L}$$

$$\frac{dV_{out}}{dt} = \frac{(1-D) \cdot i_L - V_{out}/R}{C}$$

Discretized at time step $\Delta t = 2\,\mu s$, the cell computes the next state $(i_L^{t+1}, V_{out}^{t+1})$ from the current state (i_L^t, V_{out}^t) and the current inputs (V_{in}, D). The loss function is MSE between predicted and ground-truth next states, minimized via the Adam optimizer. Through backpropagation, the network adjusts L, C, R, V_d, and r_L to minimize prediction error, effectively performing parameter identification from waveform data.

A ReLU constraint is applied to i_L to enforce the physical requirement that inductor current cannot be negative, naturally handling Discontinuous Conduction Mode (DCM) without any additional logic.

The five learnable parameters embedded in the cell are:

Parameter	Physical Meaning	Storage Form
L	Inductance	e^{L_log}
C	Capacitance	e^{C_log}
R	Load Resistance	e^{R_log}

V_d	Diode Forward Voltage	$e^{V\_forward\_log}$
r_L	Inductor Parasitic Resistance	e^{r_log}

All parameters are stored in log-space to guarantee positivity throughout training, eliminating the need for manual clamping and ensuring physical validity at every gradient step.

2.3.2 Training Data

Training data is generated from a PLECS simulation of a standard Boost converter, performing parameter sweeps across varying input voltages and duty cycles. Each simulation run produces a CSV file with five columns: $Time, V_{in}, I_L, V_{out}, D$.

2.3.3 Forward Mode (Fast Simulation)

In Forward Mode, the PANN acts as a fast surrogate simulator. Given a set of component parameters (L, C, R) determined by the Agent's design step, the model rolls out the full dynamic waveform of i_L and V_{out} over time by iterating the *EulerCell_Boost* recurrently. This validates the design before any physical assembly takes place, replacing the need for a slow PLECS/SPICE simulation.

The key advantage over traditional simulation is speed: the PANN's forward pass consists entirely of matrix-vector multiplications with $O(N)$ complexity, compared to the iterative Newton-Raphson solver used in SPICE which scales at $O(N^{1.2} \sim N^3)$. This enables near real-time waveform generation suitable for integration into the Agent's interactive planning loop.

2.3.4 Inverse Mode (Twin Diagnosis)

In Inverse Mode, the same PANN architecture is used for parameter identification on real hardware data. Experimental waveforms of i_L and V_{out} collected from the physical PCB are fed into the training pipeline. The network then optimizes its learnable parameters to minimize the discrepancy between predicted and measured waveforms, converging to estimates of the actual circuit's L, C, R, V_d, and r_L.

By comparing the identified parameters against the nominal design values, the subsystem diagnoses performance deviations. For example, a converged L significantly lower than the designed value indicates inductor saturation or manufacturing tolerance issues. The Agent then uses these diagnostic results to suggest specific component adjustments to the user, completing the closed-loop workflow.

Requirements	**Verification**
1. PANN Forward Mode prediction error for V_{out} waveform shall be < 5% RMSE compared to PLECS ground truth across all test operating points.	Generate 10 unseen test cases in PLECS with varying V_{in} and D. Compute RMSE between PANN-predicted and PLECS-simulated V_{out} waveforms. All cases must pass the 5% threshold.
2. PANN Forward Mode waveform generation time shall be < 1s for a 10ms	Time the PANN forward pass on the target hardware (CPU inference) using Python *time* module, averaged over 10 runs.

simulation window at $\Delta t = 2\ \mu s$.

3. Inverse Mode shall converge to within 10% of the true L and C values when given clean PLECS simulation data as input.	Train PANN on PLECS data with known ground-truth L and C. Compare converged parameter estimates against ground truth.
4. Inverse Mode shall identify a $\geqslant$ 20% deviation in L and C from nominal values when such deviation is artificially introduced in simulation.	Generate PLECS data with deliberately altered L/C ($\pm 20\%$, $\pm 50\%$). Verify that PANN diagnosis correctly flags the deviation direction and magnitude within 20% error.

2.4 Hardware Execution & Data Acquisition Subsystem

The Hardware Execution and Data Acquisition Subsystem serve as the physical backbone of the closed-loop workflow. It provides a modular Boost converter platform on which the Agent's verified design is physically realized, and a STM32-based control and acquisition unit that manages the entire startup sequence, PWM generation, and real-time data collection automatically. We can control the operation of the entire hardware platform via the PE-GPT Agent. The subsystem requires no manual instrument intervention after the initial one-button system startup.

2.4.1 Plug-and-Play PCB Modules

The physical Boost converter is realized through a modular PCB design centered on a Si MOSFET half-bridge topology. To support a range of user-specified design requirements, the PCB exposes three categories of swappable component interfaces, with the following support parameter ranges:

Parameter	Supported Range
Input Voltage V_{in}	5~20 V
Output Voltage V_{out}	10~40 V
Switching Frequency f_s	20 kHz (fixed)
Duty Cycle D	0.1~0.8 (software-controlled)

The switching frequency is fixed at 20 kHz, which is well within the comfortable operating range of standard Si MOSFETs, ensuring low switching losses, stable gate drive operation, and straightforward PCB layout without requiring specialized high-frequency design techniques.

- **Inductor Interface:** A dedicated terminal block accepts interchangeable inductor modules. Three inductance values are provided to cover the Agent's design space. The selection of mH-range inductors is consistent with the 20 kHz switching frequency, as the minimum required inductance for CCM operation is given by:

$$L \geq \frac{V_{in} \cdot D}{f_s \cdot \delta i_L}$$

where Δi_L is the allowable inductor current ripple. The three available modules are:

Module	Inductance
L1	500 μH
L2	1 mH
L3	2 mH

- **Capacitor Interface:** A dedicated terminal block accepts interchangeable capacitor modules. Three capacitance values are provided to support different output ripple requirements:

Module	Capacitance
C1	220 μF
C2	500 μF
C3	1000 μF

- **Load Resistor Interface:** A dedicated terminal block accepts interchangeable load resistor modules representing different user load conditions:

Module	Resistance	Approx. Output Power (at $V_{out} = 24V$)
R1	10 Ω	57.6 W
R2	15 Ω	38.4 W
R3	22 Ω	26.2 W

All three interfaces follow a plug-and-play design: components are swapped by the user during the Agent-guided assembly phase. The PCB also integrates a relay module controlled by the STM32, which physically disconnects the half-bridge power supply until the Agent sends an explicit enable command, preventing accidental energization during component assembly.

2.4.2 Data Acquisition & Control Unit

A STM32 microcontroller is integrated on the PCB as the central control and acquisition unit. It performs three functions simultaneously: receiving design parameters from the PC-side Agent via USB-UART, generating the PWM signal to drive the half-bridge gate driver, and acquiring real-time i_L and V_{out} waveforms via its onboard ADC for transmission back to the PANN diagnostic pipeline. The complete automated startup sequence is as follows:

Phase 1 — Parameter Receipt: After the Agent computes the optimal L, C and D for the user's requirements, it transmits D to the STM32 via USB-UART. The STM32 stores the received D value but holds PWM output disabled and keeps the relay open, ensuring the half-bridge remains de-energized during component assembly.

Phase 2 — Guided Assembly: The Agent interface instructs the user to select and insert the recommended L and C modules into the PCB terminal blocks. The half-bridge board remains fully de-energized throughout this phase.

Phase 3 — Sequential Enable: Upon receiving the user's confirmation via the Agent interface, the Agent transmits an "enable" command to STM32. STM32 then executes the following timed startup sequence: PWM output is activated first at $f_s = 20\text{kHz}$ with the Agent-specified duty cycle D, followed by a 100 ms stabilization delay, after which the relay closes to connect the half-bridge power supply. This sequencing ensures the gate driver receives a stable PWM signal before the main power circuit is energized, preventing undefined switching states at startup.

Phase 4 — Data Acquisition & Transmission: With the circuit running, the STM32 continuously samples i_L and V_{out} at $f_s = 20\text{kHz}$, providing 5 sample points per switching period, which is sufficient for the PANN Inverse Mode to perform accurate parameter identification. Voltage sensing is achieved through a resistive divider that scales V_{out} down to the STM32 ADC input range of 0~3.3 V:

$$V_{ADC} = V_{out} \cdot \frac{R_2}{R_1 + R_2}$$

With $R_1 = 36k$ and $R_2 = 4.7k$, the maximum scaled voltage at $V_{out} = 40\text{V}$ is:

$$V_{ADC} = 40 \times \frac{4.7}{36+4.7} \approx 4.61V \times \frac{4.7}{40.7} \approx 3.19V$$

which remains safely within the ADC input range with adequate margin. Current sensing is achieved through a 0.1 Ω shunt resistor in series with the inductor, amplified by a rail-to-rail operational amplifier with gain $G_{amp} = 10$:

$$V_{sense} = i_L \cdot R_{shunt} \cdot G_{amp}$$

For a maximum inductor current of $i_L = 4A$, the amplified signal reaches 4×0.1×10 = 4.0 V, which requires a small correction: the op-amp gain should be reduced to $G_{amp} = 8$ to ensure the signal stays within the 3.3 V ADC range at maximum current, giving 4×0.1×8=3.2 V. The STM32 packages time-stamped (i_L, V_{out}) samples and transmits them to the PC via USB-UART at 115200 bps, where they are directly fed into the PANN Inverse Mode pipeline without any manual data export step.

Requirements	**Verification**
1. The PCB shall sustain stable Boost converter operation across the full supported range (V_{in}: 5~20 V, V_{out}: 10~40 V, D: 0.1~0.8) with output voltage ripple ≤5% of V_{out} at each tested operating point.	Test at three representative operating points covering the supported range. Measure V_{out} ripple via the STM32 ADC. Ripple must satisfy $\Delta V_{out}/V_{out} \leq 5$ at all points.
2. The STM32 shall execute the sequential enable correctly: PWM output must precede relay closure by 100 ms±10 ms.	Use a logic analyzer to timestamp the PWM enable signal and the relay control GPIO signal. Verify the delay falls within 90~110 ms across 10 consecutive startup cycles.
3. The voltage sensing circuit shall reconstruct V_{out} across the full range 10~40 V with measurement error ≤3%.	Apply known reference voltages (10 V, 24 V, 40 V) to the divider input. Compare ADC-reconstructed values against a calibrated multimeter. Error

	must be ≤3% at each point.
4. The current sensing circuit shall measure i_L in the range 0~4 A with error ≤5%.	Compare STM32 ADC-reconstructed current against a calibrated clamp meter at three load points (R_1, R_2, R_3). Error must be ≤5% at each point.
5. The Data Acquisition Unit shall transmit continuous (i_L, V_{out}) data to the PC at $f_s = 20\text{kHz}$ with zero packet loss over a 60-second acquisition window.	Run a 60-second acquisition session. Count received packets on the PC side and verify against the expected count of 60,000 samples. Packet loss must be 0%.

2.5 Schematics

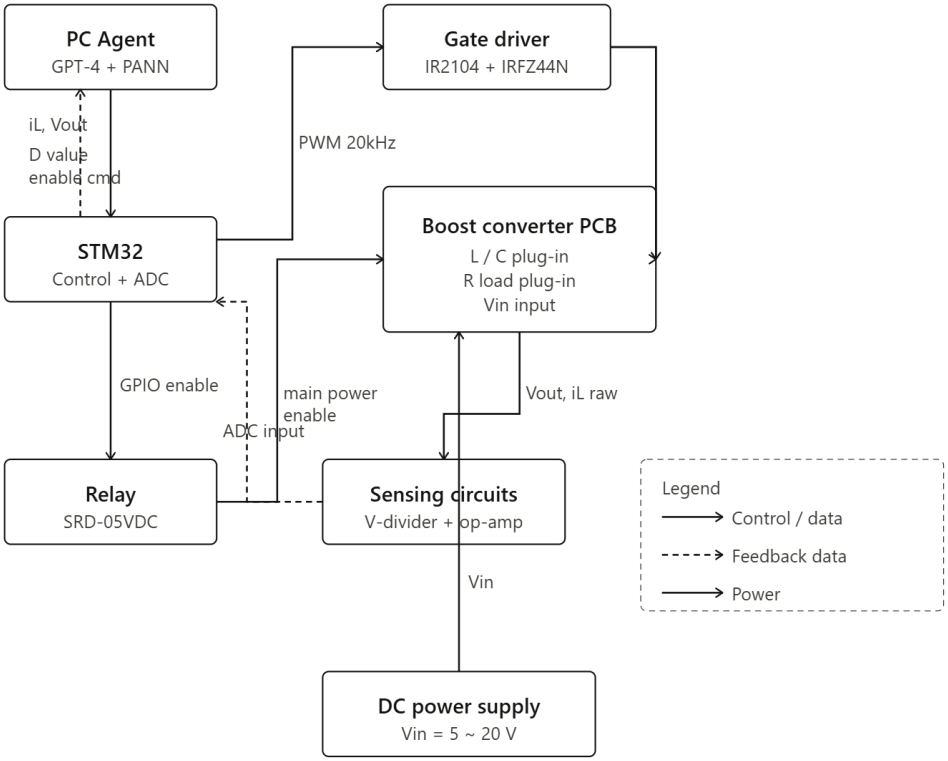

Figure 3: Overall system connection diagram

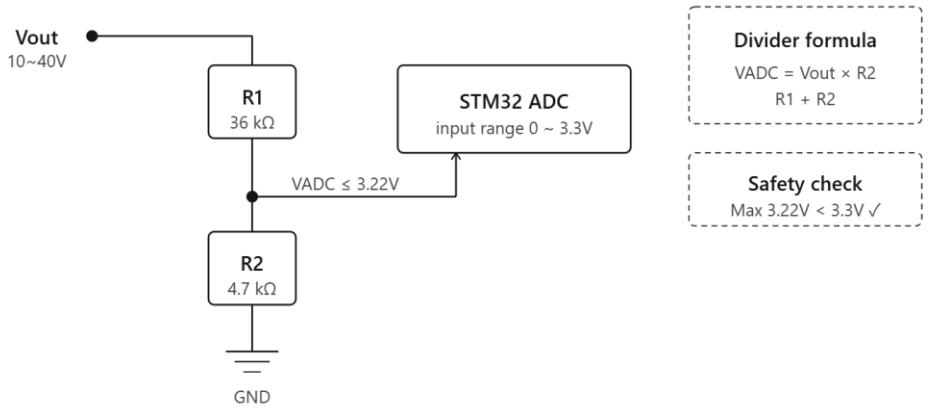

Figure 4: Voltage sensing circuit (resistive divider)

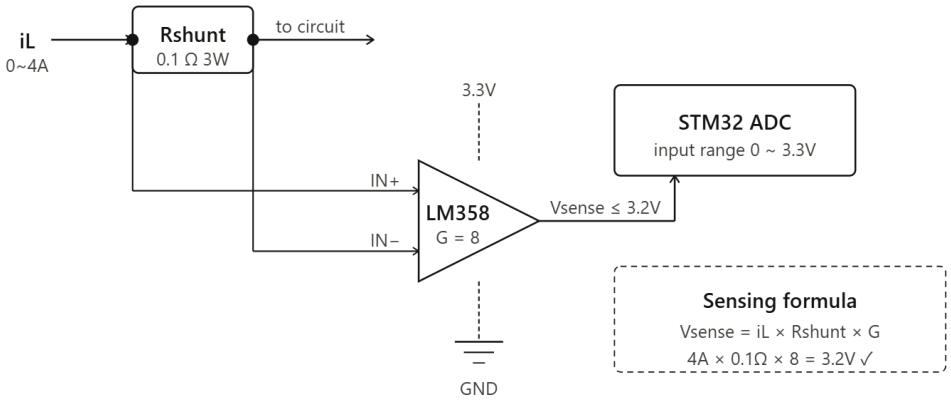

Figure 5: Current sensing circuit (shunt + op-amp)

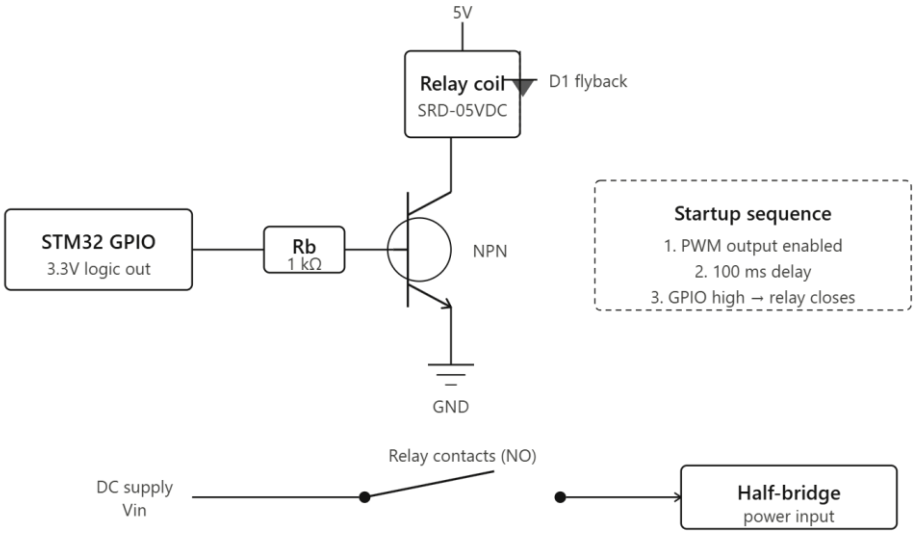

Figure 6: Relay control circuit with startup sequence

2.6 Tolerance Analysis

In practical power electronics systems, component tolerances and non-ideal characteristics may influence converter performance. For the proposed boost converter, tolerance analysis focuses primarily on variations in the inductor and output capacitor, which are the most critical passive components in the circuit.

The steady-state voltage conversion ratio of an ideal boost converter is given by

$$V_o = \frac{V_{in}}{1 - D}$$

where V_{in} is the input voltage and D is the duty cycle. This relationship shows that the output voltage is mainly determined by the duty cycle, while passive component variations primarily affect ripple and dynamic behavior.

Inductor Tolerance

Commercial inductors typically have tolerances of approximately **±20%**. Variations in inductance affect the inductor current ripple and may influence the conduction mode of the converter. However, the steady-state voltage conversion ratio remains unchanged as long as the converter operates in continuous conduction mode.

Capacitor Tolerance

The output capacitor influences the output voltage ripple, which can be approximated as

$$\Delta V_o \approx \frac{I_o D}{f C}$$

where I_o is the output current, f is the switching frequency, and C is the output capacitance.

From this relationship, a 10% decrease in capacitance results in approximately a 10% increase in voltage ripple. The selected capacitor value ensures that the output ripple remains within acceptable limits even under tolerance variations.

System Robustness

Considering typical component tolerances (±20% for inductors and ±10% for capacitors), the converter is expected to maintain stable operation and output voltage regulation within ±5% of the target value. Additionally, the PANN diagnostic subsystem can analyze measured waveforms to detect parameter deviations and assist users in identifying potential component mismatches.

3 Cost

Component	Description	Quantity	Unit Price (RMB)	Total (RMB)
STM32F103C8T6	Main microcontroller, with USB-UART, ADC, TIM PWM output	1	15	15
IR2104 + IRFZ44N	Si half-bridge gate driver + MOSFET pair, rated 55V/49A, suitable for 20kHz	1 set	20	20
SRD-05VDC-SL-C	5V relay module, controls half-bridge power supply enables	1	8	8
LM358	Rail-to-rail op-amp for current sensing amplification, gain = 8	1	2	2
Shunt Resistor 0.1 Ω	Current sensing, rated 3W	1	3	3
Resistor Kit	$R_1 = 36k\Omega, R_2 = 4.7k\Omega$ for voltage divider, plus misc	1 set	5	5
Inductor L1	500 μH, rated 5A	1	15	15
Inductor L2	1 mH, rated 5A	1	18	18
Inductor L3	2 mH, rated 5A	1	22	22
Capacitor C1	220 μF, 63V electrolytic	1	5	5
Capacitor C2	500 μF, 63V electrolytic	1	8	8
Capacitor C3	1000 μ, 63V electrolytic	1	12	12
Load Resistor R1	10 Ω, rated 50W wire wound	1	15	15
Load Resistor R2	15 Ω, rated 50W wire wound	1	15	15
Load Resistor R3	22 Ω, rated 50W wire wound	1	15	15
Terminal Block Connectors	Plug-and-play interfaces for L, C, R modules	1 set	10	10
PCB Manufacturing	Custom PCB, 2-layer, 100mm × 100mm, JLCPCB	5 pcs	4	20
Miscellaneous	Capacitors, resistors, headers, wires, solder	1 set	20	20
Total				228

4 Schedule

Week	Haojun Li	Xinyu Zhan	Jiarong Xu	Jiaming Ma
3.30	Confirm framework & interfaces	Assist system framework discussion and documentation	Order all components (STM32, MOSFET, relay, passives)	Set up PE-GPT environment and reproduce baseline
4.6	Build PE knowledge base	Help build PE knowledge base	Complete PCB schematic	Test PE-GPT workflow and agent interaction
4.13	Finish requirement parsing	Assist development of requirement parsing module	Finish PCB layout and submit for fabrication	Implement requirement parsing for converter design
4.20	Develop core planning logic	Support development of planning logic	Solder boards; verify STM32 boot and UART	Integrate PANN forward simulation
4.27	Deliver full version for PANN	Implement verification routines for agent outputs	Verify PWM, relay sequence, and sensing circuits	Connect agent planning with PANN simulation
5.4	Integrate verification loops	Assist integration of PANN simulation pipeline	Full closed-loop integration; verify data transmission	Implement hardware data interface
5.11	Embed safety rules & testing	Support system debugging and testing	Debug hardware; test all L/C/R module combinations	Develop PANN inverse diagnosis module
5.18	Final integration & document freeze	Assist final system validation and demo preparation	Prepare demo platform; rehearse with software team	Final system integration and demo support

5 Ethics & Safety

5.1 Ethics

5.1.1 Ethical Principles for AI-Driven Power Electronics Design

This project adheres to core ethical principles for responsible AI development,

ensuring the Boost Converter Design Agent operates with transparency, accountability, and fairness throughout its lifecycle.

1. Transparency & Explainability: The AI agent's design decisions, parameter calculations, and optimization suggestions are fully traceable. All design workflows, reasoning paths (via Chain-of-Thought), and simulation results are documented in human-readable format, eliminating "black box" decision-making. Users can audit every step of the design process, from requirement parsing to final component selection, ensuring full visibility into how the AI generates recommendations.
2. Accountability & Responsibility: The system is designed as an assistive tool for engineers, not a replacement for human oversight. All AI-generated designs require explicit human validation before physical implementation, with clear disclaimers that the final responsibility for hardware safety and performance rests with the human designer. The agent includes mandatory human-in-the-loop checkpoints at critical stages (e.g. parameter finalization, PCB assembly) to prevent unvetted designs from being deployed.
3. Fairness & Non-Discrimination: The RAG knowledge base and training data for PANN are curated to include diverse design cases, industry standards, and component options from global manufacturers, avoiding bias toward specific vendors, regions, or design methodologies. The agent provides equal, objective design recommendations regardless of user background, ensuring accessibility for both expert engineers and students learning power electronics design.
4. Data Privacy & Security: All user input, design data, and experimental results are processed with strict privacy protection. Sensitive design specifications, proprietary project data, and user information are encrypted in transit and at rest, with no unauthorized access or data sharing. The system complies with global data protection regulations (e.g. GDPR, CCPA) and institutional research ethics guidelines, ensuring user data is only used for the intended design workflow.
5. Responsible Innovation & Misuse Prevention: The agent is restricted to legitimate, non-harmful applications of power electronics design. It includes guardrails to prevent misuse for unauthorized or dangerous projects (e.g. high-voltage designs without proper safety certification, unregulated power supplies for critical infrastructure). The system enforces compliance with international power electronics safety standards (e.g., IEC 60950, UL 60950) in all design recommendations, blocking non-compliant parameter configurations.

5.1.2 Ethical Risk Mitigation

- Hallucination Mitigation: The RAG module and verification table act as ethical safeguards, ensuring the AI only generates design recommendations grounded in verified domain knowledge and physical laws, eliminating speculative or incorrect outputs that could lead to unsafe hardware.
- Bias Auditing: Regular audits of the knowledge base and agent outputs are conducted to identify and resolve any implicit bias in component selection, design methodologies, or vendor recommendations.

- Ethical Review Board Oversight: The project undergoes periodic review by an institutional ethical review board to ensure ongoing compliance with research ethics and responsible AI principles.

5.2 Safety

5.2.1 Hardware Safety for Boost Converter Design

This section addresses safety risks associated with physical boost converter implementation, ensuring the AI agent prioritizes user safety, hardware reliability, and compliance with global safety standards.

1. Electrical Safety Guardrails: The agent enforces strict safety constraints in all design calculations and recommendations:

- Component Derating: Mandates minimum 20% voltage, current, and temperature derating for all power components (inductors, capacitors, MOSFETs) to prevent overstress, thermal runaway, and component failure.
- Overvoltage/Overcurrent Protection: Automatically includes design recommendations for overvoltage protection (OVP), overcurrent protection (OCP), and short-circuit protection (SCP) circuits in all generated designs, ensuring the converter can safely handle fault conditions.
- Isolation & Insulation: For high-voltage boost converter designs, the agent specifies compliance with isolation standards (e.g., IEC 60664) and recommends appropriate insulation distances, creepage, and clearance for PCB design to prevent electric shock hazards.

2. Thermal Safety & Reliability: The PANN simulation module integrates thermal modeling to evaluate component temperature rise under full-load conditions. The agent flags designs with component temperatures exceeding safe operating limits (per manufacturer datasheets) and provides optimization suggestions (e.g., heat sink sizing, component layout adjustment) to ensure thermal safety and long-term reliability.
3. EMC/EMI Safety Compliance: The agent incorporates electromagnetic compatibility (EMC) and electromagnetic interference (EMI) design guidelines into all recommendations, ensuring the boost converter complies with international EMC standards (e.g., CISPR 32, FCC Part 15). It suggests EMI filtering, shielding, and layout optimizations to prevent harmful electromagnetic emissions that could interfere with other electronic systems.
4. User Safety Guidance: The system provides clear, step-by-step safety warnings and operational guidelines for physical assembly, testing, and deployment of the designed boost converter. This includes warnings for high-voltage operation, proper ESD (electrostatic discharge) protection during assembly, and safe testing procedures to prevent injury or equipment damage.

5.2.2 AI System Safety

5. Robustness & Fault Tolerance: The AI agent includes multiple layers of safety checks to prevent system failures:

- Input Validation: Rejects invalid or unsafe design requirements (e.g., impossible

voltage conversion ratios, non-physical component parameters) and provides clear error messages to the user.

- Simulation Validation: All design parameters are validated via PANN simulation before being presented to the user, ensuring the design is physically realizable and free from catastrophic failure risks (e.g., inductor saturation, capacitor voltage breakdown).
- Fallback Mechanisms: In the event of AI reasoning errors or tool failures, the system falls back to manual design workflows and human oversight, preventing automated generation of unsafe designs.

6. Cybersecurity Safety: The system is protected against unauthorized access, tampering, and malicious attacks. All API calls, data transfers, and user interactions are encrypted, and the agent is designed to operate in a secure, air-gapped environment for sensitive industrial or research projects, preventing external interference with design workflows.
7. Safety Compliance & Certification: All design recommendations are aligned with global power electronics safety standards (e.g., IEC, UL, CSA) and industry best practices. The agent generates documentation to support third-party safety certification of the final hardware, ensuring the designed boost converter meets regulatory requirements for commercial deployment.

5.2.3 Safety Risk Mitigation

- Pre-Deployment Safety Testing: All AI-generated designs undergo rigorous safety testing (electrical, thermal, EMC) in a controlled laboratory environment before real-world deployment.
- Continuous Safety Monitoring: Post-deployment, the twin diagnosis module monitors hardware performance in real time, detecting safety-critical deviations (e.g., overheating, efficiency drop) and alerting users to potential hazards.
- Safety Training & Documentation: The project provides comprehensive user documentation and safety training to ensure all users understand the risks of power electronics design and the proper use of the AI agent.

References

[1] X. Li *et al.*, “Temporal Modeling for Power Converters With Physics-in-Architecture Recurrent Neural Network,” *IEEE Transactions on Industrial Electronics*, vol. 71, no. 11, pp. 14111–14123, Nov. 2024, doi: 10.1109/TIE.2024.3352119.