ECE 445

SENIOR DESIGN LABORATORY

DESIGN DOCUMENT

Automated Guided Vehicle Wireless Charging System with DSP-Based Position-Adaptive Frequency Control

Team #14

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1. Introduction

1.1 Problem Statement

Wireless power transfer (WPT) has emerged as a promising charging solution for electric vehicles (EVs) and automated guided vehicles (AGVs), driven by national carbon-neutrality goals and the rapid development of intelligent transportation systems [1, 2]. Unlike conventional plug-in charging, WPT enables power delivery across an air gap without physical connectors, offering improved safety, convenience, and system longevity.

However, practical WPT systems suffer from significant efficiency degradation when the transmitter (Tx) and receiver (Rx) coils are misaligned, a common occurrence in real AGV parking scenarios [3]. Existing systems typically operate at a fixed switching frequency and lack position-adaptive control, resulting in suboptimal power transfer under non-ideal alignment conditions. The previous generation of this project (Spring 2025, Project No. 39) operated at a fixed switching frequency with no position feedback or adaptive control. When coils were offset from their ideal alignment, transfer efficiency dropped considerably with no mechanism to compensate. Additionally, no automated vision-based positioning or precision parking capability was implemented, meaning the AGV had no way to actively reduce coil misalignment prior to charging.

1.2 Solution Overview & Visual Aid

We propose an integrated closed-loop AGV wireless charging system that addresses misalignment through two complementary strategies: (1) vision-assisted precision parking that physically minimizes coil offset before charging begins, and (2) DSP-based position-adaptive frequency modulation that compensates for any residual misalignment through real-time switching frequency adjustment.

The system integrates three processors with distinct roles:

- A Raspberry Pi 4B performs real-time ArUco marker detection via USB camera, computes the coil offset (x, y) and rotation angle using OpenCV PnP pose estimation, and broadcasts position data over UART to both the DSP and STM32.
- A STM32 microcontroller executes line-following during transit and transitions to vision-guided precision parking when the charging station enters camera view, driving DC motors with encoder feedback to achieve sub-centimeter alignment.
- A DSP TMS320F28335 receives position offset data and maps it through a pre-characterized look-up table to the optimal switching frequency for the CLLC resonant converter, maintaining high transfer efficiency despite residual misalignment.

The power stage employs a CLLC resonant topology with a base switching frequency of 50 kHz, operating from a 21 V DC input to deliver at least 20 W at 12 V to the AGV battery. The adaptive frequency modulation range is estimated at 47–53 kHz, covering the coupling coefficient variation expected under realistic parking offsets.

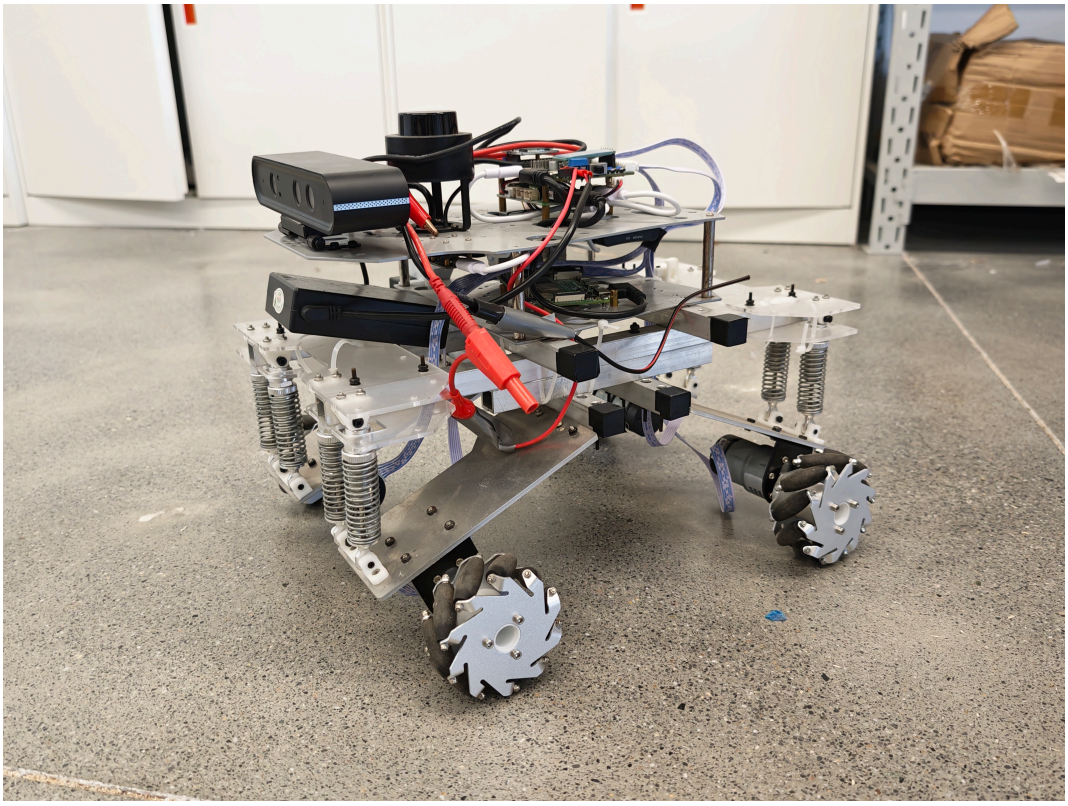

Figure 1: Visual aid illustrating the system architecture and key components: the AGV equipped with a Raspberry Pi and STM32 for vision-assisted parking, the wireless charging station with Tx coil and DSP-based adaptive frequency control, and the power flow from the 21 V DC source through the CLLC converter to the Rx coil and rectifier.

1.3 High-Level Requirements List

1. **Wireless Charging Efficiency:**
   - The system shall deliver $\geq 20\,\text{W}$ of charging power at $12\,\text{V} \pm 0.5\,\text{V}$ output.
   - DC-DC power transfer efficiency shall remain $\geq 75\%$ under coil misalignment up to $\pm$ 2 cm in any lateral direction, measured with the adaptive frequency control active.
2. **Visual Positioning Accuracy:**
   - The ArUco-based vision system shall estimate coil offset with an accuracy of $\pm$ 5 mm and orientation angle within $\pm\ 3^\circ$ at the operational camera-to-marker distance.
   - After vision-assisted precision parking, the residual coil misalignment shall be $\leq$ 1 cm.
3. **Adaptive Frequency Control:**

- The DSP shall adjust the CLLC switching frequency within the range of 50 kHz $\pm$ 3 kHz based on received position data.
- The end-to-end frequency update latency (from position capture to new PWM period) shall be $\leq$ 50 ms.

4. **Output Voltage Stability:**
   - Output voltage ripple shall be $\leq$ 0.5 V peak-to-peak under steady-state charging conditions, achieved with the 100 μF output filter capacitor.

2. Design

2.1 Block Diagram

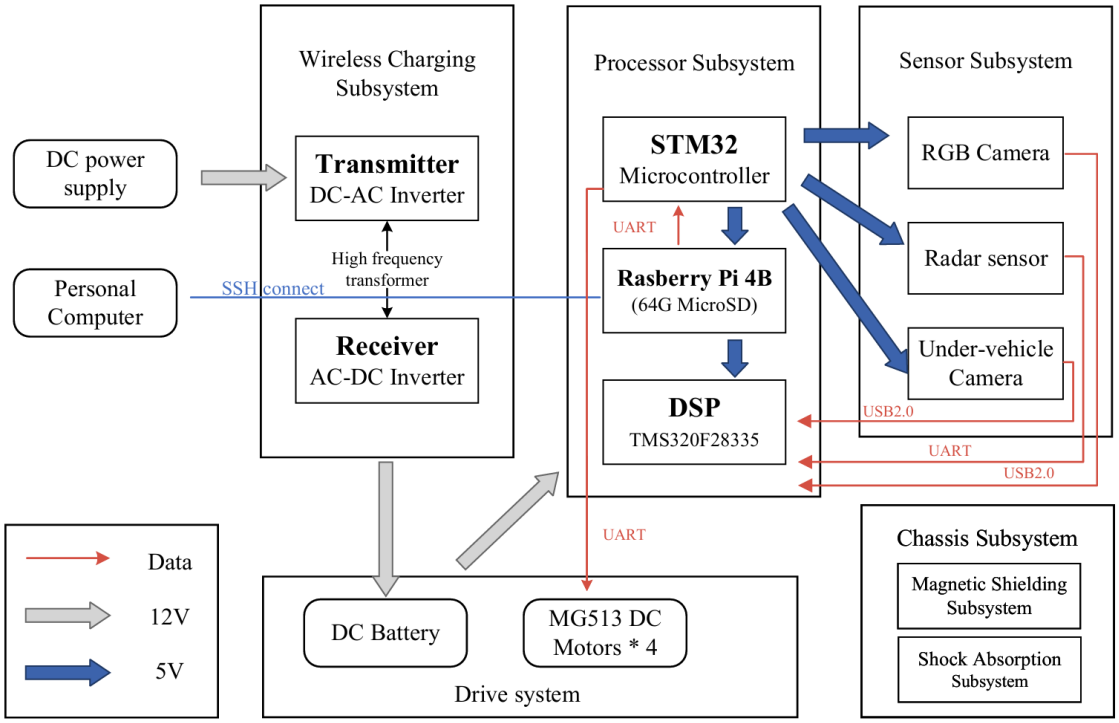

Figure 2: Block diagram of the complete system

2.2 Wireless Charging Subsystem

The wireless charging subsystem is responsible for converting a 21V DC input into a regulated 12V DC output to charge the AGV's onboard battery across an air gap. It adopts a symmetric CLLC resonant converter topology [4], with the base switching frequency set to 50 kHz. Compared to the previous-generation system which operated at a fixed frequency with no position feedback, the key innovation of this subsystem is DSP-based pulse frequency modulation (PFM): a TMS320F28335 digital signal controller [5] receives real-time

coil position offset data from the visual positioning subsystem and dynamically adjusts the switching frequency in a narrow range around 50 kHz to compensate for coupling coefficient variations caused by residual coil misalignment, thereby maintaining high transfer efficiency without requiring perfect mechanical alignment.

2.2.1 Resonant Converter Topology (CLLC)

The subsystem employs a symmetric CLLC resonant converter consisting of three stages: a full-bridge inverter on the transmitter (Tx) side that converts 21V DC to high-frequency AC, a CLLC resonant tank spanning both sides of the loosely coupled transformer (Tx and Rx coils), and a full-bridge rectifier on the receiver (Rx) side that converts the AC back to DC for battery charging. The overall circuit topology is illustrated in Figure 3.

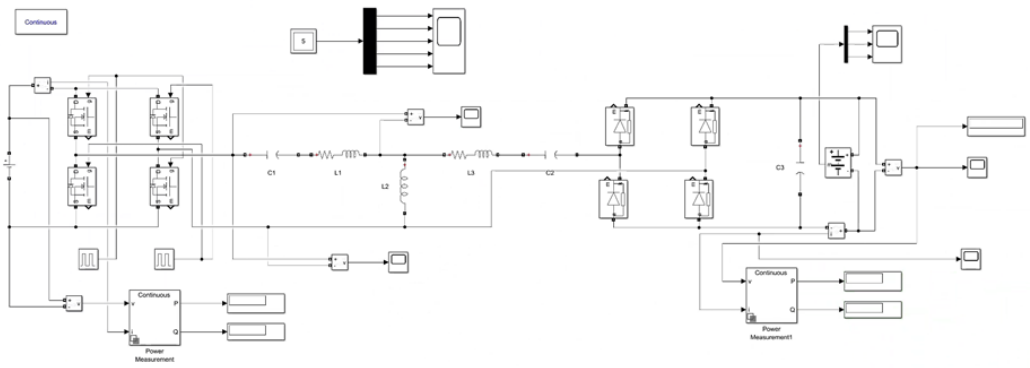

Figure 3: CLLC resonant converter topology. Left: full-bridge inverter and primary resonant tank (L_1, C_1). Center: loosely coupled transformer (Tx/Rx coils with coupling coefficient k). Right: secondary resonant tank (L_3, C_2) and full-bridge rectifier.

The CLLC topology is selected for the following reasons:

- **Symmetric structure:** The resonant elements exist on both the primary and secondary sides, allowing the converter to achieve a load-independent voltage gain when the resonant components are properly matched, which simplifies output voltage regulation.
- **Soft switching capability:** At and near the resonant frequency, the CLLC converter naturally achieves zero-voltage switching (ZVS) for the inverter MOSFETs and zero-current switching (ZCS) for the rectifier diodes, significantly reducing switching losses at 50 kHz [3].
- **Frequency-dependent gain:** The voltage gain of the CLLC network varies monotonically with switching frequency near resonance. This characteristic is the foundation of our adaptive PFM strategy—small frequency deviations from the resonant point can compensate for coupling coefficient changes caused by coil misalignment.

Voltage Gain Analysis. The voltage gain of the CLLC resonant network is derived using Kirchhoff's voltage laws. Denoting the impedances of the three resonant branches as Z_1 (primary series LC), Z_2 (magnetizing branch), and Z_3 (secondary series LC), and the load impedance as Z_L, the voltage gain is given by:

$$G = \frac{V_{out}}{V_{in}} = \frac{Z_3}{Z_1 + Z_3 + \dfrac{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3}{Z_L}} \tag{1}$$

To achieve load-independent gain (i.e., the output voltage does not vary with load current), the following condition must be satisfied:

$$Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 = 0 \tag{2}$$

When Equation (2) holds, the gain simplifies to a purely reactive voltage divider:

$$G = \left| \frac{Z_3}{Z_1 + Z_3} \right| \tag{3}$$

Each resonant branch impedance consists of a series inductor L_i and capacitor C_i:

$$Z_i = j\omega L_i + \frac{1}{j\omega C_i} = j\left(\omega L_i - \frac{1}{\omega C_i}\right) \tag{4}$$

At the resonant frequency ($\omega_r = 2\pi f_r = 2\pi \times 50\,\text{kHz}$), each branch impedance can be driven to zero by selecting:

$$C_i = \frac{1}{\omega_r^2 \, L_i} \tag{5}$$

When $Z_1 = Z_2 = 0$ at resonance, Equation (2) is automatically satisfied, and the gain approaches unity ($G \to 1$). The actual required gain is less than unity due to semiconductor voltage drops, as analyzed below.

Required Gain and Component Calculation. Accounting for MOSFET conduction losses in the full-bridge inverter ($\sim$1.5V total drop across two series devices) and diode forward voltage drops in the rectifier ($\sim$1.0V total), the required gain of the resonant network is:

$$G_{required} = \frac{V_{out} + V_{diode}}{V_{in} - V_{MOSFET}} = \frac{12 + 1.0}{21 - 1.5} = \frac{13}{19.5} \approx 0.667 \tag{6}$$

This near-unity gain is achievable with the CLLC topology by designing Z_1 and Z_2 to resonate at 50 kHz (driving them close to zero), so the gain is primarily set by Z_3 and the transformer turns ratio. In the symmetric design, the primary and secondary resonant inductances are equal to the respective coil self-inductances, and the resonant capacitors are calculated from Equation (5).

Assuming a coil inductance of $L = 100\,\mu\text{H}$ (to be finalized after coil fabrication and measurement by Jinru Cai), the corresponding resonant capacitance is:

$$C = \frac{1}{(2\pi \times 50000)^2 \times 100 \times 10^{-6}} = \frac{1}{9.870 \times 10^{10} \times 10^{-4}} \approx 101.3\,\text{nF} \tag{7}$$

In practice, the nearest standard capacitor value (100 nF) will be used, with fine tuning achieved by adding a small parallel trim capacitor if necessary.

Off-Resonance Behavior and Frequency Tunability. When the switching frequency f_{sw} deviates from f_r, the branch impedances Z_i become non-zero and the gain G shifts according to Equation (1). This frequency-dependent gain behavior is the mechanism that enables our adaptive control: as coil misalignment changes the effective coupling coefficient k and thus the reflected load Z_L, the DSP shifts f_{sw} slightly above or below 50 kHz to an operating point where the gain compensates for the coupling change, maintaining the target output voltage.

The sensitivity of gain to frequency deviation depends on the quality factor Q of the resonant tank:

$$Q = \frac{\omega_r L}{R_{ac}} = \frac{2\pi f_r L}{\frac{8}{\pi^2} \cdot \frac{V_{out}^2}{P_{out}}} \tag{8}$$

where $R_{ac} = \frac{8}{\pi^2} \cdot \frac{V_{out}^2}{P_{out}}$ is the equivalent AC load resistance. For our design targets ($V_{out} = 12\,\text{V}$, $P_{out} = 20\,\text{W}$, $L = 100\,\mu\text{H}$):

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{144}{20} \approx 5.84\,\Omega, \qquad Q = \frac{2\pi \times 50000 \times 100 \times 10^{-6}}{5.84} \approx 5.4 \tag{9}$$

A Q value of approximately 5 provides a good trade-off: high enough for efficient resonant operation with minimal circulating currents, yet low enough that the gain curve has a meaningful slope near f_r, allowing effective frequency adjustment within $\pm$3–5 kHz. If the measured Q turns out to be too high (excessively narrow bandwidth), additional damping resistance can be introduced in the resonant tank.

Requirements	Verification
1. Output voltage: 12V ± 0.5V under perfectly aligned condition at 50 kHz	1. Connect a 7.2 Ω resistive load (≈20 W at 12 V) to rectifier output. Measure V_{out} with oscilloscope over 60 s. Pass: $V_{out} \in [11.5,\ 12.5]$ V throughout
2. ZVS achieved for all four inverter MOSFETs at 50 kHz under nominal load	2. Capture V_{DS} and V_{GS} simultaneously on each MOSFET with oscilloscope. Pass: V_{DS} falls below 1 V before V_{GS} rises above threshold for every switching cycle
3. Measured voltage gain within ±10% of design value (0.667) at 50 kHz	3. Measure V_{out}/V_{in} at aligned condition and nominal load. Pass: $G \in [0.60,\ 0.73]$
4. Overall DC-to-DC efficiency ≥ 75% at aligned condition, 20 W output	4. Measure $P_{in} = V_{in} \times I_{in}$ and $P_{out} = V_{out} \times I_{out}$ with multimeters. Pass: $\eta = P_{out}/P_{in} \geq 75\%$

2.2.2 DSP Adaptive Frequency Control (PFM)

The TMS320F28335 digital signal controller serves as the core frequency control unit. It receives real-time coil position offset data (Δx, Δy) from the Raspberry Pi via UART, maps the offset to an optimal switching frequency using a pre-calibrated look-up table (LUT), and outputs high-resolution PWM signals to drive the full-bridge inverter through the gate drivers.

Control Flow. The adaptive frequency control operates as a position-feedforward system with the following steps executed in each control cycle:

1. The visual positioning subsystem (Raspberry Pi) detects the ArUco marker on the charging station and computes the coil offset (Δx, Δy) in millimeters.
2. The offset data is transmitted to the DSP via UART at 115200 bps in a structured packet (Table 2), at an update rate ≥ 10 Hz.
3. Upon receiving a valid packet, the DSP computes the radial offset:
$$d = \sqrt{\Delta x^2 + \Delta y^2} \tag{10}$$
4. The DSP uses the pre-built LUT to determine the optimal switching frequency $f_{opt}(d)$ via linear interpolation between calibration points.
5. The ePWM timer period register (`TBPRD`) is updated to set the new frequency:
$$\texttt{TBPRD} = \frac{f_{clk}}{f_{opt}} - 1 \tag{11}$$
where $f_{clk} = 150$ MHz is the DSP system clock.
6. The frequency transition takes effect at the next PWM cycle boundary, ensuring glitch-free switching.

Look-Up Table Construction. The LUT maps radial coil offset $d\,(\text{mm})$ to optimal switching frequency $f_{opt}\,(\text{Hz})$. It is constructed through an offline calibration procedure before deployment:

1. Fix the Tx and Rx coils at a known offset position d_i (measured with calipers).
2. Sweep the switching frequency from 45 kHz to 55 kHz in 0.5 kHz steps.
3. At each frequency, measure output power $P_{out} = V_{out} \times I_{out}$ and input power $P_{in} = V_{in} \times I_{in}$.
4. Record the frequency $f_{opt,i}$ that yields maximum transfer efficiency $\eta = P_{out}/P_{in}$.
5. Repeat for offset positions $d = 0, 2, 5, 8, 10, 12, 15, 18, 20\,\text{mm}$.
6. Store the resulting $(d_i, f_{opt,i})$ pairs in DSP flash memory as a fixed-point array.

Since the coil misalignment after vision-assisted parking is expected to be small ($\leq 20\,\text{mm}$) and the coupling coefficient varies smoothly with offset, the LUT is expected to contain approximately 10 entries, with linear interpolation providing sufficient accuracy between calibration points. Table 1 shows a hypothetical LUT; actual values will be determined experimentally.

Offset d (mm)	**Est. coupling k**	**f_{opt} (kHz)**	**Est. efficiency η**
0	0.35	50.0	80%
5	0.32	50.5	78%
10	0.28	51.5	75%
15	0.23	52.5	70%
20	0.18	53.5	65%

Table 1: Hypothetical look-up table entries (actual values TBD from calibration experiments)

PWM Resolution Analysis. The F28335 system clock is 150 MHz. At 50 kHz, the ePWM timer period is:

$$\texttt{TBPRD} = \frac{150 \times 10^6}{50 \times 10^3} - 1 = 2999 \quad \text{(3000 counts per PWM cycle)} \tag{12}$$

The minimum achievable frequency step is:

$$\Delta f_{min} = \frac{f_{clk}}{\texttt{TBPRD} \times (\texttt{TBPRD} + 1)} \approx \frac{150 \times 10^6}{3000 \times 3001} \approx 16.7\,\text{Hz} \tag{13}$$

Within a ± 5 kHz adjustment range, this provides over 600 discrete frequency steps—far more than the resolution required for smooth gain adjustment.

UART Communication Protocol. The position data packet from the Raspberry Pi to the DSP follows the format shown in Table 2. Position values are transmitted as signed 16-bit integers in units of 0.1 mm (e.g., a value of 125 represents 12.5 mm). The checksum is the XOR of all bytes between the header and the checksum field.

Header	**Δx (int16)**	**Δy (int16)**	**Angle (int16)**	**Status**	**Checksum**
0xAA 0x55	2 bytes	2 bytes	2 bytes	1 byte	1 byte

Table 2: UART data packet format (Raspberry Pi → DSP), 10 bytes per packet

At 115200 bps with 8N1 framing, a 10-byte packet requires $10 \times 10/115200 \approx 0.87$ ms to transmit, well within the 100 ms budget for a 10 Hz update rate.

Requirements	**Verification**
1. DSP outputs PWM at commanded frequencies across 45–55 kHz with accuracy $\leq \pm 100$ Hz	1. Send test commands to set frequencies at 45, 47.5, 50, 52.5, 55 kHz. Measure actual output with oscilloscope (frequency counter mode). Pass: $\lvert f_{meas} - f_{cmd} \rvert \leq 100$ Hz for all test points
2. Control latency (UART RX to PWM update) ≤ 20 ms	2. DSP toggles GPIO-A on UART RX interrupt and GPIO-B on `TBPRD` register write. Measure interval with logic analyzer over 100 packets. Pass: average ≤ 20 ms, max ≤ 30 ms
3. V_{out} maintained within 12V $\pm$ 0.5V at offsets of 0, 10, 20 mm with adaptive PFM enabled	3. Physically offset Rx coil to each position; record V_{out} with PFM on and off (fixed 50 kHz). Pass: $V_{out} \in [11.5,\ 12.5]$ V at all positions with PFM on. Document ΔV_{out} and $\Delta\eta$ improvement over fixed frequency
4. LUT interpolation produces smooth, monotonic frequency output	4. Inject synthetic offsets 0–20 mm in 1 mm steps via test UART packets. Record PWM frequency at each step. Pass: monotonically increasing, no step > 200 Hz between adjacent 1 mm increments

2.2.3 Coil Design and Magnetic Coupling

The transmitter (Tx) and receiver (Rx) coils form the loosely coupled transformer that transfers power across the air gap between the charging station and the AGV. Their self-inductance, mutual inductance, and coupling coefficient directly determine the resonant network behavior and the range of frequency adjustment required for the adaptive PFM control.

Coil Geometry and Construction. New Tx and Rx coils will be wound for this project to match the 50 kHz resonant frequency. Both coils are planar circular spiral coils wound

with multi-strand enamel-insulated copper wire. The key design parameters are summarized in Table 3. Multi-strand wire is chosen because, at 50 kHz, the skin depth in copper is approximately:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} = \sqrt{\frac{1.68 \times 10^{-8}}{\pi \times 50000 \times 4\pi \times 10^{-7}}} \approx 0.29\,\text{mm} \tag{14}$$

By using individual strands with diameter $< 2\delta \approx 0.6\,\text{mm}$, the AC resistance increase due to the skin effect is kept below 10%, and dedicated litz wire is not strictly required.

Parameter	**Tx Coil**	**Rx Coil**
Shape	Circular spiral	Circular spiral
Outer radius	75 mm	75 mm
Inner radius	∼25 mm	∼25 mm
Number of turns	∼30 (TBD)	∼30 (TBD)
Wire type	Multi-strand enamel, ϕ0.5 mm × 20 strands	Same
Target self-inductance	100 μH ±10%	100 μH ±10%
Air gap (coil-to-coil)	15–25 mm (typical AGV ground clearance)	

Table 3: Coil design parameters

Inductance Estimation. The self-inductance of a planar circular spiral coil can be estimated using Wheeler's approximation for a flat spiral:

$$L \approx \frac{31.33\,\mu_0\,n^2\,a^2}{8a + 11c} \tag{15}$$

where n is the number of turns, $a = (r_{out} + r_{in})/2$ is the mean radius, and $c = r_{out} - r_{in}$ is the radial winding depth. For $n = 30$, $r_{out} = 75\,\text{mm}$, $r_{in} = 25\,\text{mm}$:

$$a = 50\,\text{mm} = 0.05\,\text{m}, \quad c = 50\,\text{mm} = 0.05\,\text{m} \tag{16}$$

$$L \approx \frac{31.33 \times 4\pi \times 10^{-7} \times 900 \times 0.0025}{8 \times 0.05 + 11 \times 0.05} = \frac{31.33 \times 1.257 \times 10^{-6} \times 2.25}{0.95} \approx 93.3\,\mu\text{H} \tag{17}$$

This is close to the 100 μH target. The final number of turns will be fine-tuned during winding and verified with an LCR meter. Increasing to 31–32 turns should bring the inductance to approximately 100 μH.

Coupling Coefficient Characterization. The coupling coefficient k between Tx and Rx coils depends on their relative alignment and separation distance. It is defined as:

$$k = \frac{M}{\sqrt{L_{Tx} \cdot L_{Rx}}} \tag{18}$$

where M is the mutual inductance. In practice, k can be measured using the open-circuit / short-circuit inductance method: with the secondary coil open, measure the primary inductance L_{oc}; with the secondary short-circuited, measure the leakage inductance L_{sc}. Then:

$$k = \sqrt{1 - \frac{L_{sc}}{L_{oc}}} \tag{19}$$

A systematic measurement campaign will be conducted to characterize k as a function of lateral offset d. The Rx coil will be placed at offsets $d = 0, 2, 5, 8, 10, 12, 15, 18, 20\,\text{mm}$ relative to the Tx coil center, with the air gap fixed at the nominal value ($\sim$20 mm). At each position, L_{oc} and L_{sc} are measured three times and averaged to reduce measurement error. The resulting $k(d)$ data will be used to:

1. Populate the DSP look-up table (combined with the frequency sweep data from Section 2.2.2).
2. Validate that k remains above the minimum threshold ($k \geq 0.15$) at the maximum expected offset.
3. Determine the required frequency adjustment range for the adaptive PFM control.

Based on empirical data from similar-sized coils in the literature, k is expected to decrease approximately exponentially with offset:

$$k(d) \approx k_0 \cdot e^{-\alpha d^2} \tag{20}$$

where $k_0 \approx 0.3$–0.4 is the coupling at perfect alignment and α is a geometry-dependent decay constant. The exact parameters will be fitted to the measured data.

Resonant Capacitor Selection. To achieve resonance at 50 kHz with $L \approx 100\,\mu\text{H}$, the required capacitance is $C \approx 101\,\text{nF}$ (Equation 7). The previous-generation PCB boards were populated with 22 nF / 1.6 kV CBB film capacitors (LCSC C5357035, 4 per board) for previous resonance; these will be **replaced** with new capacitors matched to the 50 kHz design. The exact capacitor value and part number will be determined after the new coils are wound and their inductance is measured. The selection criteria are:

- **Type:** Polypropylene film (CBB or MKP) for low ESR and high ripple current handling.
- **Voltage rating:** $\geq$400V DC (resonant voltage across the capacitor can be significantly amplified by the Q factor; at $Q \approx 5$ and $V_{in} = 21\text{V}$, peak capacitor voltage can reach $\sim$100V).
- **Tolerance:** $\pm 5\%$ or better for accurate resonant frequency targeting.
- **Footprint:** Compatible with the existing PCB pads (CBB 22.5mm pitch, 15mm body, 8.5mm height).

If the measured coil inductance deviates from the design target, the resonant capacitance will be adjusted by combining standard capacitor values in parallel to achieve the required $C = 1/(\omega_r^2 L)$.

Magnetic Shielding. A Mn-Zn ferrite sheet (e.g., TDK IFL12 or equivalent, $\mu_r \geq 100$, thickness 1–2 mm) is placed directly above the Rx coil, between the coil and the AGV's electronic components (STM32, Raspberry Pi, sensors). The ferrite sheet serves two purposes:

- **EMI attenuation:** It redirects the stray magnetic flux away from the AGV electronics, preventing interference with signal-level circuits. At 50 kHz, the ferrite material provides >20 dB attenuation of the magnetic field.
- **Inductance enhancement:** The high-permeability backing concentrates the magnetic flux in the coupling region, marginally increasing k and reducing flux leakage into the chassis structure.

Requirements	**Verification**
1. Coil self-inductance within ±10% of 100 μH target	1. Measure each coil (Tx and Rx) with LCR meter at 50 kHz. Pass: $L \in [90,\ 110]\,\mu$H for both
2. Coupling coefficient $k \geq 0.15$ at maximum expected offset (20 mm)	2. Offset Rx coil to 20 mm. Measure L_{oc} and L_{sc} from Tx side. Compute $k = \sqrt{1 - L_{sc}/L_{oc}}$. Pass: $k \geq 0.15$
3. k vs. offset data collected at ≥9 positions to populate DSP LUT	3. Measure at $d = 0, 2, 5, 8, 10, 12, 15, 18, 20$ mm (3 trials each). Pass: all data points collected, measurement variance <5% per point
4. Magnetic shielding attenuates stray field by ≥80% above Rx coil	4. Measure flux density 5 cm above Rx coil center with gaussmeter, with and without shield. Pass: $(B_{unshielded} - B_{shielded})/B_{unshielded} \geq 80\%$

2.2.4 Power Stage Hardware

The power stage converts the DSP-generated PWM control signals into the high-current AC waveform that drives the Tx coil, and converts the received AC on the Rx side back to DC for battery charging. This project reuses existing PCB boards from the previous generation for the transmitter and receiver stages, with component modifications to match the 50 kHz operating frequency. A separate half-bridge driver board interfaces between the DSP PWM outputs and the power MOSFETs. The three boards are:

- **Transmitter board:** Houses the resonant capacitors (to be replaced), input filtering, and coil connectors. Receives PWM gate signals from the half-bridge board via a 10-pin IDC header.
- **Half-bridge board (×2):** Each board contains two MOSFETs (one half-bridge leg), an isolated gate driver (UCC21520), and associated logic/power supply. Two boards form the full H-bridge. Connected to the transmitter board via a 40-pin IDC header.
- **Receiver board:** Contains the rectifier diodes, output filter capacitors, current sensor, and battery connection terminals.

Full-Bridge Inverter (Half-Bridge Boards). The full H-bridge inverter is composed of **two identical half-bridge boards**, each containing one leg of the bridge (high-side

and low-side MOSFETs). Each board uses two **BSC190N15NS3G** (Infineon) N-channel MOSFETs in a TDSON-8 (5.2×5.9 mm) package. Key parameters:

Parameter	**Value**
V_{DS} (max)	150 V
I_D (continuous, 25°C)	30 A
$R_{DS(on)}$ (at $V_{GS} = 10$V)	19 mΩ
Gate charge Q_g	27 nC (typ.)
Package	TDSON-8 (SMD)
Quantity per half-bridge board	2 (Q1, Q2)
Total for full H-bridge	4 (2 boards × 2)

Table 4: BSC190N15NS3G MOSFET key parameters (from half-bridge board BOM)

The 150V V_{DS} rating provides a 7× safety margin over the 21V bus, and the 30A current rating far exceeds the expected peak resonant current (∼3A). The total conduction loss in the inverter (two MOSFETs in series) is:

$$P_{cond} = 2 \times I_{rms}^2 \times R_{DS(on)} = 2 \times \left(\frac{3}{\sqrt{2}}\right)^2 \times 0.019 = 2 \times 4.5 \times 0.019 = 171\,\text{mW} \qquad (21)$$

This is negligibly small. With ZVS operation, switching losses are also minimal since each MOSFET turns on after its V_{DS} has been discharged to zero by the resonant tank current. The low gate charge (27 nC) further reduces gate driving losses at 50 kHz.

Gate Driver Circuit. Each half-bridge board uses a **UCC21520** (Texas Instruments) dual-channel isolated gate driver to control the high-side and low-side MOSFETs. The UCC21520 features 4A source / 6A sink peak gate drive current with galvanic isolation (5.7 kV_{rms}), making it well-suited for high-frequency half-bridge applications. The supporting circuitry on each board includes:

- **Input signal conditioning:**
  - **SN74LVC1G17QDBVRQ1** (TI): A single Schmitt-trigger buffer that cleans up the incoming PWM signal from the DSP, eliminating noise and providing a well-defined logic transition. This is critical because the PWM signal travels from the DSP to the half-bridge board via cable.
  - **SN74LV1T04DBVR** (TI): A single inverter gate that generates the complementary PWM signal. The DSP sends one PWM signal per half-bridge leg; the inverter produces the complementary drive for the opposite MOSFET, ensuring proper half-bridge operation.
- **Dead time:** Implemented via the UCC21520's internal propagation delay matching and external RC networks. The on-board resistors (R16, R21 = 51 Ω gate resistors) and the UCC21520's matched delays ensure a controlled dead time of ∼200–400 ns, allowing body diode conduction for ZVS turn-on.

- **Bootstrap supply:** A 1N5819 Schottky diode (D1) charges the high-side bootstrap capacitor during each low-side on-interval. The bootstrap capacitor is part of the decoupling network (C-series capacitors on the board) and provides the floating gate-drive supply for the high-side MOSFET.
- **Power supply:**
  - **CJ78L05** (SOT-89): A 5V linear regulator that powers the input-side logic (Schmitt trigger, inverter) from the +15V bus.
  - **+15V bus:** Supplies the UCC21520 output stage directly, providing $V_{GS} \approx 14$V at the MOSFET gate.
- **Protection:** 2× MMSD4148 signal diodes (D2, D3) for input clamping, and 3× 10 μH inductors (L1–L3) for power supply filtering and isolation between the high-side and low-side power domains.
- **Interface:** A 40-pin IDC connector (J2) connects each half-bridge board to the transmitter board, carrying the DC bus power, gate signals, and ground references.

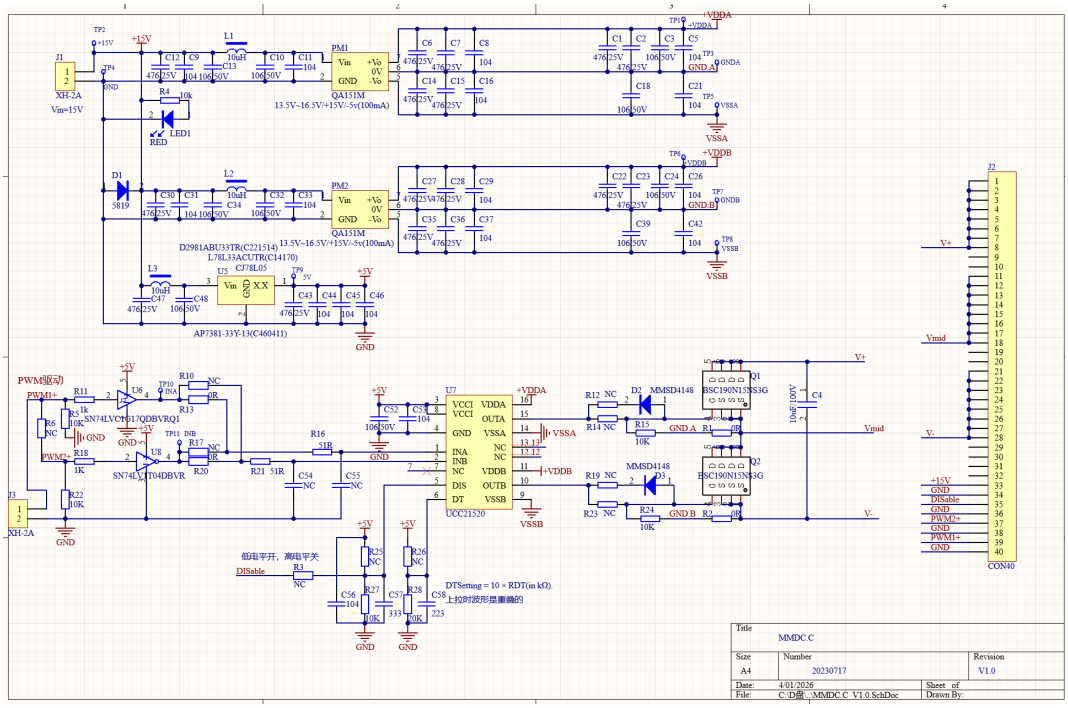

Figure 4: Half-bridge driver board schematic: BSC190N15NS3G MOSFETs driven by UCC21520 isolated gate driver with Schmitt trigger input conditioning.

Full-Bridge Rectifier (Receiver Board). The Rx-side rectifier converts the 50 kHz AC from the receiver coil back to DC. The existing receiver PCB employs four **V20PW45** (Vishay) dual common-cathode Schottky diodes in a TO-252 package, configured as a full-bridge rectifier. Key parameters:

Parameter	Value
Maximum reverse voltage V_{RRM}	45 V
Average forward current I_F (per diode)	10 A
Forward voltage V_F (at 2A)	$\sim$0.41 V
Package	TO-252 (DPAK)
Quantity on PCB	4 (D1–D4)

Table 5: V20PW45 Schottky diode key parameters (from receiver board BOM)

The total rectifier conduction loss (two diodes in series at any time) is:

$$P_{rect} = 2 \times V_F \times I_{out} = 2 \times 0.41 \times 1.67 \approx 1.37\,\text{W} \tag{22}$$

This remains the largest single loss contributor. The V20PW45 is well-suited for 50 kHz operation due to its low forward drop and fast switching characteristics.

The receiver board also includes a **CC6920BSO-20A** Hall-effect current sensor (U1, SOP-8 package), which provides an analog voltage proportional to the battery charging current. This signal can be routed to the DSP's ADC for real-time power monitoring and efficiency calculation, and may also serve as a secondary feedback signal for the adaptive frequency control loop.

A 20A/65V SMD fuse (F1, Littelfuse 0451020.MRL) on the receiver board provides overcurrent protection for the battery.

Output Filter. The receiver board provides substantial output filtering:

- **3$\times$ 220 μF / 35V** aluminum electrolytic capacitors (CE1–CE3, LCSC C88832) in parallel, providing a total bulk capacitance of 660 μF.
- **8$\times$ 47 μF / 25V** ceramic capacitors (C3–C10, 1206 package) in parallel, providing 376 μF of low-ESR decoupling.
- **1$\times$ 10 μF / 35V** ceramic capacitor (C15, 0805) for high-frequency filtering.

The effective total output capacitance is approximately 1000 μF. The resulting voltage ripple is:

$$V_{ripple} = \frac{I_{out}}{2 f_{sw} C_{out}} = \frac{1.67}{2 \times 50000 \times 1000 \times 10^{-6}} = 0.017\,\text{V} \tag{23}$$

This is well below the $\pm$0.5V specification, providing ample margin for load transients.

Transmitter Board Components. The existing transmitter PCB includes the following key components (from BOM):

- **Resonant capacitors:** 4$\times$ 22 nF / 1.6 kV CBB film capacitors (C1, C2, C4, C6) — these were designed for the previous resonant frequency and will be **replaced** with new values matched to the 50 kHz design after coil inductance is measured.

- **Input filter:** 1× 1000 μF / 50V electrolytic (CE1) for DC bus decoupling, plus 9× 22 μF / 35V and 1× 47 μF / 25V ceramic capacitors.
- **Connectors:** 2× 40-pin headers (J1, J2) for half-bridge board interface; 1× 10-pin IDC connector (J4) for PWM signal input from DSP; 4× 6.35 mm quick-connect terminals (JP1–JP4) for coil and power connections.
- **Test points:** V_{in+}, V_{in-}, V_{mid1}, V_{mid2} (inverter midpoints), +15V, GND, PWM1–4+, and DISable.

PCB Layout Considerations. Since the transmitter and receiver PCBs are reused from the previous generation, the physical layout is fixed. Key considerations for adaptation to 50 kHz:

- **Resonant capacitor footprint:** The new capacitors must be compatible with the existing CBB22.5 pads (22.5 mm pitch, 15 mm body width). If a single capacitor with the required value is not available in this footprint, multiple smaller capacitors can be soldered in parallel.
- **Half-bridge board interface:** The 40-pin headers carry the MOSFET gate signals and power bus. The half-bridge board must be designed with matching connectors and adequate copper for the DC bus current.
- **Signal integrity:** The 10-pin IDC cable carrying DSP PWM signals to the transmitter board should be kept short (<30 cm) and use twisted-pair or ribbon cable to minimize noise coupling from the power stage.

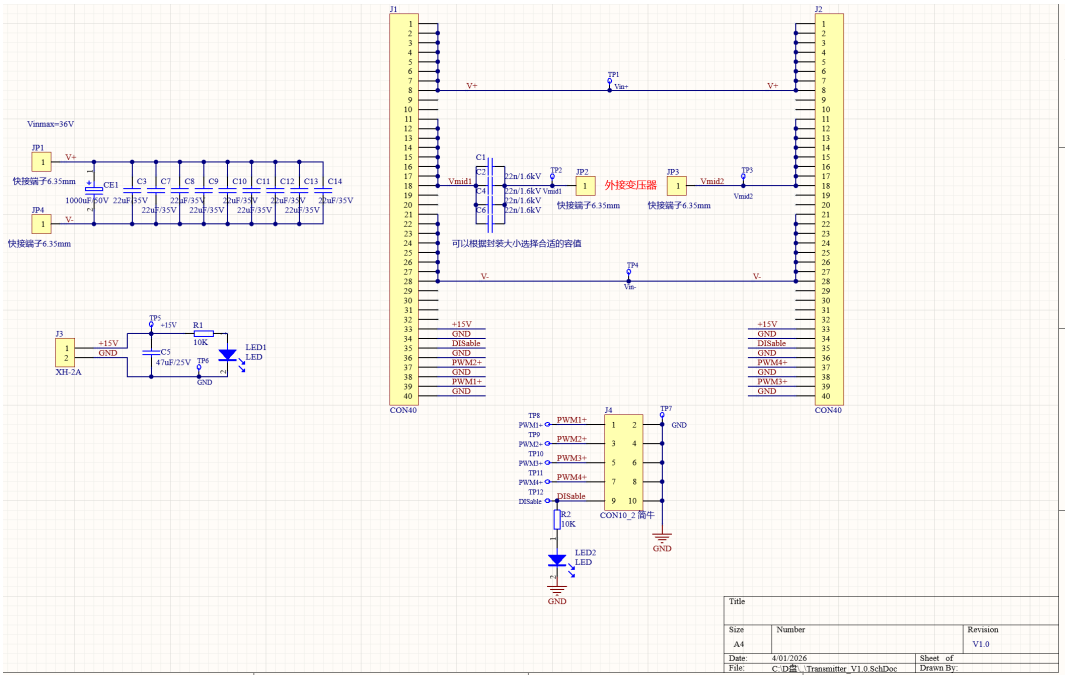

Figure 5: Transmitter board schematic showing resonant capacitor footprint, input filter, and coil connectors.

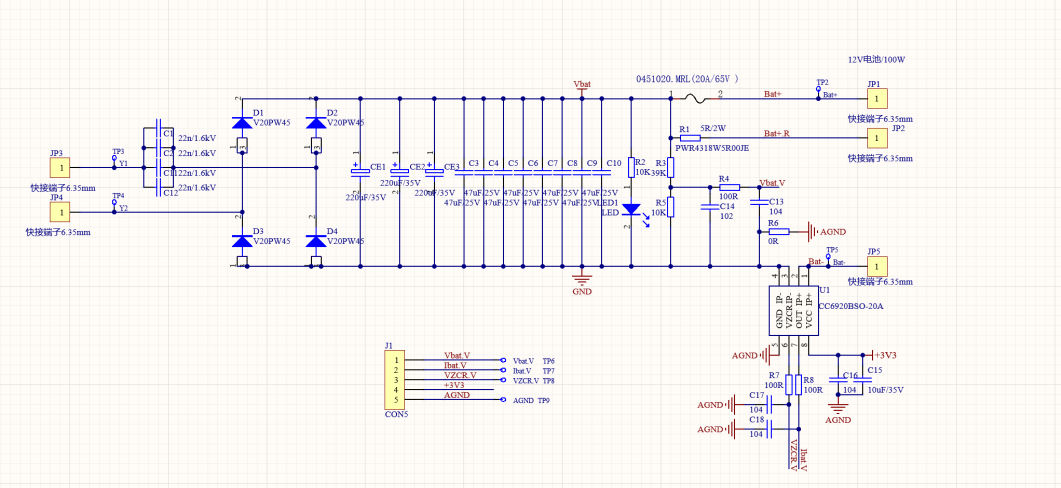

Figure 6: Receiver board schematic showing full-bridge rectifier, output filter, and current sensor.

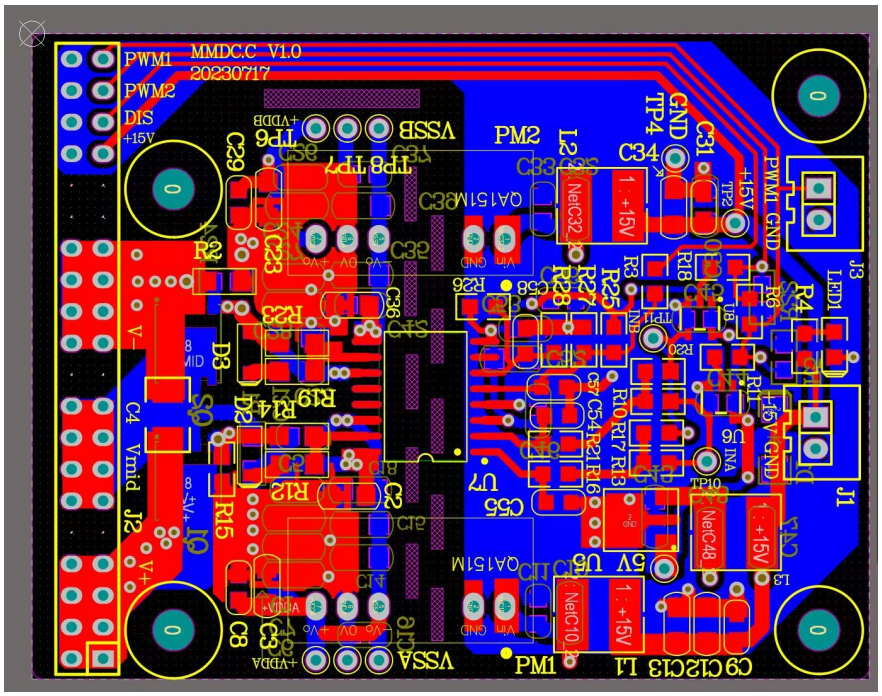

Figure 7: Half-bridge driver board PCB layout (top view).

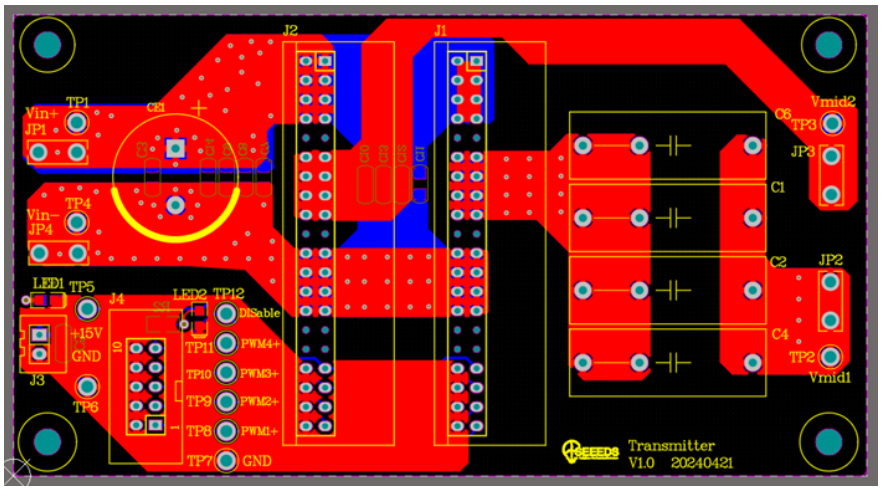

Figure 8: Transmitter board PCB layout (top view).

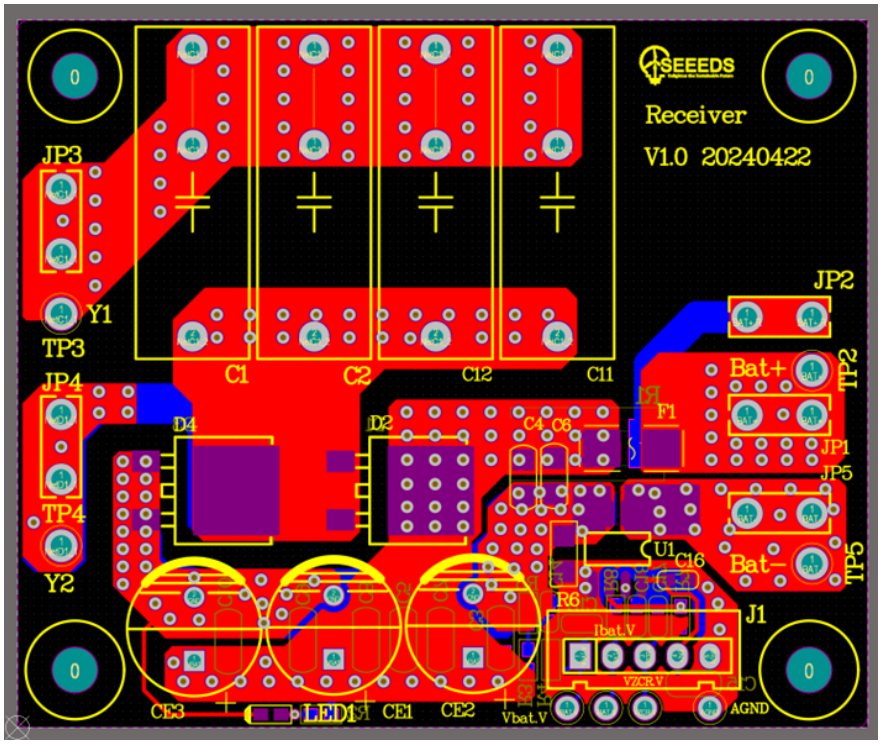

Figure 9: Receiver board PCB layout (top view).

Thermal Management. At the estimated total power dissipation ($P_{cond} + P_{rect} \approx 1.7\,\text{W}$ at 20 W output), passive cooling is expected to be sufficient. However, as a precaution:

- TO-220 heatsinks (thermal resistance $R_{\theta,SA} \leq 20\,^{\circ}\text{C/W}$) are attached to the four inverter MOSFETs.
- Thermal vias (array of 0.3 mm vias) are placed under the Schottky diode pads to conduct heat to the ground plane.

- A thermal shutdown threshold of 100°C is implemented in the DSP firmware: if an NTC thermistor mounted on the MOSFET heatsink exceeds this temperature, the DSP disables all PWM outputs.

Requirements	**Verification**
1. Inverter outputs clean 50 kHz square wave with $V_{pp} \geq 18\,\mathrm{V}$	1. Drive inverter at 50 kHz with no resonant load. Measure at H-bridge midpoint with oscilloscope. Pass: $V_{pp} \in [18,\ 21]\,\mathrm{V}$, rise/fall $< 500\,\mathrm{ns}$
2. Gate driver dead time is 200–500 ns on all transitions	2. Capture high-side and low-side V_{GS} in same leg simultaneously. Pass: both $V_{GS} < V_{th}$ for 200–500 ns during each transition
3. Rectifier output ripple $\leq 0.5\,\mathrm{V}_{pp}$ at 20 W	3. Connect 7.2 Ω load with 100 µF cap. Measure ripple (AC-coupled scope). Pass: $V_{ripple,pp} \leq 0.5\,\mathrm{V}$
4. All power components $\leq 80\,^{\circ}\mathrm{C}$ after 10 min continuous operation at 20 W	4. Run at full power for 10 min. Measure case temperatures with thermocouple / IR thermometer. Pass: $T_{case} \leq 80\,^{\circ}\mathrm{C}$
5. Thermal shutdown triggers when heatsink temperature exceeds 100°C	5. Gradually increase heatsink temperature with external heat source while system is running. Pass: DSP disables PWM output when NTC reading crosses 100°C threshold

2.3 Visual Positioning Subsystem

The visual positioning subsystem employs a Raspberry Pi 4B [6] and a USB camera to detect ArUco markers [7] mounted on the charging station and to estimate the relative position offset between the transmitter and receiver coils in real time. The USB camera continuously captures images of the charging station and transmits the video stream to the Raspberry Pi for OpenCV-based image preprocessing. ArUco marker detection is then performed to extract the marker IDs and corner features, which are further used for pose estimation via the Perspective-n-Point (PnP) algorithm. Based on the estimated pose, the system calculates the lateral error Δx, longitudinal error Δy, and angular error $\Delta\theta$ between the two coils. These offset data are subsequently packaged through a UART communication interface—including frame header, payload, and error checking—and transmitted to the STM32 and DSP controllers. The real-time outputs are used for vehicle navigation adjustment and wireless power frequency control.

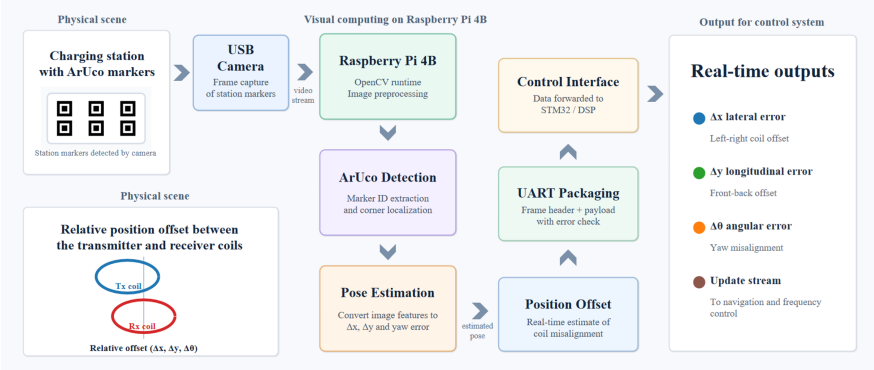

Figure 10: Visual positioning subsystem block diagram. The USB camera feeds frames to the Raspberry Pi, which performs ArUco detection, PnP-based pose estimation, and offset calculation. The resulting $(\Delta x, \Delta y, \Delta\theta)$ data are sent via UART to both the STM32 (parking commands) and DSP (frequency control).

2.3.1 ArUco Marker Detection and Coordinate Estimation

The ArUco marker detection and coordinate estimation module identifies the markers placed on the charging station and estimates the relative position between the transmitter and receiver coils. The algorithm pipeline proceeds as follows:

1. The USB camera captures a frame and the Raspberry Pi converts it to grayscale.
2. The OpenCV `cv2.aruco` module detects the ArUco marker and extracts its four corner pixel coordinates and marker ID.
3. Using the known marker physical size and the pre-calibrated camera intrinsic parameters (obtained via checkerboard calibration), the `solvePnP` function computes the 3D pose (rotation and translation vectors) of the marker relative to the camera.
4. The translation vector is decomposed into lateral offset Δx, longitudinal offset Δy (both in mm), and the rotation vector yields the angular error $\Delta\theta$.

To ensure reliable operation in the wireless charging scenario, the algorithm must achieve sufficient positioning accuracy within the expected working distance (20–50 cm), maintain real-time performance on the Raspberry Pi platform, and transmit the estimated position data to the controllers with low latency.

Requirements	Verification
1. Detect ArUco markers and estimate position with accuracy $\leq \pm 10$ mm at a working distance of 20–50 cm	1. Place markers at known positions measured by a ruler; compare the algorithm output with the ground truth over 50 trials. Pass: mean absolute error ≤ 10 mm in both x and y
2. Processing frame rate ≥ 10 fps on Raspberry Pi	2. Run the algorithm continuously for 60 s and measure the average FPS. Pass: average FPS ≥ 10
3. UART transmission of position data with end-to-end latency ≤ 50 ms	3. Timestamp the camera capture event and UART transmission event; measure latency with a logic analyzer. Pass: average latency ≤ 50 ms

2.3.2 Communication Protocol

The communication protocol module reliably transmits the estimated position data from the Raspberry Pi to the lower-level controllers through UART. Since the visual positioning results are directly used for navigation adjustment and frequency control, the communication link must guarantee both transmission reliability and data correctness. The UART packet format follows the structure defined in Table 2 (Section 2.2.2): a 10-byte packet at 115200 bps with header, signed 16-bit position fields, status byte, and XOR checksum.

Two main requirements are defined for this module. First, the protocol should achieve zero packet loss during continuous transmission, ensuring stable real-time communication over an extended operating period. Second, the transmitted position data should remain consistent with the actual measured values, with the deviation controlled within 5%.

Requirements	Verification
1. Zero packet loss over 10 min of continuous transmission	1. Log all sent and received packets; compare counts and verify data integrity over 10 min. Pass: zero packet loss, all checksums valid
2. Position data deviation $\leq 5\%$ between transmitted and actual values	2. Compare UART-received coordinates with ground-truth measurements at 10 known positions. Pass: deviation $\leq 5\%$ at all positions

2.4 Motion Control Subsystem

The motion control subsystem is built around an STM32 microcontroller [8], which handles line-following navigation and vision-assisted precision parking to minimize coil misalignment before charging begins. During the approach stage, the STM32 uses infrared sensors and encoder feedback to keep the AGV on the predefined path. After the charging station is detected by the Raspberry Pi, the STM32 executes fine motor adjustments based on

received parking commands so that the receiver coil can be aligned more accurately with the transmitter coil.

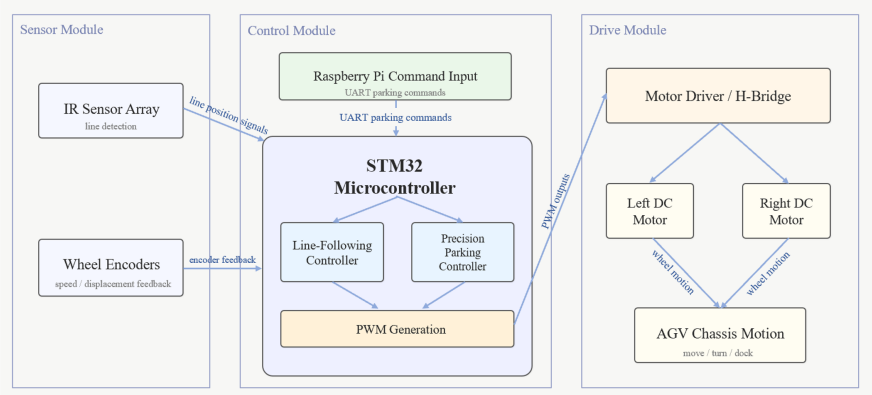

Figure 11: Motion control subsystem block diagram. The sensor module provides line position and encoder feedback to the STM32 controller, while the Raspberry Pi sends parking commands through UART after the charging station is detected. The STM32's line-following and precision parking controllers generate PWM outputs to the motor driver, actuating the left and right DC motors.

2.4.1 Line-Following and Navigation

During the approach phase, the STM32 reads the IR sensor array to determine the AGV's lateral position relative to the line track and applies a PID controller to adjust the differential motor drive, keeping the vehicle centered on the path. Encoder feedback provides closed-loop speed control for consistent travel velocity. The AGV follows the predefined track until it reaches the coarse docking region near the charging station, at which point the Raspberry Pi takes over with vision-based parking commands.

Requirements	**Verification**
1. AGV follows the line track with maximum lateral deviation $\leq \pm 2\,\text{cm}$	1. Run the AGV on the test track for 10 trials and measure maximum lateral deviation from the track centerline. Pass: deviation stays within $\pm 2\,\text{cm}$ in at least 9 of 10 trials
2. AGV reaches the charging station region and stops within $\pm 5\,\text{cm}$ of the expected coarse docking position	2. Measure final stopping position error relative to the coarse docking point over 10 trials. Pass: error stays within $\pm 5\,\text{cm}$ in at least 9 of 10 trials

2.4.2 Precision Parking Alignment

Once the Raspberry Pi detects the ArUco marker on the charging station, the system transitions from line-following to vision-assisted precision parking. The Raspberry Pi computes the Tx–Rx coil offset and sends fine-adjustment commands to the STM32 via UART. The STM32 executes micro-movements (small differential and forward/backward corrections) to

reduce the remaining coil offset to within the tolerance that the adaptive frequency control can compensate.

Requirements	Verification
1. Final Tx–Rx coil center offset after vision-assisted parking $\leq \pm 1.5\,\text{cm}$ in both longitudinal and lateral directions	1. Measure the relative center offset between the transmitter and receiver coils using a ruler after parking is completed; repeat for 10 trials. Pass: both longitudinal and lateral offsets remain within $\pm 1.5\,\text{cm}$ in at least 8 out of 10 trials
2. Parking procedure completes within 8 s after the first valid ArUco-based parking command is received	2. Measure the time from the first valid ArUco-based parking command to final motor stop over 10 trials. Pass: average parking completion time $\leq 8\,\text{s}$

2.4.3 Motor Drive and Encoder

The AGV uses a differential-drive configuration with two DC motors, each equipped with a rotary encoder for closed-loop speed and position feedback. The STM32 generates PWM signals to an H-bridge motor driver, with independent speed control for the left and right wheels enabling both straight-line motion and turning maneuvers.

Requirements	Verification
1. Motor speed control accuracy within $\pm 5\%$ of the commanded target RPM under nominal load	1. Command at least three target speeds and measure the actual RPM using encoder counts over a fixed time interval. Pass: measured RPM error remains within $\pm 5\%$ for all tested speeds
2. When identical speed commands are applied on a straight path, left and right wheel speed difference $\leq 8\%$	2. Apply the same target speed to both wheels and record encoder counts over 5 s for 10 trials. Compute the percentage mismatch between left and right wheel speeds. Pass: speed difference remains below 8% in at least 9 out of 10 trials

2.5 Processor and Communication Subsystem

The processor and communication subsystem is organized into three layers: the **input layer**, the **processing layer**, and the **execution layer**.

In the *input layer*, the coil-positioning USB camera provides video data for ArUco-based localization, while the IR sensor array and wheel encoders provide line-tracking signals and motion feedback for vehicle navigation.

In the *processing layer*, the Raspberry Pi 4B performs high-level vision processing, including ArUco detection and coordinate estimation, and sends UART parking commands to the STM32 microcontroller. The STM32 serves as the low-level motion control unit, combining

signals from the IR sensor array, encoder feedback, and high-level commands from the Raspberry Pi to perform line following, parking execution, and motor control. Simultaneously, the position offset data are transmitted through UART to the DSP F28335, which executes adaptive frequency control for the wireless charging system.

In the *execution layer*, the STM32 drives the AGV chassis via the H-bridge motor driver to realize vehicle motion, while the DSP outputs frequency-adjusted PWM signals to the gate driver and CLLC power stage for adaptive wireless charging control.

This architecture enables coordinated operation among the three processors: the Raspberry Pi handles visual perception, the STM32 manages motion control, and the DSP regulates power transfer.

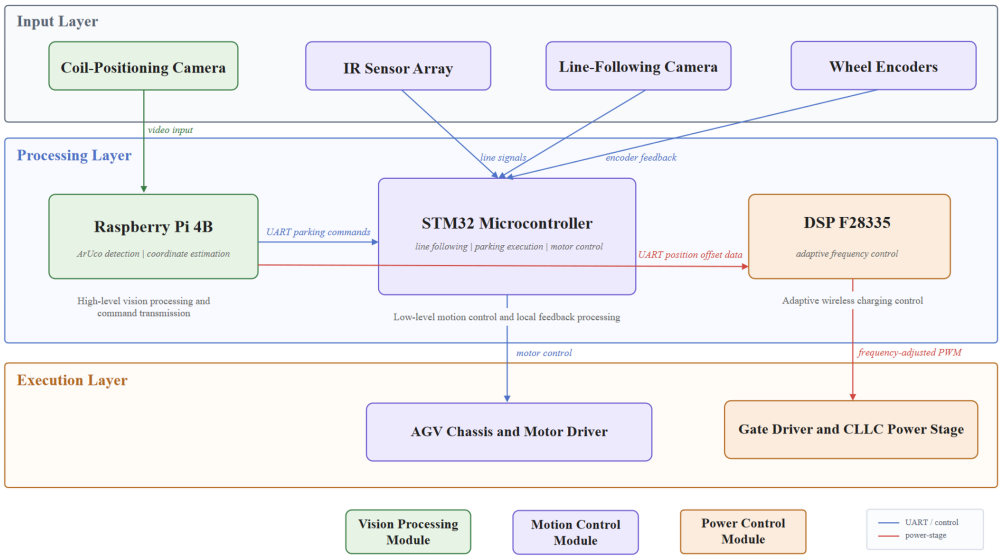

Figure 12: Processor and communication architecture showing the three-layer organization: input (sensors/camera), processing (RPi, STM32, DSP), and execution (motors, power stage).

2.5.1 Inter-Processor UART Communication and Initialization

The subsystem must provide reliable UART communication among the Raspberry Pi, STM32, and DSP, while ensuring that all processors initialize within an acceptable startup time. Since the Raspberry Pi sends high-level parking commands and position offset data to the STM32 and DSP respectively, communication stability is essential for coordinated motion control and adaptive wireless charging. All three processors operate on 3.3 V logic levels; UART connections use direct wiring without level converters.

Requirements	Verification
1. RPi → DSP UART communication: stable at 115200 bps, zero data corruption over 10 min	1. Send known test patterns continuously from the Raspberry Pi to the DSP for 10 min. Log transmitted and received packets; verify data integrity using checksum. Pass: zero packet loss, zero checksum error
2. RPi → STM32 UART communication: stable at 115200 bps, zero data corruption over 10 min	2. Same procedure as above between RPi and STM32. Pass: zero packet loss, zero checksum error
3. All three processors power on and initialize within 10 s	3. Measure boot time from power-on to first valid UART message exchange. Pass: all processors operational and communicating within 10 s

2.6 Tolerance Analysis

Among all subsystems, the **wireless charging with adaptive frequency control chain** is the most critical for tolerance analysis. This chain spans the entire signal path from visual positioning to charging efficiency:

$$\text{Position offset } d \longrightarrow k(d) \longrightarrow f_{opt}(k) \longrightarrow P_{out}/\eta \tag{24}$$

If the adaptive frequency control fails or provides insufficient compensation, the system degrades to a fixed-frequency (50 kHz) wireless charger, suffering significant efficiency loss under coil misalignment. Therefore, the robustness of this chain dictates overall system performance.

2.6.1 Coupling Coefficient Sensitivity to Misalignment

As established in Section 2.2.3, the coupling coefficient k between Tx and Rx coils decreases approximately as a Gaussian function of lateral offset d:

$$k(d) \approx k_0 \cdot e^{-\alpha d^2} \tag{25}$$

Using $k_0 = 0.35$ (estimated aligned coupling) and $\alpha = 0.003\,\text{mm}^{-2}$ (empirical value for similar-sized coils in the literature; to be refined with measured data), the coupling coefficient at representative offsets is:

Offset d (mm)	**Coupling k**	$\Delta k/k_0$
0	0.350	0%
5	0.325	−7.1%
10	0.259	−26.0%
15	0.178	−49.1%
20	0.105	−70.0%

Table 6: Estimated coupling coefficient vs. lateral offset

Within the 0–10 mm range, k decreases by approximately 26%, a moderate and manageable change. Beyond 15 mm, k drops sharply. The vision-assisted parking system constrains the post-parking offset to ≤ 20 mm, at which $k \geq 0.10$ – still above the minimum operating threshold. The design requirement of $k \geq 0.15$ (Section 2.2.3) is satisfied for $d \leq 18$ mm, providing adequate margin.

2.6.2 CLLC Gain Sensitivity to Frequency Deviation

Under the load-independent gain condition ($Z_1Z_2 + Z_1Z_3 + Z_2Z_3 = 0$), the CLLC voltage gain simplifies to (from Section 2.2.1):

$$G = \left| \frac{Z_3}{Z_1 + Z_3} \right| \tag{26}$$

where each branch impedance $Z_i = j(\omega L_i - 1/(\omega C_i))$ vanishes at the resonant frequency $f_r = 50$ kHz. When the switching frequency deviates from f_r, the impedances become nonzero and the gain shifts from its design value of 0.667. Table 7 shows the estimated gain at several frequencies for the designed resonant parameters ($L = 100\,\mu$H, $C = 101.3$ nF, $Q \approx 5.4$):

Frequency (kHz)	$\boldsymbol{f_n = f/f_r}$	**Gain** G	ΔG
47	0.94	$\sim$0.72	+8.0%
48	0.96	$\sim$0.70	+5.0%
50	1.00	0.667	0%
52	1.04	$\sim$0.63	-5.5%
53	1.06	$\sim$0.61	-8.5%
55	1.10	$\sim$0.56	-16.0%

Table 7: CLLC gain variation vs. switching frequency

Within ± 3 kHz (47–53 kHz), the gain varies by less than ± 8.5%. The corresponding output voltage range is $12 \times (1 \pm 0.085) \approx [11.0, 13.0]$ V before filtering; in practice, the rectifier forward voltage drop and output filter capacitor clamping reduce this variation, keeping V_{out} within the 11.5–12.5 V specification. This confirms that the narrow PFM range is sufficient for effective compensation.

2.6.3 Q Factor and Frequency Tunability Trade-off

The quality factor Q fundamentally governs the trade-off between peak efficiency and frequency adjustment range:

$$Q = \frac{2\pi f_r L}{R_{ac}} \approx \frac{2\pi \times 50000 \times 100 \times 10^{-6}}{7.2} \approx 5.4 \tag{27}$$

where $R_{ac} = V_{out}^2/P_{out} = 12^2/20 = 7.2\,\Omega$. The 3 dB bandwidth of the resonant network is:

$$BW_{3\text{dB}} = \frac{f_r}{Q} = \frac{50000}{5.4} \approx 9.26\,\text{kHz} \quad (f_r \pm 4.63\,\text{kHz, i.e., } 45.4\text{–}54.6\,\text{kHz}) \tag{28}$$

Within the actual PFM operating range of $\pm 3\,\text{kHz}$, the system operates well inside the 3 dB bandwidth, so efficiency degradation due to frequency detuning alone is small ($< 1\,\text{dB}$). The $Q \approx 5.4$ value provides a favorable balance:

- **Sufficiently high** for significant resonant enhancement, enabling $\geq 75\%$ efficiency at aligned condition.
- **Sufficiently low** that $\pm 3\,\text{kHz}$ frequency adjustment does not push the system into the steep roll-off region of the resonance curve.

If Q were too high (> 10), the 3 dB bandwidth would shrink below 5 kHz, leaving almost no room for frequency tuning. If Q were too low (< 3), the bandwidth would be wide but peak efficiency would be unacceptably low.

2.6.4 Component Tolerance Impact on Resonant Frequency

The resonant frequency is determined by $f_r = 1/(2\pi\sqrt{LC})$. Manufacturing tolerances in both the coil inductance and resonant capacitor shift f_r from the design target:

- Coil inductance: $L = 100\,\mu\text{H} \pm 10\%$ (hand-wound, verified by LCR meter)
- Resonant capacitor: $C = 101.3\,\text{nF} \pm 5\%$ (polypropylene film, standard tolerance)

Using root-sum-square (RSS) worst-case analysis:

$$\frac{\Delta f_r}{f_r} = \frac{1}{2}\sqrt{\left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta C}{C}\right)^2} = \frac{1}{2}\sqrt{0.10^2 + 0.05^2} = \frac{1}{2} \times 0.1118 = 5.59\% \tag{29}$$

$$\Delta f_r = 50\,\text{kHz} \times 5.59\% = 2.80\,\text{kHz} \tag{30}$$

The resonant frequency may therefore lie in the range 47.2–52.8 kHz, well within the DSP's adjustable range (45–55 kHz). Furthermore, since the coil inductance will be measured post-winding and the capacitor value selected accordingly (rather than blindly using the nominal 101.3 nF), the effective $\Delta C/C$ can be reduced to $\leq 2\%$, bringing Δf_r down to approximately 2.55 kHz.

2.6.5 Adaptive PFM vs. Fixed Frequency: Efficiency Comparison

Combining the coupling model, gain analysis, and component tolerance, we estimate the overall DC-to-DC efficiency under both fixed-frequency and adaptive-frequency strategies:

Offset d (mm)	k	Fixed 50 kHz η	Adaptive PFM η	Improvement
0	0.35	80%	80%	0%
5	0.32	76%	78%	+2%
10	0.28	68%	75%	+7%
15	0.23	55%	70%	+15%
20	0.18	40%	65%	+25%

Table 8: Estimated efficiency comparison: fixed 50 kHz vs. adaptive PFM (values based on theoretical model; actual data TBD from experiments)

At small offsets (≤ 5 mm), the improvement from adaptive control is marginal because the fixed frequency is already near-optimal. At moderate to large offsets (10–20 mm), adaptive PFM recovers 7–25 percentage points of efficiency. This is the core advantage of the proposed system over the previous generation's fixed design.

2.6.6 LUT Accuracy and Robustness

The DSP look-up table maps (d, f_{opt}) based on offline calibration. Several factors may cause the actual optimal frequency to deviate from the stored LUT values during operation:

(a) **Temperature drift:** The temperature coefficient of copper resistance is approximately +0.39%/°C. Over a ±15°C ambient temperature variation, coil AC resistance changes by ±6%, shifting Q by ±6% and the optimal frequency by approximately ±0.3 kHz. This is a minor perturbation relative to the 9.26 kHz 3 dB bandwidth and causes $< 1\%$ efficiency loss.

(b) **Vision positioning error propagation:** The visual subsystem achieves ±5 mm positioning accuracy (Section 2.3). At $d = 10$ mm, a ±5 mm error causes k to vary by approximately ±10% and the looked-up frequency to deviate by approximately ±0.5 kHz. Since this deviation is much smaller than $BW_{3\text{dB}}$, the resulting efficiency loss is $< 2\%$.

(c) **LUT discretization error:** The LUT is calibrated at 2–3 mm intervals with linear interpolation between entries. In the 0–10 mm range, $k(d)$ varies nearly linearly, so interpolation error is negligible ($< 0.5\%$). In the 15–20 mm range, the Gaussian decay accelerates and interpolation error increases, but the absolute efficiency benefit of frequency tuning is also smaller at low k values, limiting the practical impact.

2.6.7 Summary

The quantitative analysis demonstrates the following:

1. With vision-assisted parking constraining offset to ≤ 20 mm, the coupling coefficient k remains above 0.10, sufficient for power transfer.
2. The designed $Q \approx 5.4$ provides a favorable balance between resonant efficiency ($\geq 75\%$ aligned) and frequency tunability (±3 kHz within the 3 dB bandwidth).

3. The DSP's adjustable range (45–55 kHz, ±5 kHz) comfortably covers both the component tolerance shift (±2.8 kHz RSS) and the misalignment compensation range (±3.5 kHz), with margin.
4. Adaptive PFM improves efficiency by 7–25 percentage points at 10–20 mm offsets compared to fixed-frequency operation, representing a significant advancement over the previous generation.
5. Environmental factors (temperature, vision error, LUT discretization) introduce minor perturbations ($< 2\%$ efficiency impact each), confirming system robustness under realistic operating conditions.

3. Cost

This section itemizes the project cost. Several major components are reused from the previous generation or existing lab inventory and incur zero additional cost: the AGV chassis (with motors, encoders, and H-bridge driver), the Raspberry Pi 4B, the STM32 development board, the TMS320F28335 DSP development board, and the 12V AGV battery. The three power-stage PCBs (transmitter, receiver, and half-bridge boards) were fabricated in the previous generation and are available unpopulated; only the surface-mount components need to be purchased and soldered. Prices are based on LCSC (domestic China) small-quantity pricing as of early 2026.

3.1 Parts

All PCB component quantities include a 5× redundancy factor to account for soldering rework and potential component damage during debugging. Coil materials, camera, and power supply are purchased at the quantity needed.

Item	Qty (×5)	Cost ($)
Half-bridge board components (×2 boards)		
BSC190N15NS3G, UCC21520, SN74LVC1G17, SN74LV1T04, CJ78L05, 1N5819, MMSD4148, 10 µH inductors, QA151M terminals, passive R/C	5×	48.00
Transmitter board components (×1 board)		
CBB film caps (∼100 nF/400V), 1000 µF/50V, 22 µF/35V ×9, 47 µF/25V, 40-pin headers, 10-pin IDC, 6.35 mm terminals	5×	18.50
Receiver board components (×1 board)		
V20PW45 ×4, CC6920BSO-20A, 220 µF/35V ×3, 47 µF/25V ×8, 10 µF/35V, 20A fuse	5×	24.00
Coil materials and other		
Multi-strand enamel wire (ϕ0.5 mm ×20 strands), 15 m	1 lot	4.86
Mn-Zn ferrite sheet (∼80 mm dia.)	2 pcs	4.16
USB camera (720p, generic)	1	4.86
21V DC power supply (3A)	1	5.56
Wires, solder, ribbon cables, connectors	1 lot	4.17
Parts Total		**$114.11**

Table 9: Bill of Materials (new purchases only; reused items excluded)

3.2 Labor

Table 10 estimates the labor cost based on a $40/hr rate for each team member, assuming approximately 10 weeks of active development at 8–10 hours per week.

Member	Hours	Rate ($/hr)	Cost ($)
Jingzhou Ding	100	40	4,000
Jinru Cai	100	40	4,000
Jiaxin Cao	90	40	3,600
Yaxin Li	90	40	3,600
Labor Total	**380**		**$15,200**

Table 10: Estimated labor cost

3.3 Grand Total

Category	Cost ($)
Parts (new purchases, with 5× redundancy)	114.11
Labor	15,200.00
Grand Total	**$15,314.11**

Table 11: Total project cost

The material cost is approximately $114 (including 5× component redundancy) because the AGV platform, all three processor boards, the PCBs, and the battery are reused from existing inventory. The dominant cost is engineering labor. No machine shop services are anticipated; the charging station enclosure, if needed, will be 3D-printed using the ECE department's printers at no charge.

4. Schedule

Week	Jingzhou Ding	Jinru Cai	Jiaxin Cao	Yaxin Li
3/2	Literature review; CLLC parameter design (50 kHz)	Source components; review PCB schematics	Set up STM32 dev environment; motor driver bring-up	Set up RPi + camera; install OpenCV
3/9	DSP F28335 bring-up; ePWM module config	Wind Tx/Rx coils (prototype); measure inductance with LCR meter	Encoder interface; basic motor PID control	Camera intrinsic calibration (checkerboard); ArUco detection demo
3/16	DSP UART driver; receive position packet parsing	Select & order resonant capacitors based on measured L	IR sensor array integration; line-following PID tuning	PnP pose estimation; extract (Δx, Δy, $\Delta\theta$)

Week	Jingzhou Ding	Jinru Cai	Jiaxin Cao	Yaxin Li
3/23	Design document: Sec. 2.2, 2.7, Cost, Ethics	Design document: Sec. 1, coil/PCB figures	Design document: Sec. 2.4 (Motion Control)	Design document: Sec. 2.3, 2.5 (Vision, Comm.)
3/30	Design Document finalization and submission			
4/6	DSP LUT framework; frequency sweep test script	Solder transmitter board (new caps); solder receiver board	Line-following track test; stopping accuracy tuning	UART protocol implementation (RPi→STM32, RPi→DSP)
4/13	Solder half-bridge boards (×2); gate driver debug	Assemble power stage: half-bridge + transmitter + coils	UART comm with RPi; receive parking commands	Vision-guided parking command generation; closed-loop offset tracking
4/20	Power stage bring-up: inverter waveform, ZVS verification	Rectifier + output filter test; charging current measurement	Precision parking controller; micro-movement execution	Integration with STM32: send $(\Delta x, \Delta y) \rightarrow$ parking commands
4/27	LUT calibration: frequency sweep at 9 offset positions; populate DSP flash	Charging station mechanical assembly; ferrite shielding test	AGV full-path test: line-follow $\rightarrow$ vision parking	Integration with DSP: send offset $\rightarrow$ frequency update verified
5/4	Full system integration: AGV drives to station, parks, charges with adaptive PFM			
5/11	Efficiency measurement (fixed vs. adaptive); tolerance validation	Thermal test (10 min run); final hardware fixes	End-to-end parking accuracy measurement (10 trials)	Vision accuracy benchmark (50 trials); latency measurement
5/18	Final demonstration, presentation preparation, and report writing			

5. Ethics and Safety

5.1 Ethics

This project adheres to the **IEEE Code of Ethics** [9] throughout its design, implementation, and testing phases. The following ethical considerations are specifically addressed:

1. **Public welfare and environmental responsibility.** Wireless charging eliminates the need for physical connectors that wear out and generate contact waste. By improving charging efficiency through adaptive frequency control, the system reduces energy waste during each charging cycle. The CLLC resonant topology achieves soft switching, which lowers switching losses and minimizes heat dissipation compared to hard-switched converters. These design choices collectively contribute to lower energy consumption and reduced environmental impact over the system's operational lifetime.

2. **Responsible use of electromagnetic energy.** The system transmits power wirelessly at 50 kHz through coupled magnetic fields. While the operating frequency is well below the 150 kHz threshold where radiated emission regulations become stringent, we recognize the responsibility to minimize unnecessary electromagnetic field (EMF) exposure. The Mn-Zn ferrite shielding on the receiver coil attenuates stray flux by $\geq$80% above the coil plane, and the charging station enclosure confines the transmitter field. The system is designed to comply with the ICNIRP 2020 guidelines for exposure to time-varying magnetic fields [10] (reference level: 27 μT at 50 kHz for general public exposure). The wireless charging design also references SAE J2954 [11] for alignment methodology and interoperability considerations in wireless EV charging systems.

3. **Privacy considerations.** The Raspberry Pi camera subsystem captures video frames for ArUco marker detection. The camera is pointed downward at the charging station and processes images locally on the Raspberry Pi; no image data is stored, transmitted over a network, or used for any purpose other than real-time position estimation. No personally identifiable information is captured. Nevertheless, in a future deployment scenario where the AGV operates in shared spaces, appropriate signage should indicate the presence of an active camera.

4. **Honest representation of results.** All efficiency figures, tolerance analyses, and performance claims in this document are based on theoretical models and clearly labeled estimates. Where experimental data is not yet available, values are marked as "TBD" or "estimated." We commit to reporting measured results accurately, including cases where performance falls short of design targets.

5. **Intellectual property and attribution.** This project builds upon the previous generation's work (Spring 2025, Project No. 39). We reuse their PCB layouts and mechanical platform with proper acknowledgment. All new design contributions—adaptive frequency control, vision-assisted parking, DSP firmware—are original work by the current team. Third-party open-source libraries (OpenCV, ArUco module) are used under their respective licenses.

5.2 Safety

The system involves a 50 kHz power stage carrying currents up to 3 A, a lithium-compatible 12 V battery, and an autonomous moving vehicle. The following safety measures are implemented:

1. **Electrical safety.**

   - The DC bus voltage is 21 V, which is below the 60 V DC safety threshold defined by IEC 60950-1 [12]. However, the resonant tank can develop peak voltages of $\sim$100 V across the capacitors due to the $Q \approx 5.4$ amplification factor. All high-voltage nodes on the transmitter and half-bridge PCBs are clearly marked with warning labels, and the charging station enclosure prevents accidental contact.

   - The receiver board includes a 20 A / 65 V fuse (Littelfuse 0451020.MRL) that disconnects the battery in the event of a short circuit or overcurrent fault.

- All PCB traces carrying power-stage currents are sized for $\geq 2\times$ the expected RMS current, with adequate clearance (≥ 1 mm) between high-voltage and low-voltage traces.

2. **Thermal protection.**
   - An NTC thermistor mounted on the MOSFET heatsink is monitored by the DSP via ADC. If the temperature exceeds 100°C, the DSP firmware disables all PWM outputs, shutting down the inverter within one switching cycle (20 μs).
   - The total estimated power dissipation is $\sim$1.7 W at 20 W output. Passive heatsinks on the MOSFETs and thermal vias under the rectifier diodes ensure that component temperatures remain below 80°C under normal operating conditions.
   - If the Rx coil temperature rises abnormally (e.g., due to a foreign metal object on the coil surface causing eddy current heating), the CC6920BSO-20A current sensor on the receiver board will detect the abnormal current draw, and the DSP can respond by reducing or halting power transfer.
3. **EMF exposure.**
   - The 50 kHz magnetic field is confined primarily to the air gap between the Tx and Rx coils (15–25 mm). At a distance of 30 cm from the coil center (the closest an operator would normally be during charging), the magnetic flux density is estimated to be well below the ICNIRP general public reference level of 27 μT [10].
   - The ferrite shielding above the Rx coil reduces stray field penetration into the AGV body, protecting on-board electronics and further reducing the field in the upward direction.
   - Charging only occurs when the AGV is parked and stationary. No power is transmitted while the AGV is in motion or while personnel are servicing the vehicle.
4. **Battery safety.**
   - The output voltage is regulated to 12 ± 0.5 V by the CLLC gain design. The adaptive frequency control further maintains voltage stability under misalignment conditions, preventing overvoltage that could damage the battery.
   - The 20 A fuse provides a hard current limit. Additionally, the DSP monitors the output current via the CC6920 sensor and can disable the inverter if charging current exceeds a software-defined threshold.
   - The system does not implement cell-level battery management (BMS); the AGV's existing battery pack is assumed to include its own BMS for cell balancing and deep-discharge protection.
5. **Mechanical and motion safety.**

- The AGV operates at low speed ($< 0.5\,\mathrm{m/s}$) during the parking phase. The STM32 firmware implements a watchdog timer; if no valid command is received from the Raspberry Pi within 500 ms, the motors are stopped.
- A physical emergency stop button on the AGV chassis cuts power to both the motor driver and the wireless charging power stage simultaneously.
- During demonstrations and testing, the AGV operates within a roped-off area to prevent bystander contact.

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