Phasor Measurement Unit

Project 7
ECE 445 Spring 2013
Final Report

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1 INTRODUCTION

AC power grids propose complexity when distributing. Phasor Measurement Units (PMUs) are devices which measure the voltage to monitor the state of the grid.

Existing PMUs have proven to be costly and space-consuming devices. One of the reasons for the high cost and large size is due to their ability to take three phase measurements. Another factor comes from the fact that existing PMUs are made to be compatible with relays to be able to automatically correct for errors within the grid.

This project, however, focuses on building a unit that can be more economical and compact, with functionality optimization; instead of three-phase measurements, by implementing only one phase voltage measurement, the important functionality of the PMU is not compromised while keeping the cost low.

With lower price and more compact size, the distribution of PMUs across the U.S. power grid can greatly increase. Ultimately, relevant industries will be able to monitor the status of the grid, potentially increasing its stability.

Most useful data collected by the PMU will be what is called a synchrophasor data. A synchrophasor is defined as the magnitude and angle of a sinusoidal function as referenced to an absolute point in time. This can be taken by having an absolute clock reference for all devices. There are three measurements that are taken at each synchrophasor measurement: magnitude, phase, and frequency. The difference in wave magnitudes at different points down the transmission and distribution system indicates losses; the difference in frequency indicates instability; and the phase difference between voltage waves with respect to an absolute point in time indicates power transfer: there is a breakdown value which the phase difference must not reach in order to keep the system stable.

Thus, this project has a large impact on the advancement of power grids. Real-time monitoring of the state on the power grid will enable avoidance of blackouts. The ability to be deployed world-wide due to cost and size benefits will not only advance the grid in the United States, but in the other countries as well.

The function of this particular PMU is as follows: sample voltage at a rate of 50 kHz and report frequency, magnitude, and phase at a rate of 10 frames per second to a web server from the sampled

voltage. The goal was to produce a PMU costing less than $14000, which is the cost of the existing PMUs.

By limiting functionality, the price of the PMU can be greatly reduced. Table 1 shows a comparison of existing PMUs and the PMU built in this project.

Table 1. PMU Comparison [1]

	Current PMUs	Our PMU
Price	$10,000 - $15,000	~ $1,500
Sample	3 phase voltage, 3 phase current	1 phase voltage
Build	Incorporated into protective relays and other devices	stand-alone product
Location	Substations	Selected Households

As shown, the price of the PMU produced here is a magnitude lower than the existing PMU. The primary reason for this is by un-incorporating the protective relays and PMU. Since this PMU is incorporated into the distribution level, meaning household, the necessity of implementing a relay is low; circuit breakers are in each household already.

2 DESIGN

2.1 Block Diagram

Figure 1 shows the block diagram of the original design for the PMU.

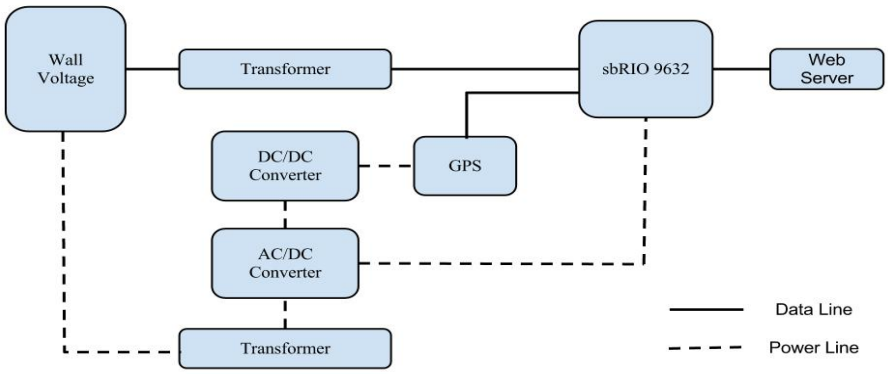


Figure 1. Original Design Block Diagram

Due to some difficulties with the configuration of the sbRIO 9632, however, the microcontroller had to be changed to another model which led to minor design changes. The block diagram for the modified design is shown in Figure 2.

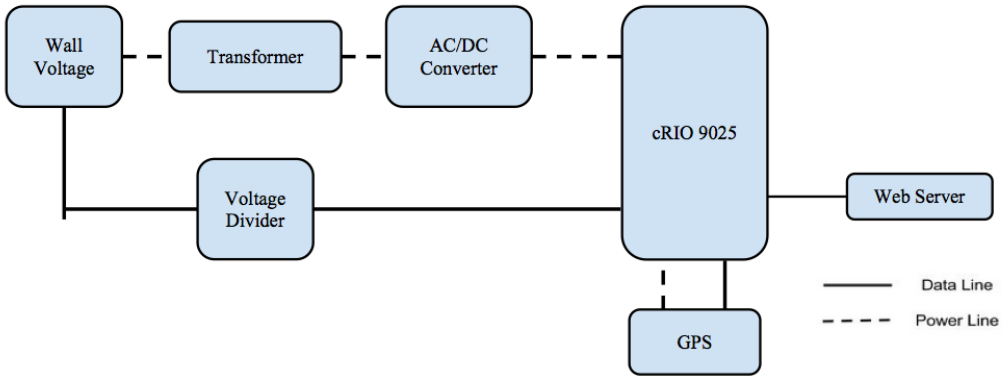


Figure 2. Modified Design Block Diagram

2.2 Block Descriptions (Modified Design)

2.2.1 Wall Outlet

Any wall outlet is a viable source of data sampling. It will connect to a transformer via modified NEMA 5-15 (AC power plugs).

2.2.2 Voltage Divider Circuit

Two resistors will be used to step down the wall voltage to a voltage that can be sampled from the compact-RIO. Desired transformer will step down 120V_{RMS} to 5V_{RMS}.

2.2.3 Transformer

A transformer will be used for the purpose of stepping down the wall voltage from 120V_{RMS} to 22V_{RMS} to act as an input for the AC/DC converter.

2.2.4 GPS

The GPS will output National Maritime Electronics Association (NMEA) GPRMC data sentence, along with a 5V pulse each second. Both data will be inputs to the compact RIO.

2.2.5 cRIO (Compact Reconfigurable I/O)

CRIO will take GPS data, GPS pulse, and stepped down wall voltage to calculate RMS value, frequency, and phase with precise timestamp. The data will be output as a text file. Serves same functionality to that of sbRIO 9632 except the cRIO is bigger in size, heavier, and about $5000 more expensive than the sbRIO 9632 (sbRIO is $900).

2.2.6 Web Server

Data generated from the cRIO will be uploaded to a web server. This will allow for the data to be observed from anywhere.

2.2.7 AC/DC Converter

This block will convert 22V_{RMS} from a transformer to a 24V_{DC}.

2.3 Preliminary Simulation Results for AC/DC Converter and Voltage Divider Circuit

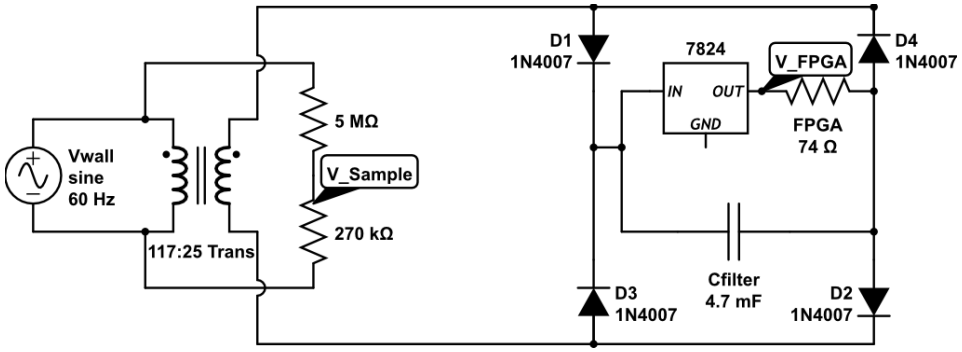


Figure 3. Power Supply

There are two parts to the power supply. The V_Sample and V_FPGA. Each component was calculated out with certain requirements.

V_FPGA is the constraint for the main part of the design. V_FPGA is voltage going to the sbRIO or cRIO and is not the actual voltage that goes into the FPGA chip. Initially, the voltage at the FPGA was chosen as 24V. Since at 60Hz, capacitive filtering would require a very large capacitor for a true rippleless voltage, a 4.7mF capacitor was decided to be used alongside with the UA 7824 voltage regulator. By doing this, the V_ripple is found to be fairly large, as shown in (1), but small enough for

this application. From the linear regulator specification [2], the linear regulator input can be found by (2) with the constraint of (3) and (4). The calculation in (2) assumes the voltage drop of 1N4001 as 0.6V each [3].

$$V_{ripple} = \frac{I_{load}}{2fC} = \frac{P}{2VfC} = \frac{7.75}{2*24*4700*10^{-6}} = .59V \quad (1)$$

$$V_{regin} = V_{secondary} - 1.2 \pm \frac{V_{ripple}}{2} \quad (2)$$

$$27V < V_{regin} < 37V \quad (3)$$

$$V_{regin} = V_{cap} < 35V \quad (4)$$

Using these properties, the V_secondary is solved for as a range in (5).

$$30.9V < V_{secondary} < 31.5V \quad (5)$$

From this calculated result, V_secondary is chosen as 31V to solve for the transformer turns ratio as 11:2.

For the V_Sample, at first, it was proposed that a step-down transformer would be an elegant solution to step down the wall voltage. However, it was determined that transformers not only are bulky, costly, and heavy, but also could produce varying losses if there are variations in wall RMS voltage or wall frequency.

Therefore, it was deduced that using a simple voltage divider rule could prove to be a more elegant solution because it is less costly, smaller, and lighter. V_Sample in Figure 3 shows the proposed circuit.

Since the range of wall voltage are given as 112 ~ 128 V_{RMS} and sbRIO analog input is limited by a range of -10~10V [4], calculations were done to find the appropriate ratio for two resistors used in the voltage divider circuit. Note that R_2 is the resistor with the voltage that will be sampled by the cRIO.

$$Wall\ Voltage \cdot \frac{R_2}{R_1+R_2} < 10 \tag{6}$$

$$\frac{R_2}{R_1+R_2} < 0.055243 \tag{7}$$

As a result, it was calculated that the ratio for the voltage divider circuit should be less than 0.055243. Then, choosing 5MΩ for R_1, it can be concluded that R_2 should have a value of 276 kΩ at most.

Further calculations can be done to prove that power dissipated in R_1 will be very small as well. Using $128V_{RMS}$ (higher limit) for wall voltage and 276 kΩ for R_2, it can be calculated that power lost through R_1 is at most shown

$$P_{lost,\ peak} = \frac{V_{1,\ peak}}{R_1} = \frac{\left(Wall\ Voltage \cdot \frac{R_1}{R_1+R_2}\right)}{R_1} = \frac{\left\{181 \cdot \frac{5 \cdot 10^6}{5 \cdot 10^6 + 276000}\right\}}{5 \cdot 10^6} = 5.9mW \tag{8}$$

It is concluded that standard quarter-watt resistors are sufficient for the circuit.

Figure 4 shows the simulation results. The results show that V_FPGA is stable at 24V, and V_Sample is an undistorted sine wave. This would power the board and allow sampling to be made.

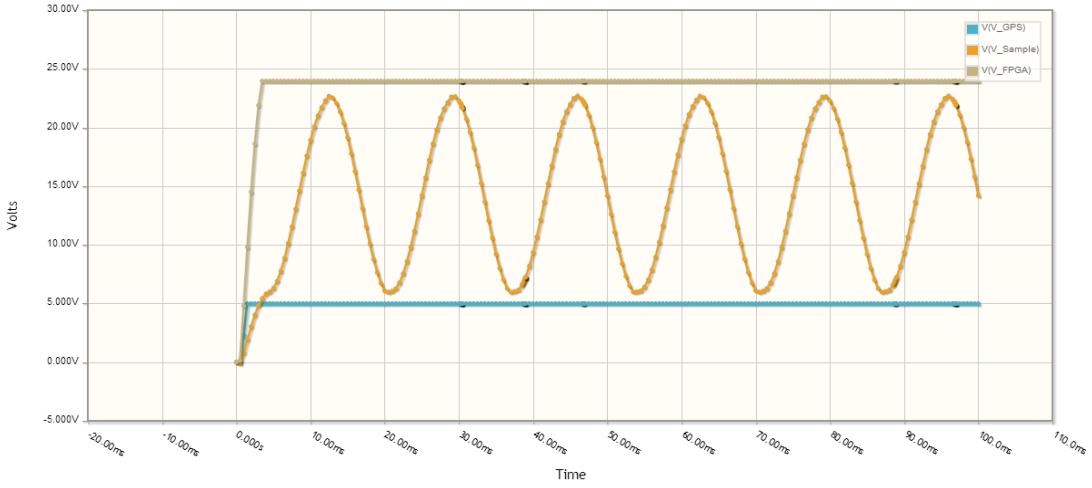


Figure 4. Simulation results

2.4 GPS Simulation

The Garmin 18x LVC provides timing information that "enables" data synchronization for the

project. A sample of the GPS 1 pulse per second signal is shown in the oscilloscope screen shot at Figure 5. The signal high is 5 V and low is 0 V. The distinct pulse leading edge marks the start of each second accurate up to 1µs. A sample of the National Maritime Electronics Association (NMEA) standard sentence "GPRMC" is shown in Figure 6, which provides the exact date and time stamp. These two form the time reference for the PMU.

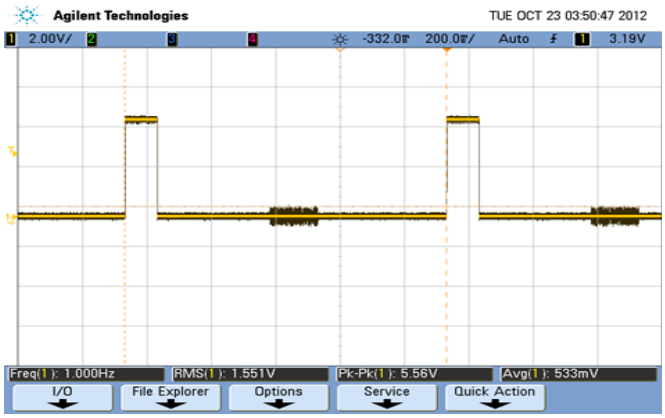


Figure 5. GPS Pulse Signal

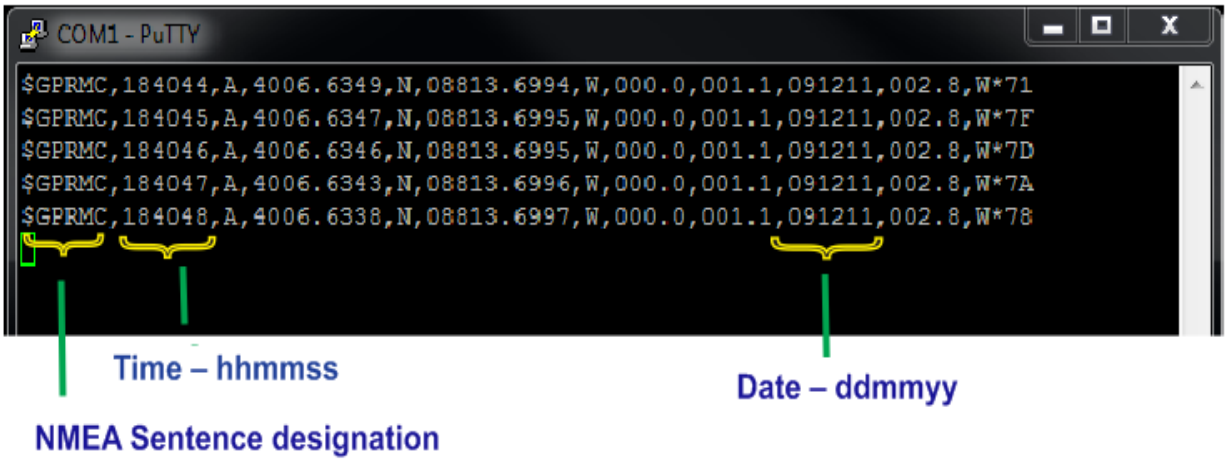


Figure 6. GPS Data Sentence for Date and Time [5]

Alternative method could be to use an atomic clock radio receiver, since the atomic clock radio receiver is proven to be more stable under various weather conditions compared to the GPS receiver.

2.5 NI LabVIEW Programming

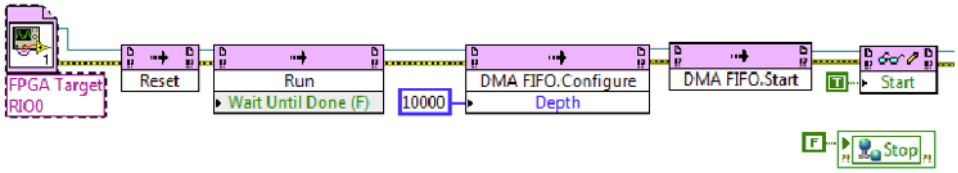
2.5.1 General Functionality

When the PMU is first plugged into the wall, the PMU will wait for the GPS pulse, which is transmitted every second. When the pulse is detected, the cRIO collects voltage data and inserts the data in a FIFO, which is a type of data storage structure. Then, every 0.1 second, the collected data is extracted from the FIFO and a voltage waveform is built. From the built waveform, frequency, phase, and RMS voltage data is calculated and uploaded to the web server.

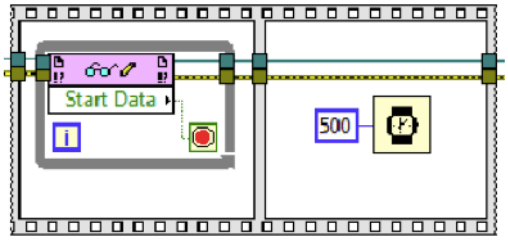
2.5.2 Control VI

Figure 7 shows the code written for the sbRIO. This VI controls 2 subVIs: FPGA VI and GPS VI. Control VI controls the overall operation for the PMU. It takes data read by FPGA subVI along with GPS subVI to calculate frequency, RMS voltage, and phase of the waveform and outputs correct data with precise timestamp. Timestamp data collected every second is divided into 6 parts and are assigned to corresponding group of voltage measurements and calculations. In this simulation, calculated data is output as waveform each time the FIFO fills up, as shown in Figure 11. LED and web server control will be added to this main VI. Figure 11 is shown on the next page.

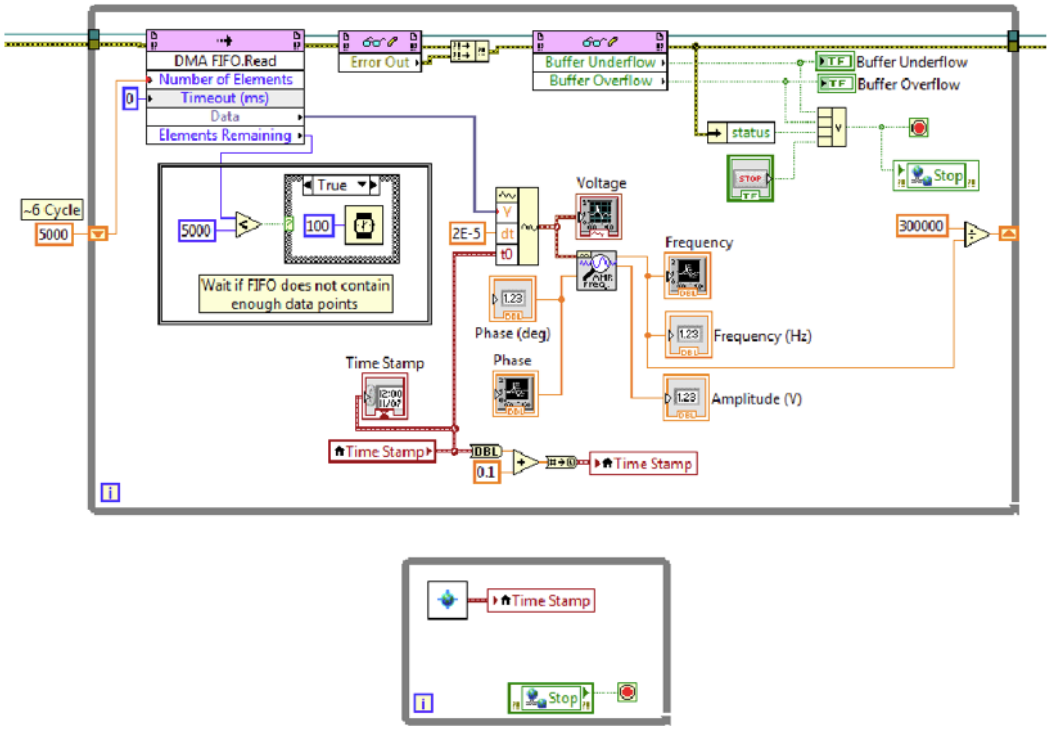
Initialize



Wait for FIFO to fill



Data collection & Analysis



"Stop"

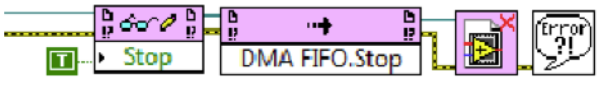


Figure 7. Control VI

2.5.3 FPGA subVI

FPGA subVI is operated by control VI to collect data at the start of pulse given by the GPS. Collected data points are put into a FIFO for control VI to utilize.

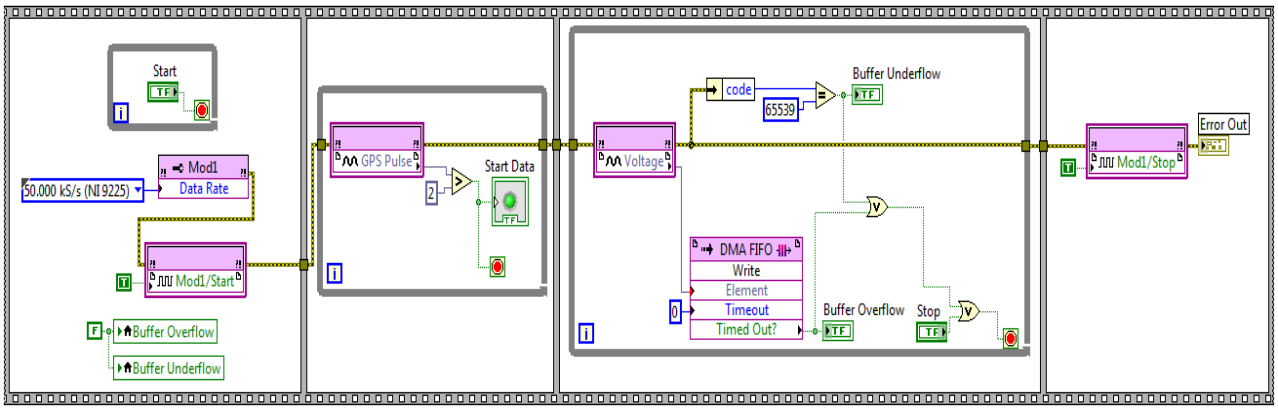


Figure 8. FPGA subVI

2.5.4 GPS subVI

This subVI collects GPS sentence in a string form and outputs year, month, date, and time exact to a second. The output is used by the control VI to stamp time to acquired voltage data.

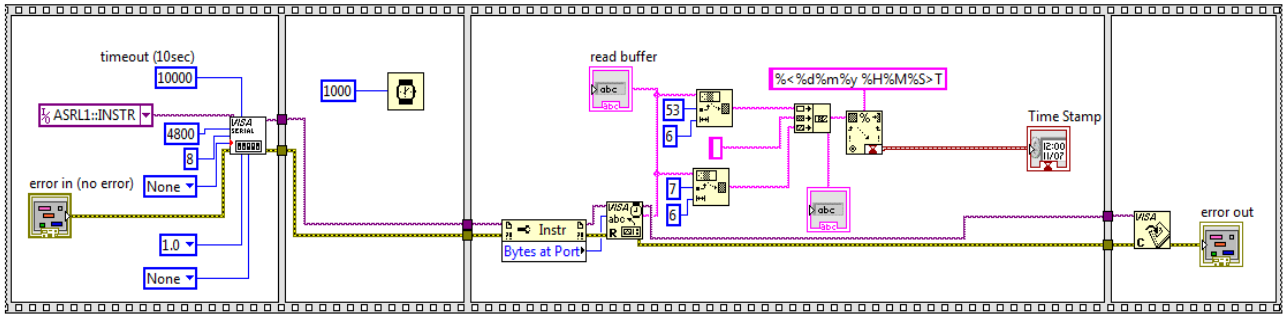


Figure 9. GPS subVI

2.5.5 Web Server

A spare Linux machine running Debian was set up as an Apache web server that can be accessed at pmu.ece.illinois.edu. FTP (File Transfer Protocol) method was used to access the webserver from the cRIO. The LabVIEW code used to do this is shown in Figure 10. It uses the FTP put buffer.vi function in LabVIEW.

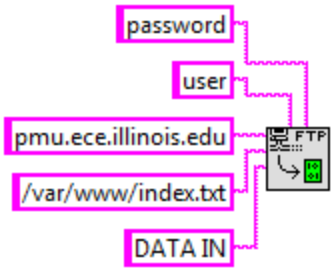


Figure 10. Web Server Access LabVIEW Code

3 Requirements and Verification

3.1 Testing Procedures

Requirements	Verification
Wall Outlet 1. Sinusoidal voltage wave with 120V_{RMS} ±6.667% provided by the utility company.	1. Tested using a voltage probe and an oscilloscope.
GPS 1. It must accurately generate a square wave with a rising edge at the beginning of each second. The pulse has 5 +- 0.6 V_{DC}. 2. The rising edge represents the beginning of each second and is accurate to within 1µs according to its specifications. The accuracy takes into account the effects c rise time.	1. The GPS signal will be verified using ar oscilloscope 2. The accuracy will not be tested since the specifications are assumed to be true.
Compact RIO 1. The FPGA inside the cRIO multiplies th analog input by the transformer step down conversion factor.	1. a. Programmatically multiply the analog signal by the transformer conversion factor b. Plot the resulting waveform in LabVIEW c. Calculate its RMS value d. It must be within 48 mV of the

	wall voltage.
2. Write code to calculate the frequency of the voltage wave.	2. The resulting frequency must be the sam as the frequency of the wave displayed on the oscilloscope.
3. The voltage wave will then be sampled and each point will be time-stamped using the GPS signal.	3. a. Display time-stamped data b. Compare timestamp with officia time c. Check the accuracy to be within 1 us.
4. It transmits data to a web server	4. a. Write code to transmit data to a server b. Test the code by giving it data to store online c. Check the web server to make sure data was successfully stored
<u>Web Server</u> 1. Continuously received data from the cRIO, as long as cRIO is powered on and no error in the code appear	1. a. Turn everything on b. Check the webserver to see if data is stored on the website c. Introduce an error by removing the GPS signal d. Check the webserver to make sure no data is stored with the GPS signal missing.
<u>AC/DC</u> 1. The AC/DC converter uses wall voltage to power the cRIO and GPS unit, therefore it must be designed to operate over the entire wall voltage range.	1. a. Power the converter using 112 V_{RMS} b. Measure the converter DC voltage using an oscilloscope

	c. It must be 25 VDC +- 20 mV d. Increment the voltage into the converter by $1V_{RMS}$. e. Measure the converter DC voltage f. It must be 25 V_{DC} +- 20 mV g. Repeat steps d. and e. until 128 V_{RMS} is at the input of the converter h. A steady converter output over the entire input voltage range wi verify its correct operation
2. cRIO input voltage from converter must be 25V_{DC} with a ripple less than 20 mV and current of 0.31A with a ripple of 25 mA	2. a. Add a 70 ohm load at the output of the AC/DC converter. This will draw 0.36 A, which is over the required limit of 0.31 A. b. Measure the voltage and its ripple using an oscilloscope c. Check if voltage is within required limits d. Measure current into the load using an oscilloscope e. Check current to make sure it is 0.36 A f. Let it running for half an hour g. Voltage and current values and ripples must not change value over time h. Make sure components do not melt or become hot while operating for a long period of time
3. GPS must be powered by the cRIO USB port	3. a. Plug the GPS into the USB port of the cRIO and verify that the pulse signal is present

3.2 Quantitative Results

3.2.1 AC/DC Converter and Voltage Divider

Figure 11 shows the DC voltage received from the AC/DC converter output. The voltage is steady and constant at 24.2V with 400 mV ripple; however, this ripple is caused by noise in the probe itself, and the converter successfully powered the board. Also, when the circuit was built and tested with R_1 and R_2 values of 5MΩ and 256kΩ for the voltage divider circuit respectively, result as shown in Figure 12 was obtained: it is verified that with a rms wall voltage of 123V, output of the voltage divider circuit is within the range of -10V to 10V.

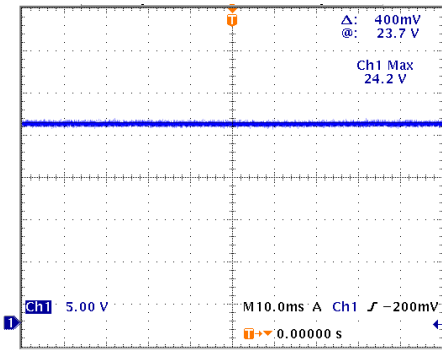


Figure 11: V_FPGA

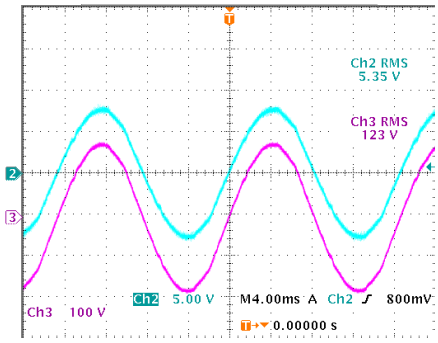


Figure 12: V_Sample (ch2)

3.2.2 Web server

Date	Time	Phase	Vrms	Frequency
04/22/13	07:08:15 PM	225.91	123.48	59.9964
04/22/13	07:08:15 PM	225.78	123.52	59.9929
04/22/13	07:08:21 PM	225.56	123.50	59.9937
04/22/13	07:08:21 PM	225.83	123.49	59.9917
04/22/13	07:08:21 PM	225.98	123.56	59.9955
04/22/13	07:08:21 PM	226.20	123.53	59.9969
04/22/13	07:08:21 PM	226.04	123.59	59.9956
04/22/13	07:08:21 PM	225.90	123.59	59.9966
04/22/13	07:08:22 PM	225.72	123.55	59.9958
04/22/13	07:08:22 PM	225.63	123.54	59.9929
04/22/13	07:08:22 PM	225.40	123.54	59.9971
04/22/13	07:08:22 PM	225.67	123.48	59.9964
04/22/13	07:08:22 PM	225.52	123.53	59.9965
04/22/13	07:08:22 PM	225.37	123.56	59.9962
04/22/13	07:08:22 PM	225.27	123.57	59.9940
04/22/13	07:08:22 PM	225.10	123.54	59.9950
04/22/13	07:08:22 PM	225.38	123.58	59.9969
04/22/13	07:08:22 PM	225.27	123.59	59.9964

Figure 13. Web server snapshot

The GPS takes a few seconds to calibrate, therefore the first set of data will not have accurate time stamps. This can be seen in data above the horizontal line of Figure 13. Once the GPS calibrates, the cRIO successfully sends 10 samples per second to the web server. This is illustrated by the data below the horizontal line of Figure 13.

3.3 Discussion of Results

The timestamp obtained from the GPS was verified by using the internet to check the official UTC time. As a result, the two times were observed to agree completely. The RMS voltage calculated by the cRIO was also successfully verified by using a multimeter on the wall voltage.

The frequency of the voltage calculated by the cRIO was verified by comparing it to the frequency of the voltage being displayed on an oscilloscope; the frequencies were the same. Furthermore, the cRIO allowed for a more precise measurement of frequency because it displayed more significant digits when compared to the oscilloscope.

Figures 14 through 16 show the waveforms obtained by plotting the data generated by the cRIO.

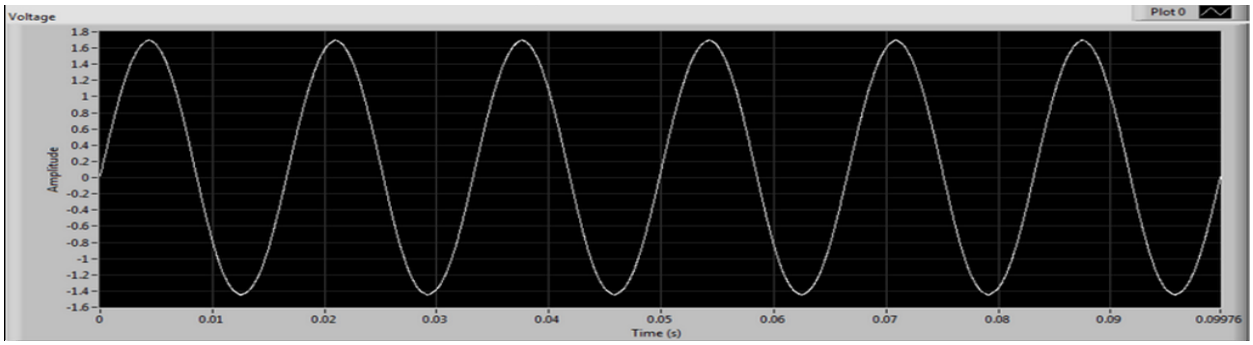


Figure 14. Voltage Waveform from cRIO Data

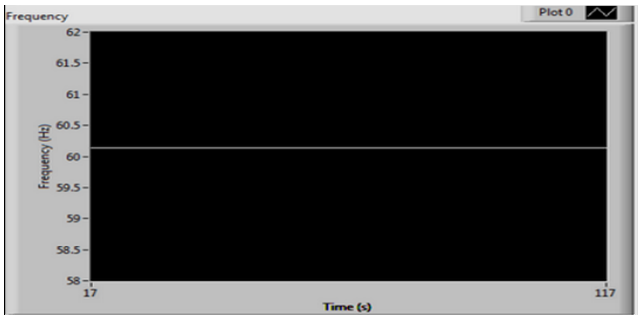


Figure 15. Calculated Voltage Frequency

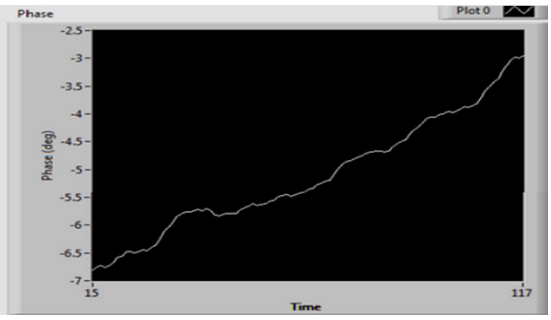


Figure 16. Calculated Voltage Phase

Since the frequency of the voltage is higher than 60 Hz, as illustrated in Figure 15, the first 6 cycles take a little less than a tenth of a second to complete; this is illustrated in Figure 14 and gives rise to a phase. In other words, the phase would be zero if the frequency was exactly 60 Hz.

3.4 Tolerance Analysis

The National Electrical Code (NEC) says the standard for the wall voltage is 120V ±5%. This gives a range of 114 V to 126 V. However, in order to accommodate outliers, we will design our power converter to operate from a voltage source range of 112 V to 128 V. The sbRIO-9632 user guide dictates that the power supply ripple must be less than 20 mV.

Since there is a step down of voltage from the wall outlet to the analog input of the FPGA, an error factor naturally exist. The accuracy of the voltage measurement is essential. However, since the FPGA is accurate up to 6220 μV at the highest voltage range (-10V to 10V), this would mean that the FPGA can theoretically be accurate up to 0.06%. To bring the error factor to low as possible, an Agilent Technologies oscilloscope will be used to make sure that this voltage is accurate up to 0.1%.

4 Cost

4.1 Labor

Name	Rate	Hours	Total	Total x 2.5
Andy Yoon	$40/hr	100	$4,000	$10,000
Bogdan Pinte	$40/hr	100	$4,00	$10,000
Kenta Kirihara	$40/hr	100	$4,000	$10,000

Total: $30,000

4.2 Parts

Description	Manufacturer	Vendor	Cost/Unit	#	Total Cost
cRIO-9225 + 2 analog modules	National Instruments	National Instruments	$6795	1	$0 (Donated)

Linear Regulator UA7824	Texas Instruments	Digikey	$0.91	1	$0.91
Metallic Base	Menards	Menards	$3.26	1d	$3.26
Capacitor UVZ1H472MRD	Nichicon	Digikey	$3.07	1	$3.07
PCB	ECE Machine Shop	ECE Machine Shop	$40.00	1	$0 (Donated)
Diode 1N4007	Vishay S.D.D.	Digikey	$0.43	4	$0 (University)
5 Port Ethernet Switch	Linksys	ECE Sore	$35.33	1	$35.33
STANCOR P8180 Transformer	STANCOR	ECE Store	$13.23	1	$13.23
Various Electrical cables	Tensility International Corp.	ECE Store	$5.00	1	$5.00
GPS 18x LVC	Garmin	gpscity	$60.00	1	$0 (donated)

4.3 Total Project Cost

Total Labor Cost	Total Parts Cost	Total Project Cost
$30,000	$60.8	$30,060.8

*Total project cost is to be $ 36,956.2 (counting donated and existing parts)

* If the sbRIO is used as first intended, the total parts cost will be $31,061.2

5 Conclusion

5.1 Accomplishments

In summary, the project was a success in many ways. Not only does the Phasor Measurement Unit successfully sample data at 50 kHZ as intended, correct frequency, phase, and voltage data were also calculated and uploaded to the web server.

5.2 Uncertainties

When the transformer was acquired and tested for functionality, the secondary voltage was higher than what its specification had stated, which was too high high for the linear regulator. However, after rectifying and filtering the transformer output with diodes and capacitors, respectively, the voltage was sufficient for the linear regulator.

Another problem the group has encountered was from the sbRIO 9632. When the board was first acquired, configuration problems persisted. At first, it was suspected the software on the computer that is used to configure the board had problems. However, upon receiving help from not only National Instruments' support engineers, but also another group that has had success in configuring their board, it was determined that the problem existed in the board itself. However, when another board was acquired and tested for, same problem existed.

Lastly, the software ran into a buffer overflow problems. Since a FIFO is utilized in the software portion of the PMU, the rate of data extracted from FIFO must be equal to the rate of data inserted to the FIFO. If the extraction rate is faster than the insertion rate, buffer underflow will happen. If the extraction rate is slower than the insertion rate, FIFO will become full and buffer will be overflowed. The buffer overflow problem did not exist without the web server implementation. However, with the code to upload the data to the web server, the extraction of data seemed to delay with inconsistent time, depending on the stability of the network connection. This problem can be solved by writing a code to allow dynamic delays within the program; the amount of time delay due to web server upload can be measured and used for increasing or decreasing the rate of data insertion. Also, the size of FIFO can be increased to allow some leeway with delay.

5.3 Ethical Consideration

Our team agrees to adhere to the IEEE Code of Ethics included in Appendix [A]. Furthermore, the following portions of the IEEE Code of Ethics are directly pertinent to our project:

1. "to be honest and realistic in stating claims or estimates based on available data" [6].

Our PMU must not operate outside of the claimed errors. Its data must be as reliable as we claim it to be.

2. "to improve the understanding of technology; its appropriate application, and potential consequences" [6].
   One main reason to build the PMU was to aid in academic research by improving the understanding of their operation.

5.4 Future work/Alternatives

In the future, intentions are to invite one of the National Instruments field engineers for hands on assistance for sbRIO configuration. After a successful configuration, plan is to replace the cRIO with the sbRIO, as the group first envisioned. As discussed in section 5.2, buffer overflow will be dealt with. Lastly, the labVIEW codes will be implemented to allow for the board to be able to run automatically when plugged in, instead of a computer having to tell the program within the board to start acquiring data.

6 Reference

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[2] Sparkfun, "Positive-Voltage Regulators," [Online Document]. 2003, [cited 29 April 2013], Available HTTP: https://www.sparkfun.com/datasheets/Components/LM7805.pdf

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[4] *National Instruments*. "NI sbRIO User Guide," [Online Document], 10 June 2008, [cited 29 April 2013], Available HTTP: http://www.ni.com/pdf/manuals/375052c.pdf

[5] K. Reinhard, "Final Project Report: Phasor Measurement Unit," Dec 9, 2011

[6] Section 7.8 IEEE Code of Ethics, IEEE. "IEEE Code of Ethics," IEEE. Web. 25 Feb. 2013. <http://www.ieee.org/about/corporate/governance/p7-8.html>.

7 Appendix

[A] Section 7.8 IEEE Code of Ethics

We, the members of the IEEE, in recognition of the importance of our technologies in affecting the quality of life throughout the world, and in accepting a personal obligation to our profession, its members and the communities we serve, do hereby commit ourselves to the highest ethical and professional conduct and agree:

1. to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;
2. to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;
3. to be honest and realistic in stating claims or estimates based on available data;
4. to reject bribery in all its forms;
5. to improve the understanding of technology; its appropriate application, and potential consequences;
6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;
7. to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others;
8. to treat fairly all persons regardless of such factors as race, religion, gender, disability, age, or national origin;
9. to avoid injuring others, their property, reputation, or employment by false or malicious action;
10. to assist colleagues and co-workers in their professional development and to support them in following this code of ethics.

Changes to the IEEE Code of Ethics will be made only after the following conditions are met:

- Proposed changes shall have been published in THE INSTITUTE at least three (3) months in advance of final consideration by the Board of Directors, with a request for comment, and
- All IEEE Major Boards shall have the opportunity to discuss proposed changes prior to final action by the Board of Directors, and
- An affirmative vote of two-thirds of the votes of the members of the Board of Directors present at the time of the vote, provided a quorum is present, shall be required for changes to be made.