Appendix

Note: Figures referred to as A.1, A.2, etc. in the main text of the paper are numbered as 1, 2, etc. in the Appendix.

Figure 1: PSoC Pin Diagram and Recommended Power Connections

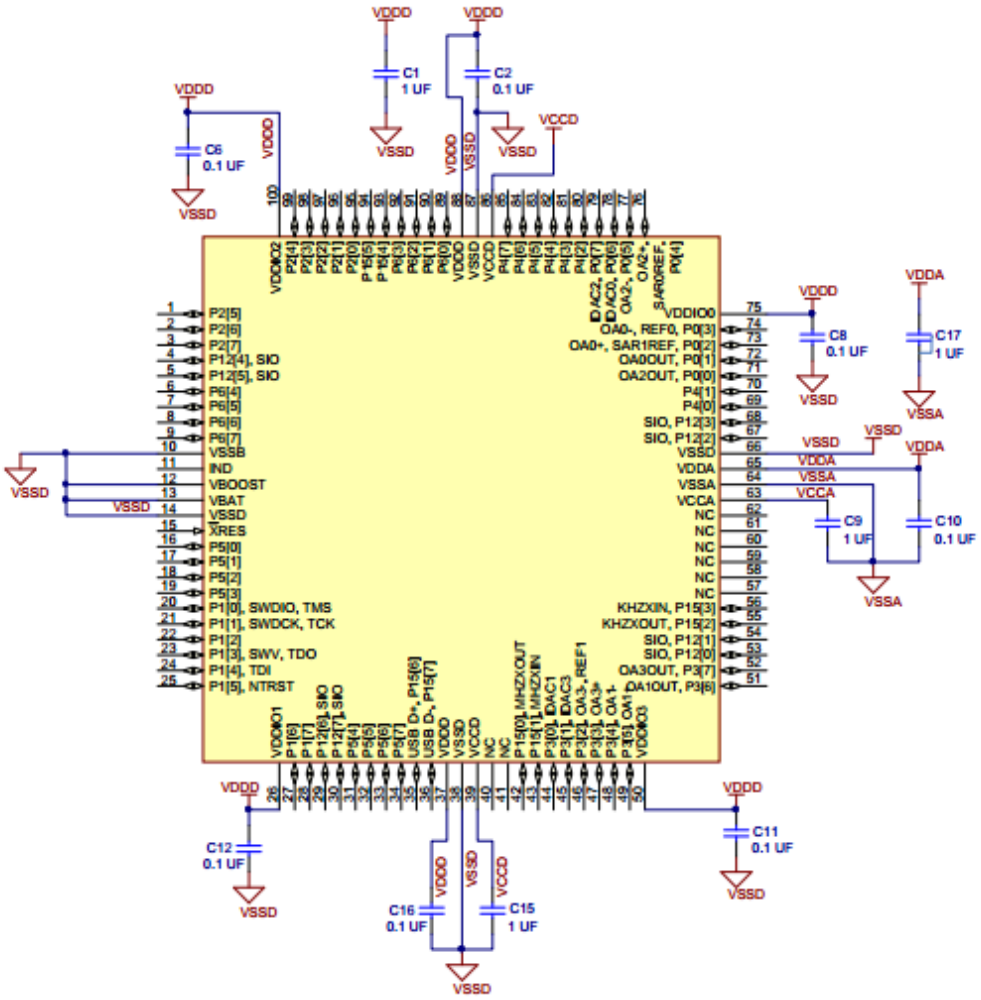

Figure 2: Display Hardware Block Diagram

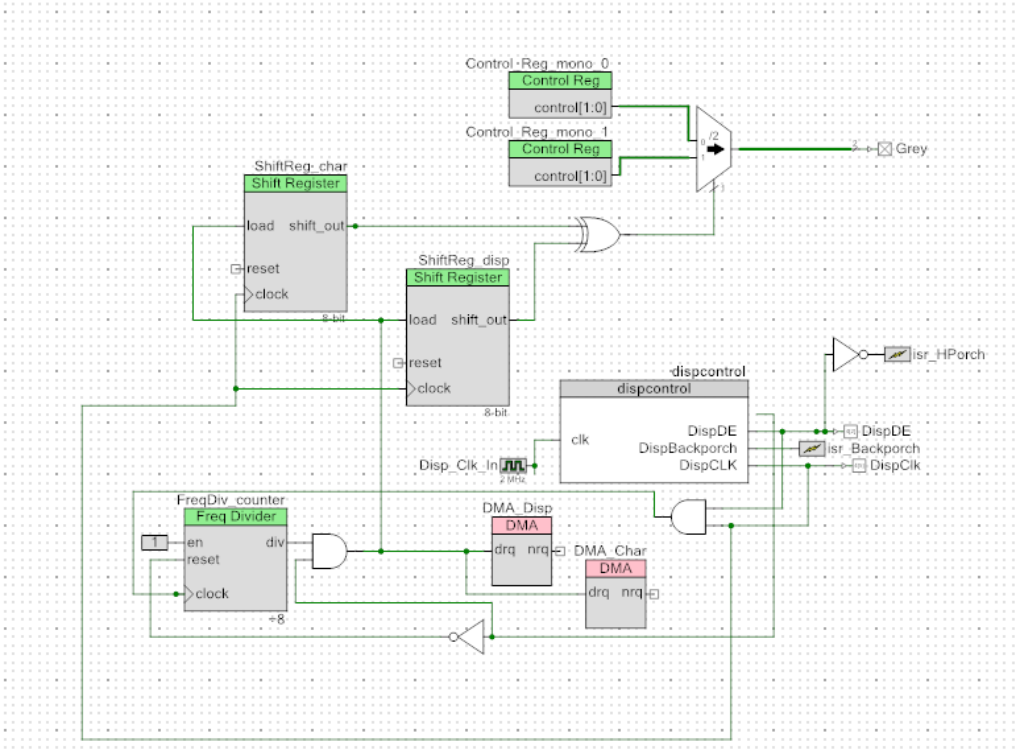

Figure 3: User Input and Xbee Software Blocks

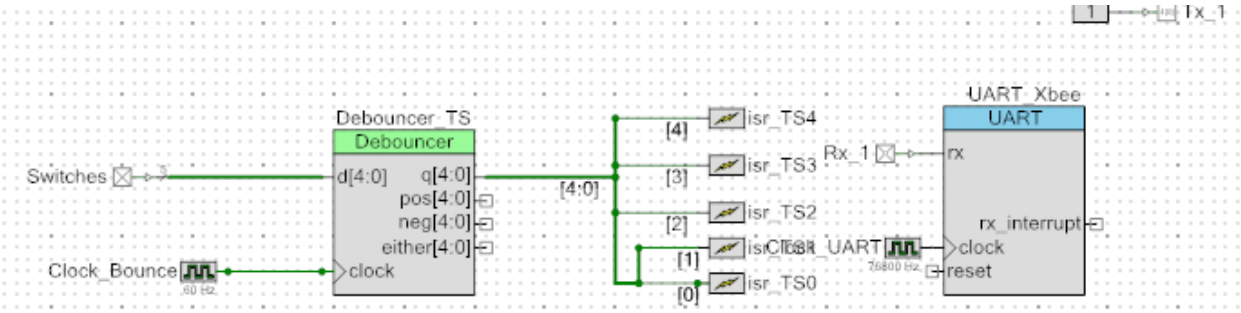

Figure 4: LCD Character Display and LED Software Blocks

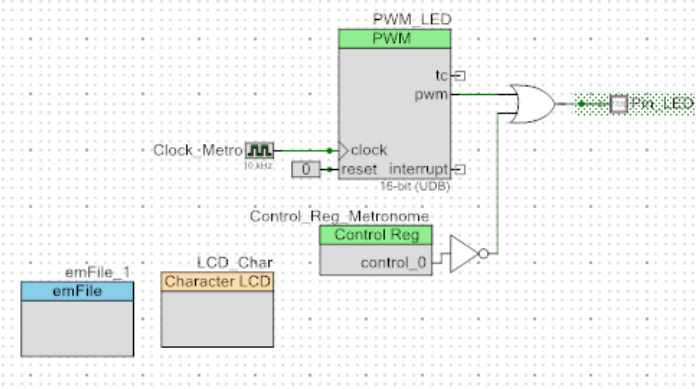

Figure 5: Data Enable Signal Generator

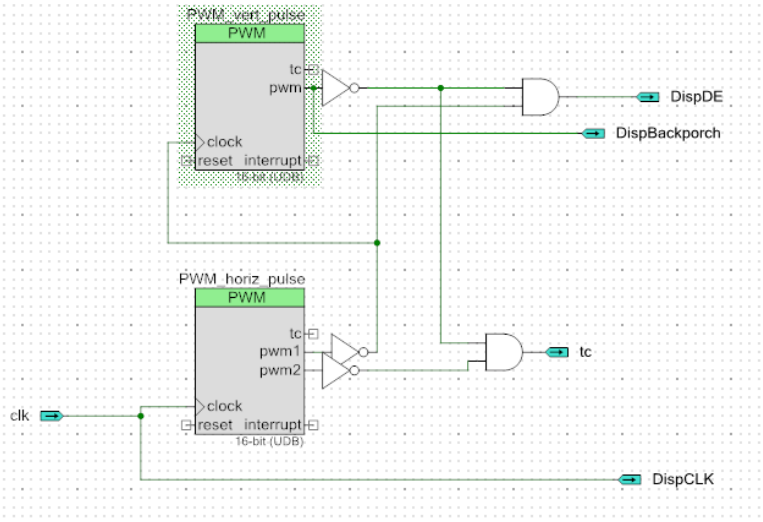

Figure 6: Final Schematic

Note: Boost Converter included in Schematic and PCB design, but not implemented

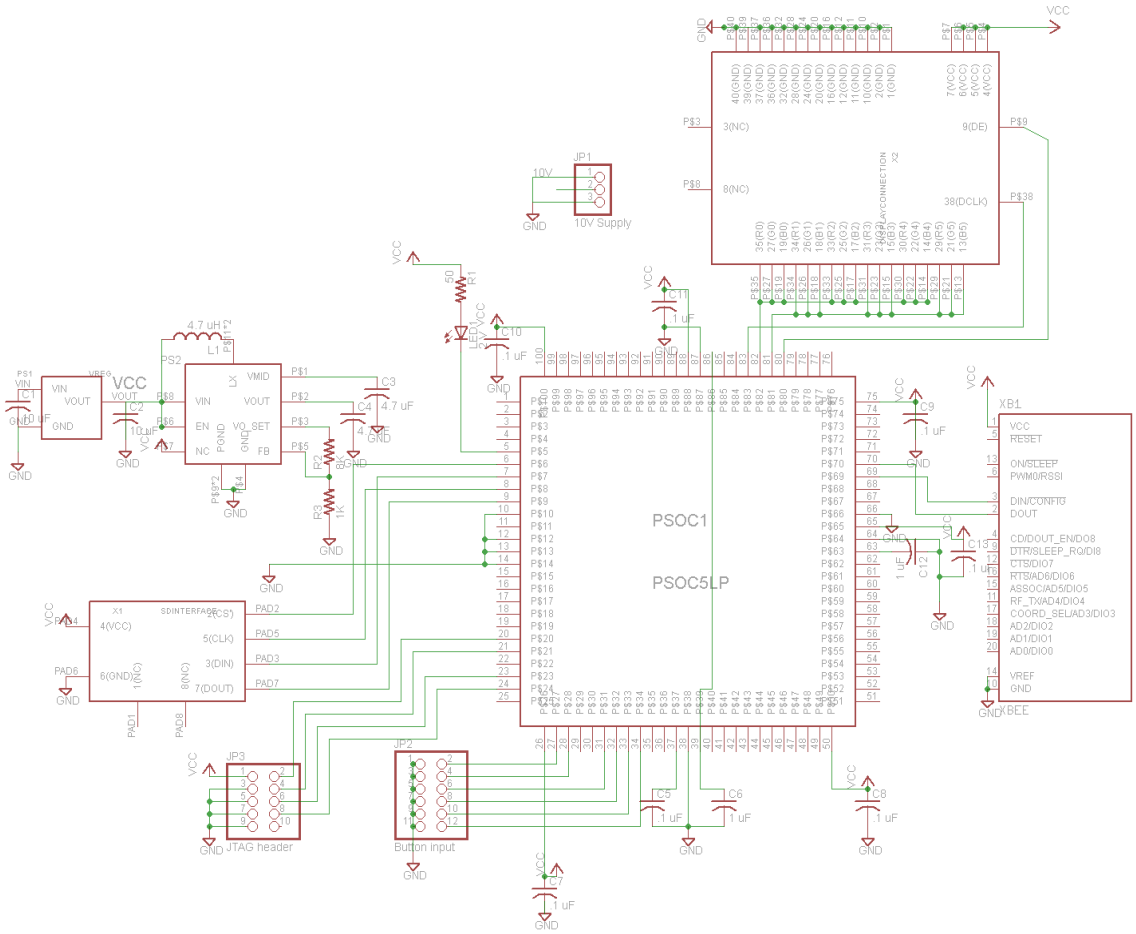

Figure 7: Final PCB Layout

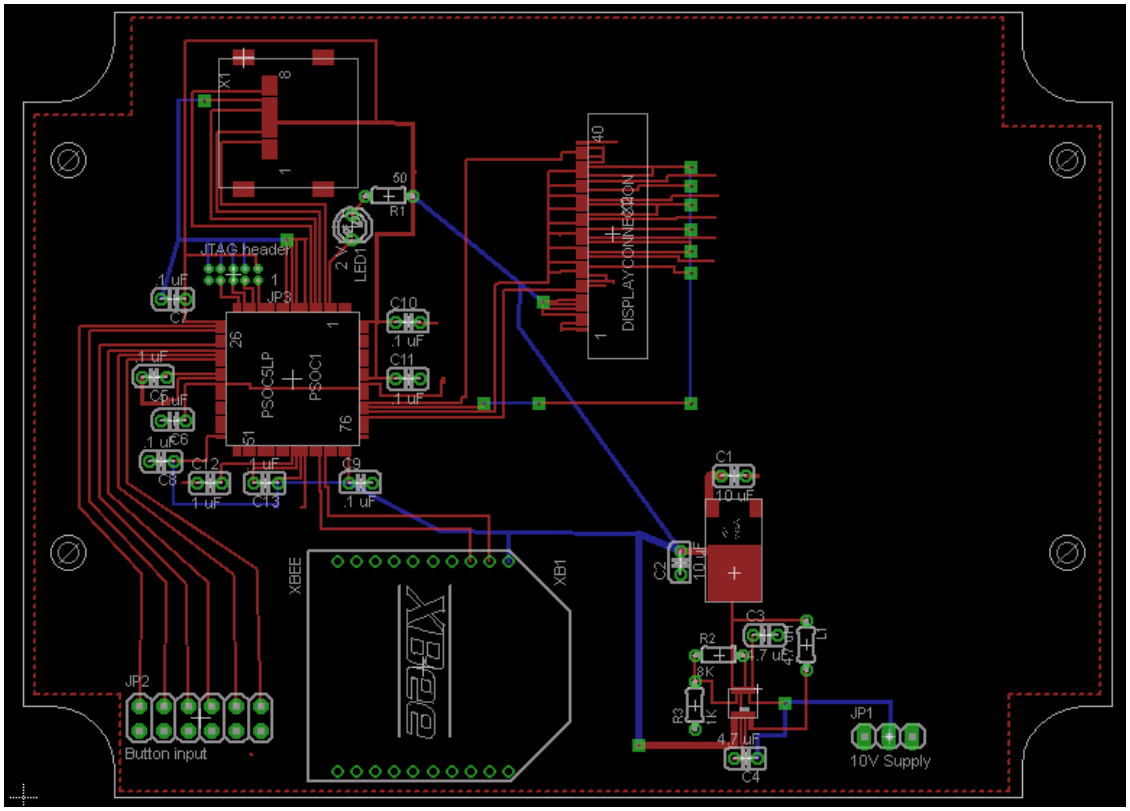

Figure 8: DevBoard Interface Schematic

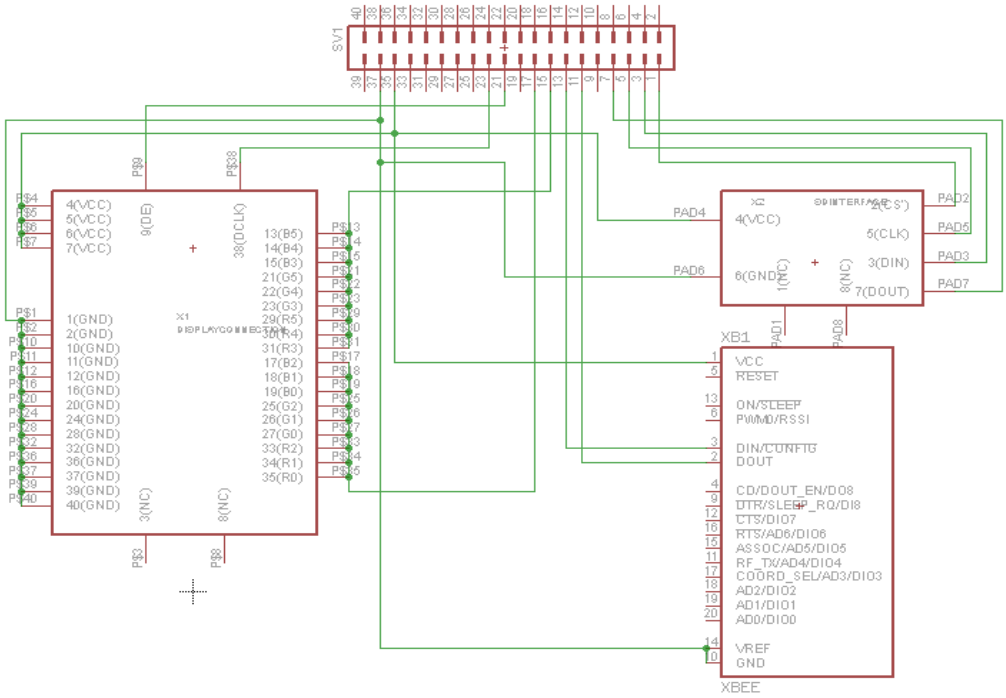

Figure 9: DevBoard Interface PCB layout

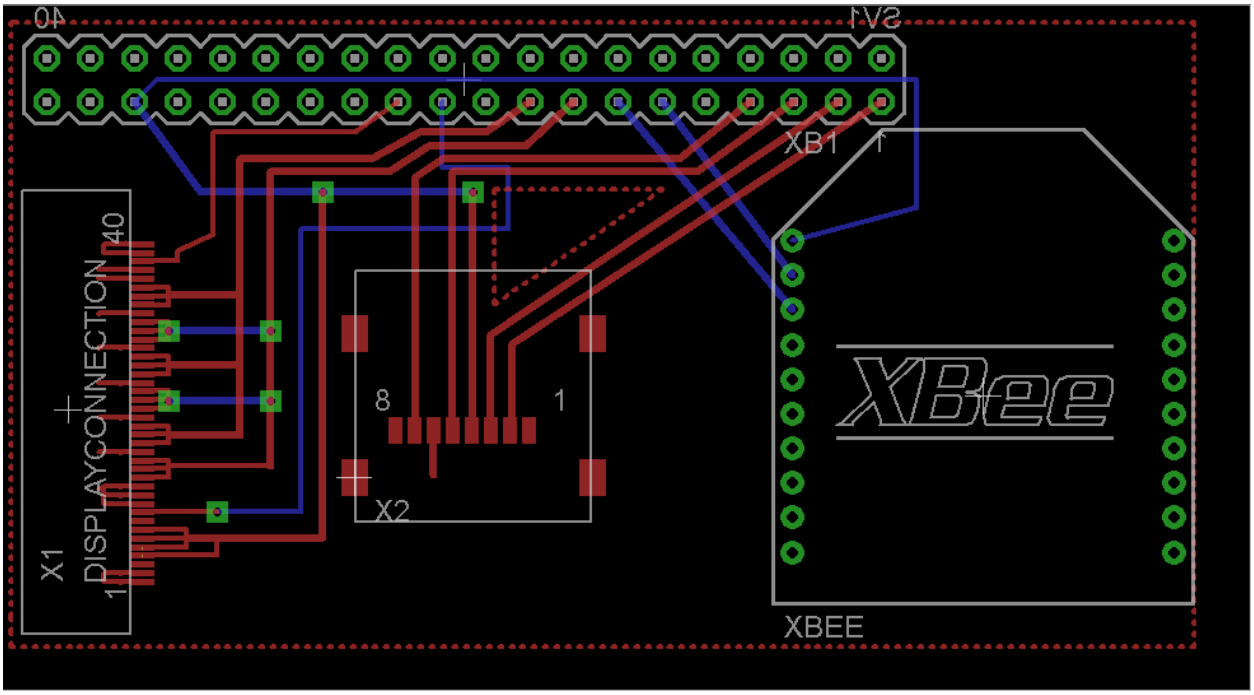

Figure 10: DevBoard Port E Schematic

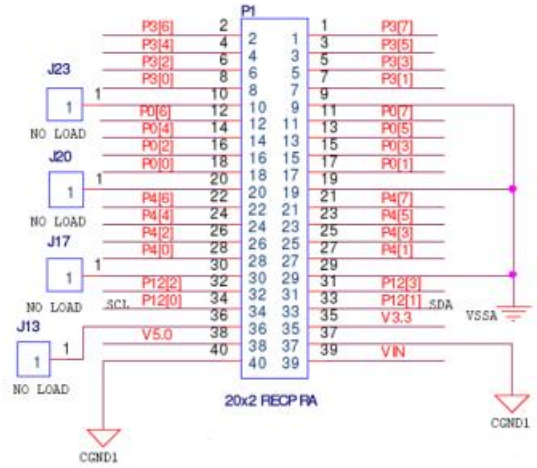

Table 1: Full Requirement and Verification Table

Requirement	Description	Verification
PS 1	Power Supply turns on, delivers 3.1 to 3.5 V to all components for 5 hours	Device is turned on, all components to full power. Dummy harness sends periodic commands to display and transceiver, preventing any component from enabling a low-power mode. Voltage is periodically checked on all power supply pins to ensure the power is within tolerance.
FAT 1	Processor can read information from the SD card.	MicroSD card is written from a PC with a FAT filesystem containing several files indicating GPIO pins to set high. Microprocessor is programmed with the filesystem component and a main program that uses the filesystem to access the files and raise the appropriate debug pin.
FAT 2	Processor can write information to the SD card	MicroSD card is formatted with a blank FAT filesystem on a PC. Microprocessor is programmed with the filesystem component and a main program that uses the filesystem to write sample file to the SD card. The SD card is read by the PC to ensure the data is correctly written.
FAT 3	Filesystem is interrupt safe	In addition to FAT 1 and FAT 2, microprocessor is configured to receive frequent timer interrupts
COMM 1	Microcontroller correctly receives packet from main controller at 300’	Central communicator is placed appropriate distance away from the device. A command is sent from central communicator to the microcontroller, which is interpreted to raise the appropriate debug pin.
CPU 1	Image loads into correct areas of video memory	PSoC is programmed with dummy VGA controller that merely outputs the grayscale values without regard for VGA timing. CPU is instructed to display sample images consisting of a short, repeating pattern. Output is inspected on oscilloscope to ensure it matches the expected pattern.
CPU 2	Menu system allows the selection of music	PSoC is programmed with dummy filesystem which raises debug pins when non-existent file is accessed. Device is booted, and menu is navigated according to the menu flowchart. Debug pins are monitored to check if the software is properly accessing the index

		and the files.
CPU 3	Menu system allows the control of metronome speed	PSoC is programmed to output metronome speed to the debug pins. Device is booted, and menu is navigated according to the menu flowchart. Debug pins are monitored to ensure the speed is increasing or decreasing.
CPU 4	Cues and text correctly overlay over image	Memory is loaded with test image, and several precalculated cue and text drawing commands are executed on top of it. Memory is compared to the expected result of the image plus the drawn figures.
VGA 1	VGA outputs 1 pixel per pixel stored in memory	Alternating white and black pattern is loaded into the display memory. Oscilloscope is used to ensure that the signal changes from white to black on the appropriate clock edges.
VGA 2	VGA line timing is appropriately synced to device	VGA controller input is set to an image consisting of alternating white and black lines, and vertical lines down the sides. Display is checked to ensure white and black lines spread entirely across the width of the display, and vertical lines are exactly on the sides of the display
VGA 3	VGA is correctly vertically synced to device	VGA controller input is set to a vertical line down the middle of the display, and horizontal lines on the very top and bottom. Display is checked to ensure line is completely vertical, and the horizontal lines are exactly on the top and bottom of the display.
MET1	Metronome ticks at correctly configured speed	Metronome is preprogrammed at different speed levels, ranging from 30 bpm to 250 bpm. Output is routed to counter on PSoC, which is checked after 5 minutes to ensure that the metronome stayed within 1% of the configured speed.