iPhone Ultrasound

Senior Design Project Design Review

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1. Introduction

a. Motivation

We will create a low-cost, portable A-scan biometric ultrasound circuit driven by an iPhone 4S. This would provide an inexpensive ultrasound alternative with a more user-friendly interface compared to existing optical ultrasound solutions.

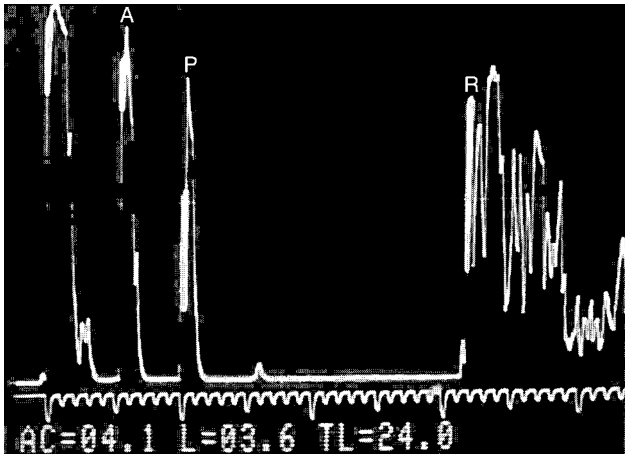


Figure 1. Typical Biometric A-Scan Result [15]

b. Objectives

The goal of our project is to implement a system that can perform 1-dimensional biometric scans that ophthalmologists can use to measure the axial lengths of eyeball components. These measurements of the eye are used to calculate intraocular lens (IOL) power for cataract surgeries. Ultrasound transducers typically operate at 10MHz, since the short distances in the eyeball require high resolution. While there are handheld ultrasound probes available, they all use processor/video/input hardware created specifically for that device - driving up its cost while having a poor user interface.

In addition, many third-world countries lack structured landline communication networks, making the sharing of this kind of medical information a heavy task. A system of sharing this information over modern, conventional wireless networks may aid in the health-care of ailing citizens.

Our project aims to alleviate these problems by improving upon the user interface of existing devices, driving down costs with the use of hardware many doctors already own (the iPhone 4S), and securely sending eye scan results over established cellular networks.

Benefits:

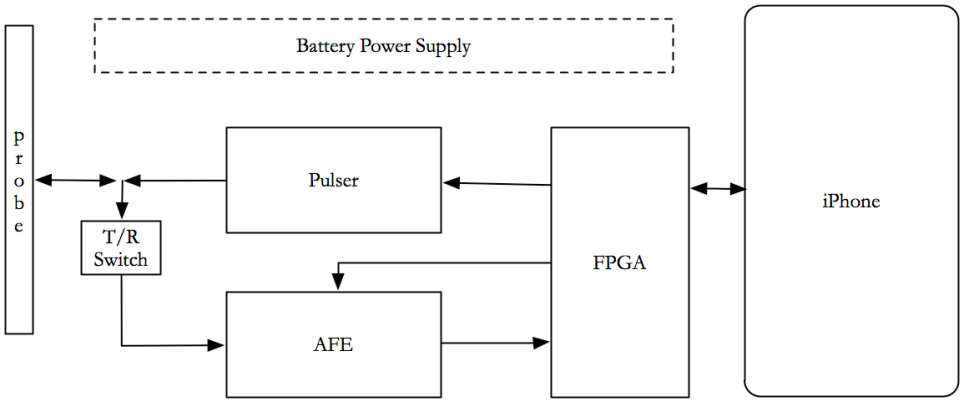
- Lower medical device costs with the use of existing hardware
- Highly portable form factor
- Immediate/live ultrasound measurements
- Axial Eye Length (AEL) measurements accurate to within 0.1mm for anterior chamber depth, lens depth, vitreous length, and axial eye length

Features:

- 10 MHz single-element ultrasonic transducer probe
- Manchester Encoded Transmission of A-scan data to iPhone 4S over 3.5mm Headphone Audio Jack
- Provides user with one echogram per second
- User-friendly interface on 3.5" iPhone 4S LCD display with touch user interface
- Choice of contact or immersion measurement
- Numeric values displayed for anterior chamber depth, lens thickness, vitreous length, and AEL with 0.1 mm resolution
- Integrated IOL power calculator
- Storage of up to 500 echograms for review and critiquing
- Ability to send echogram images over MMS or e-mail

2. Design

a. Block Diagram (Figure 2)



b. Block Descriptions

- **Ultrasound Probe:**
  The ophthalmic ultrasound transducer probe is responsible for transmitting and receiving ultrasonic pulses by means of a single piezoelectric element that operates at 10MHz. In the transmission phase, a high-voltage pulse is sent to the Probe, which relays an ultrasonic pulse out of the Probe's tip. As the Probe receives the echoes from that pulse, it relays low-voltage pulses back to the circuit.
- **T/R Switch:**
  The Transmit/Receive Switch prevents interference between the high voltage pulses being sent to the probe transducer and the lower amplitude echoes being returned from the eye. This also protects the low noise amplifier in the Receiver from the high voltage signals coming from the Transmitter.
- **Transmit Pulser:**
  The Transmit Pulser circuit generates a short 10MHz, high-voltage pulse. This pulse is sent through the T/R Switch on to the Ultrasound Probe.
- **Analog Front End (AFE):**
  The AFE circuit preprocesses signals received from the Ultrasound Probe into more meaningful ones for AEL measurement at the back end of our device. Because received signals are attenuated as they travel through eye tissues, this circuit tailors the gain of the amplifiers to compensate for these losses over time through Time-Gain Compensation (TGC). This circuit also converts the amplified analog signal to high frequency digitized data that is sent to the FPGA over LVDS (Low Voltage Differential Signaling).
- **FPGA:**
  The FPGA module acts as the communication interface between the probe and the iPhone. It communicates with three components: the iPhone, Pulser, and AFE. Commands to initiate and stop scans are sent from the iPhone's audio jack port and are passed as control logic inputs to the Transmitter. Pre-processed and digitized data from the AFE are received and processed for transmission to the iPhone. The FPGA also sends signals to status LED indicators.
- **iPhone 4S:**
  The iPhone serves as the graphical user interface, displaying scan results and accepting user input commands. The user can initiate and stop a scan from the phone, with a live graph of incoming ultrasound measurements available while the scan is in progress. Between scans, the user can adjust sound velocity parameters for different eye conditions, perform IOL calculations, save the last scan, or send a scan image via email or MMS.
- **Power Electronics:**
  A 9V Lithium-Ion battery will be used to supply power to the chips on the device's front-end circuitry (T/R switch, Pulser, AFE, and FPGA). Boost/Buck Converters and Voltage regulators will be implemented to satisfy individual chips' requirements.

c. Electrical Design Schematics and Simulations

■ Altera Cyclone III FPGA

The Altera Cyclone III is a powerful Field-Programmable Gate Array (FPGA) featuring 10,320 Logic Elements. Its 144 pins are divided into three sections below by function, and the communication protocol with the iPhone is discussed.

Section 1: Power

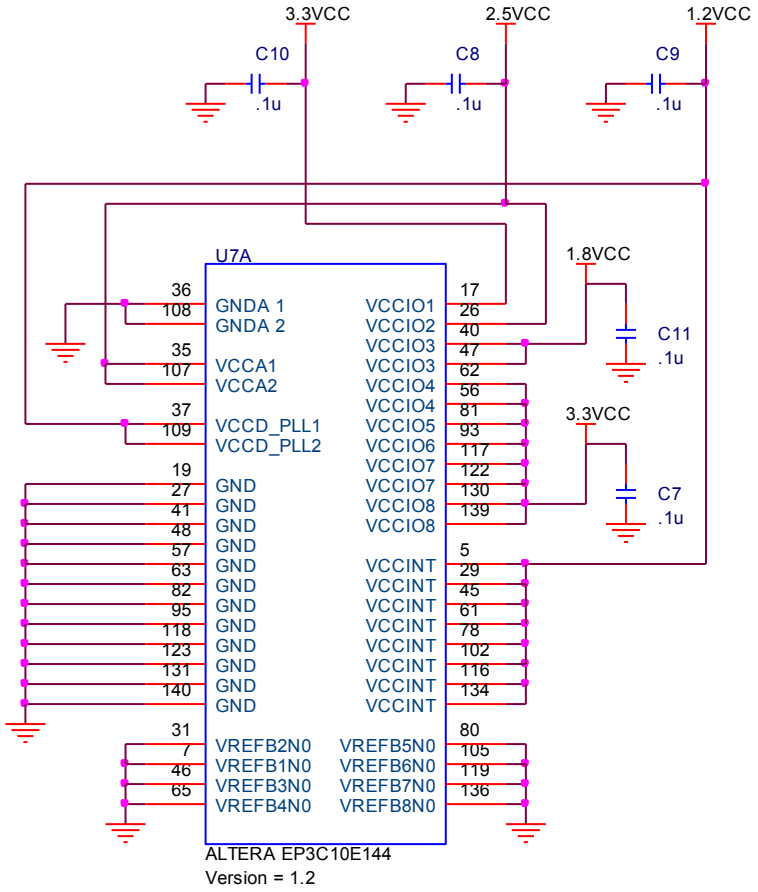


Figure 3. FPGA Power Pinouts

Four different DC voltage levels power the FPGA: 1.2V, 1.8V, 2.5V, and 3.3V. All supplies have .1uF capacitors connected to ground to filter out any AC noise. Internal logic voltages (VCCINT) and PLL digital power (VCCD_PLL) are all set to 1.2V. PLL analog power (VCCA) and I/O Bank 2 (VCCIO2) are set to 2.5V. I/O Bank 2 handles communications with the AFE over Low-voltage Differential Signaling (LVDS), a high speed communication protocol requiring 2.5V supply. I/O Bank 3 (VCCIO3) is set to 1.8V, the logic level used for serial communication with the AFE. All other I/O bank supplies are set to 3.3V. VREF pins are not used and tied to ground.

Section 2: I/O

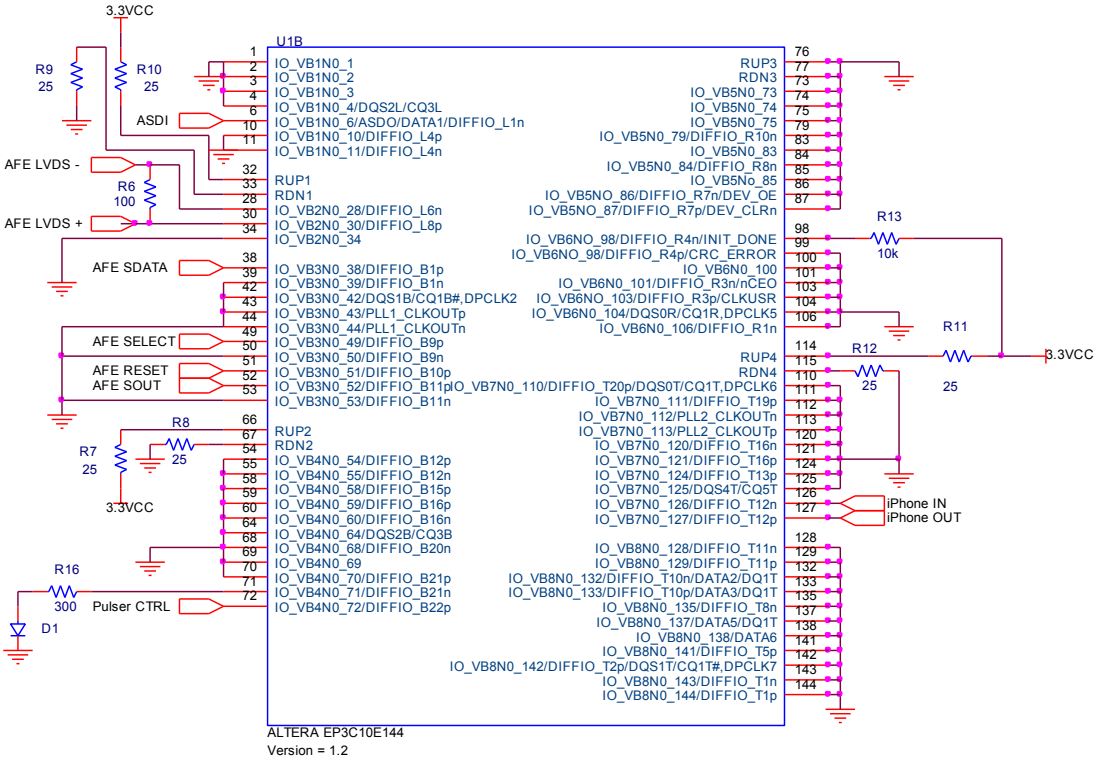


Figure 4. FPGA I/O Pinouts

The FPGA features eight I/O banks, five of which are utilized for our circuit. I/O Bank 1 is used solely for sending a control signal (ASDI) to the serial programming device to read out configuration data. I/O Bank 2 accepts LVDS waveform data from the AFE. A 100Ω resistor is connected between the positive and negative leads of the differential signal as recommended by Altera for signal stability. 25Ω pull-up and pull-down resistors are connected to RUP and RDN to enable on-chip termination, which improves signal clarity. I/O Bank 3 handles serial programming of the AFE using one input (AFE SDATA) and three outputs (AFE SELECT, AFE RESET, and AFE SOUT). I/O Bank 4 has two outputs: the 10MHz pulsing signal (Pulser CTRL) and an LED to indicate if a scan is in progress. I/O Bank 5 is unused. I/O Bank 6 is unused except for a required connection to 3.3V across a 10k resistor. I/O Bank 7 transmits and receives data from the iPhone. I/O Bank 8 is unused.

Section 3: Programming and Clocks

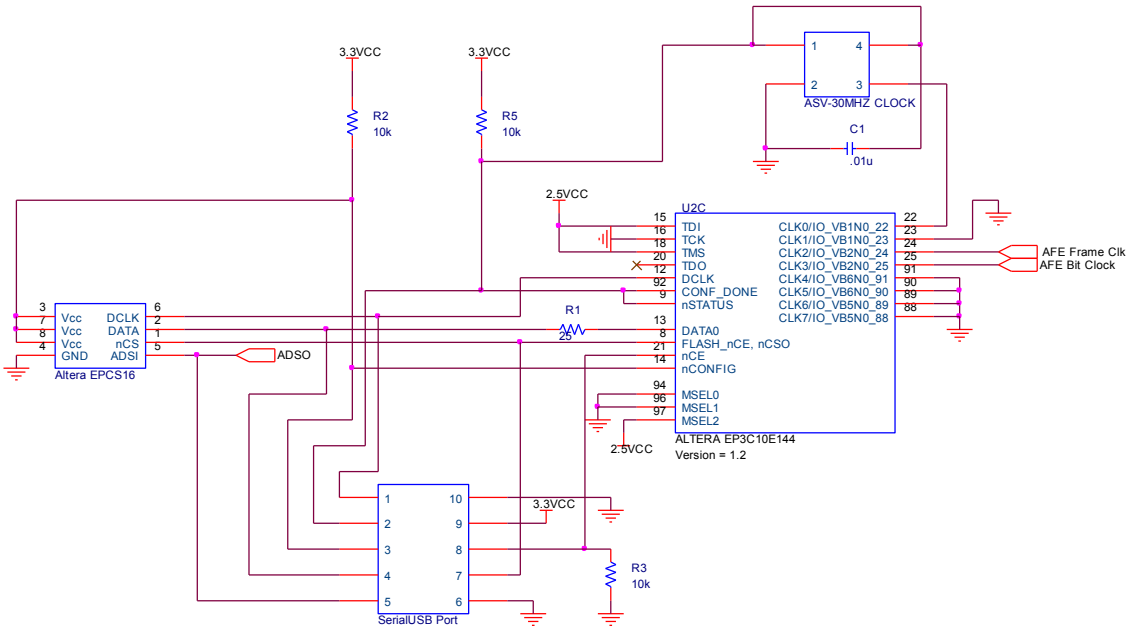


Figure 5. FPGA Programming and Clocks Pinouts

An ASV-30.000MHZ-EJ-T oscillator is used as a 30MHz clock for the FPGA and AFE ADC. This is the primary clock for the FPGA and I/O Bank 1. I/O Bank 2 receives two clock signals from the AFE to synchronize LVDS communication: a frame clock and bit clock. An Altera EPCS16 chip serves as the interface for Active Serial (AS) non-volatile programming of the FPGA. The chip can be programmed using Quartus II software and a Serial-USB Blaster cable, which connects to a 10-pin male connector on the board. Per Altera recommendations, 10k resistors are connected serially with voltage sources and a 25Ω resistor is connected serially on the DATA line. See [5] for the guide for connections between the FPGA and EPCS1.

Section 4: iPhone Communication

Data is sent to and from the iPhone over the headphone audio jack using a Manchester encoded signal. Manchester encoding allows for digital encoding with a sinusoidal analog signal. A positive voltage represents digital “1”, and negative voltage represents digital “0”. Since a long string of 1s or 0s would saturate the audio channel, each bit is encoded using a complete AC cycle as either “01” for 0 or “10” for 1. Data is transmitted according to the UART protocol in 10 bit packets, including 1 data byte, 1 start bit, and 1 stop bit. A test signal was generated from the iPhone and probed with an oscilloscope as shown below. This shows transmission of x02 with a start bit 1 and stop bit 0. When no data is being sent, the UART line is high and represented by a long string of 01s. The start bit creates a double baud length 1 pulse, resynchronizing the receiver with the incoming data byte. iPhone code libraries to produce and receive Manchester encoded audio are provided by University of Michigan’s Project HiJack [6]. This communication protocol was chosen for its simplicity over Bluetooth and Wifi, and due to the inaccessibility of the iPhone’s USB data protocol.

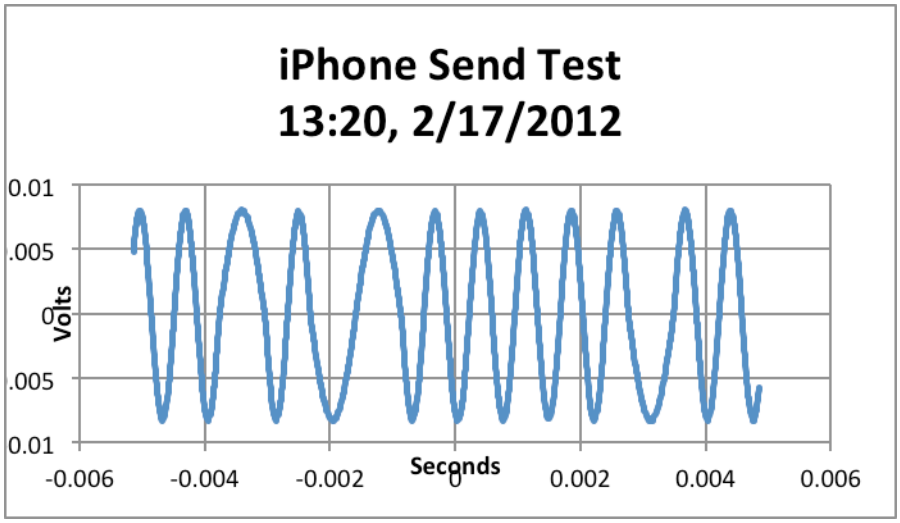


Figure 6. Sample Manchester Encoded x02 from iPhone Left Audio

Data Rate

The limiting factor for data transmission rate is the iPhone's audio sampling rate of 44.1 kHz, corresponding to 22.05 kbaud in Manchester encoding. The calculation below shows what this corresponds to in kB/sec.

$$Rate = \frac{(22050\,kBaud)(.8\,data\,/\,packet)}{8\,bits\,/\,byte} = 2.205\,kB\,/\,\sec$$

The faster data is transmitted, the higher the likelihood of dropped bits, so a safer data rate of 0.8kB/sec is assumed until further tests can be accomplished. This data rate corresponds to the ability to send approximately 1 ultrasound image per second to the iPhone. Calculations for the size of one ultrasound image are below.

$$Samples\ per\ image = \frac{30\,mm\ axial\ length}{.05\,mm\ desired\ resolution} = 600\,samples\,/\,image$$

$$Image\ Size = (600\,samples\,/\,image)(2\,bytes\,/\,sample) = 1.2\,kB\,/\,image$$

Sending Data from the iPhone

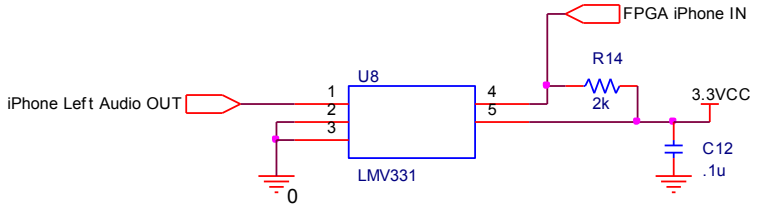


Figure 7. iPhone Receiver Circuitry

The Manchester encoded AC data signal is generated on the iPhone's left audio channel at a maximum V_{pp} of 2.76V. This signal must be converted to a digital signal with 3.3V logic before entering the FPGA. To accomplish this, an LMV331 comparator is used with a V_{ref} = 0V to convert positive voltages to 3.3V and negative voltages to 0V. At the suggestion of the manufacturer, a 2k pull-up resistor is used at the output and a .1uF capacitor eliminates noise at the supply. Simulation of this circuit operating is shown below with the analog input sinusoid in green and digital output signal in red.

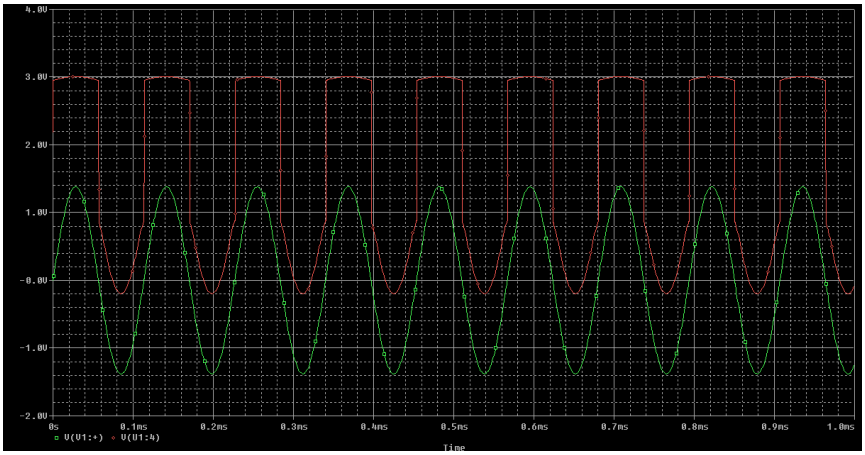


Figure 8. iPhone Receiver Circuitry PSpice Simulation

Sending Data from the FPGA

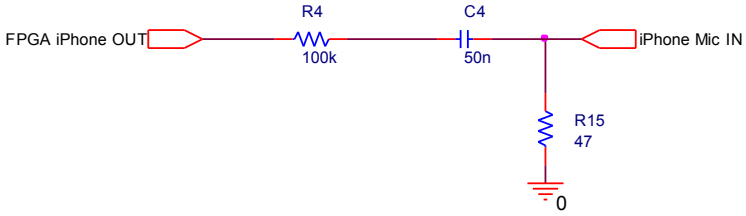


Figure 9. iPhone Transmission Circuitry

Manchester encoded data from the FPGA is a digital signal at 3.3V logic and must be converted to an AC signal. The signal will be received by the iPhone's microphone input, which expects AC signals with no DC offset and V_{pp} of less than 2mV. The 50nF capacitor in series AC couples the DC signal, and the two resistors attenuate the incoming signal using the voltage divider rule.

$$V_{pp,out} = (V_{pp,in})\frac{R_1}{R_1 + R_2} = (2.76V)\frac{47}{100k + 47} = 1.3mV$$

Simulation of this circuit is shown below with a 3.3V logic signal input in green and attenuated, AC coupled signal output in red.

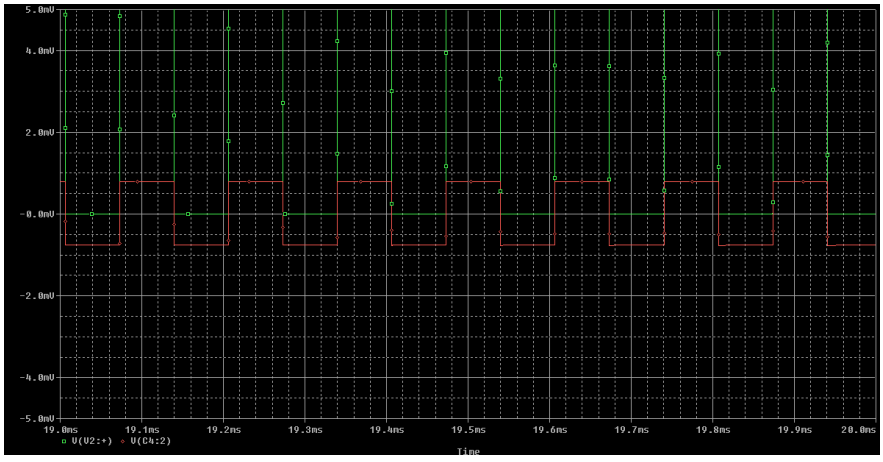


Figure 10. iPhone Transmission Circuitry PSpice Simulation

■ Power Electronics

A single lithium 9-volt battery will power the device's front-end circuitry. Due to the relative complexity of this circuitry, nine different voltage levels will require regulation: +30V, +10V, -10V, +5V, -5V, +3.3V, +2.5V, +1.8V, and +1.2V. The tree diagram below describes how these levels will be achieved.

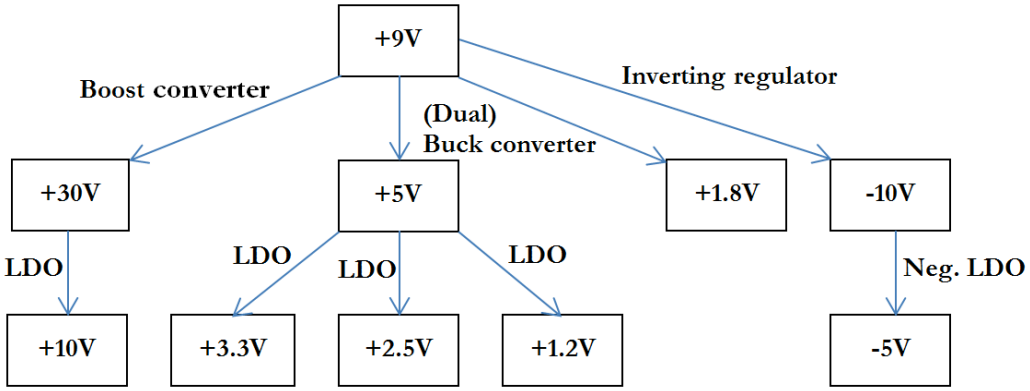


Figure 11. Voltage regulation tree diagram

The above approach was taken for several reasons:

- Boost converters, buck converters, and inverting regulators are much more complex to implement than linear regulators, but they provide significantly better conversion efficiency
- The analog front end's high-speed ADC (+1.8V) pulls a significant amount of current, compared to the other components, so we wanted to achieve high conversion efficiency for that voltage level
- We couldn't find a suitable LDO to regulate +1.2V from a +1.8V supply, so we chose to use the +5V supply, instead

In the end, we chose to implement to a scheme that would provide a fair tradeoff between energy efficiency and complexity. In order to get a rough estimate of how much power our front-end circuitry would draw, we examined each component's data sheet to make conservative approximations of current draw. These estimations are provided in the table below.

Table 1. Approximate current drawn by each front-end component

	+30V	+10V	-10V	+5V	-5V	+3.3V	+2.5V	+1.8V	+1.2V
FPGA	-	-	-	-	-	10mA	17mA	-	41mA
Analog Front End	-	-	-	-	-	9mA	-	400mA	-
T/R Switch	-	-	-	7mA	7mA	0.05mA	-	-	-
Transmit Pulser	3mA	14.5mA	14.5mA	-	3mA	0.05mA	-	-	-
Total	*3mA*	*14.5mA*	*14.5mA*	*7mA*	*10mA*	*19.1mA*	*17mA*	*400mA*	*41mA*

Using this information, the following calculations were made:

Approximate power drawn by major components:

$$P_{comp} = \sum_i |V_i| I_i \approx 1350\text{mW}$$

Approximate power dissipated in LDOs:

$$P_{LDO} = \sum (|V_H| - |V_L|) * I_L \approx 550\text{mW}$$

Approximate power dissipated in other converters (assume 85% efficiency):

$$P_{conv} = \sum (1 - 0.85) * |V_L| I_L \approx 150mW$$

Approximate total power drawn from 9V battery source:

$$P_{total} \approx P_{comp} + P_{LDO} + P_{conv} = 2{,}050mW$$

When drawing 500mA, the capacity of an Energizer lithium 9V battery is about 750mAh and operates at 7V. Given this information, the ultrasound device can last

$$t_{life} = \frac{Q_{capacity} V_{operating}}{P_{total}} \approx 2.6 \text{ hours}$$

Two and a half hours of battery life seems reasonable, considering that it's a portable ultrasound device, which would typically require a larger, rechargeable battery. In addition, it's worth emphasizing that these calculations were fairly conservative. For example, they don't account for the fact that our application only utilizes one of eight channels, since it's a one-dimensional scan.

As indicated in the voltage regulation tree above, our power electronics module consists of eight voltage converters/regulators. In order to simplify the complexity, we chose to employ Texas Instruments power management ICs. The selected chips are listed below:

- TPS61170 Boost Converter
- TPS54286 Dual Buck Converter
- TL497A Inverting Regulator
- TPS7A3001 Negative Linear Regulator
- TPS76912 Linear Regulator
- TPS76925 Linear Regulator
- TPS76933 Linear Regulator
- LP2985 Linear Regulator

TPS61170 Boost Converter

This boost converter will be used to step the 9V battery voltage up to +30V. Its schematic is provided below, followed by a design procedure for its external components and a PSpice simulation:

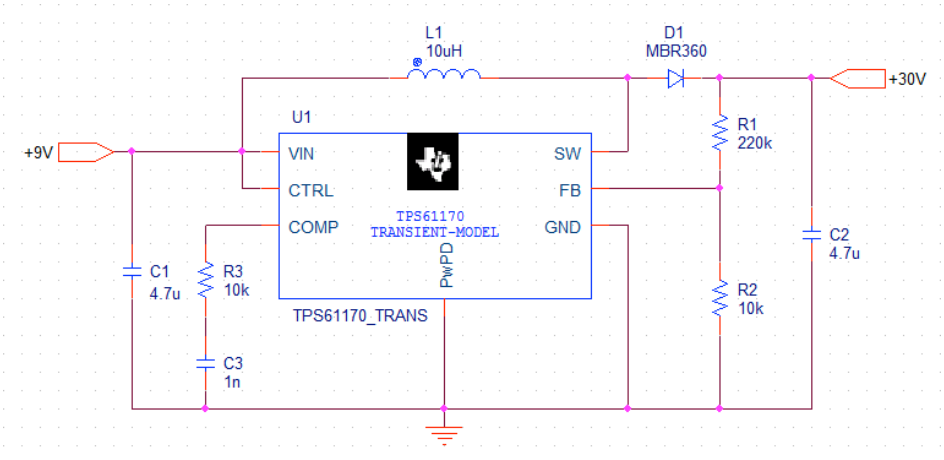


Figure 12. TPS61170 Boost Converter Schematic

The data sheet provided by Texas Instruments outlined a general design procedure and external circuit set-up. The values of each analog component were chosen as follows:

The output voltage is programmed by selecting R1 and R2 such that

$$V_{out} = V_{ref} \times \left(\frac{R1}{R2} + 1\right)$$

where V_{ref} is 1.229V and an optimal value for R2 is around 10kΩ. Thus, for an output voltage of 30V,

$$R1 = 10k\Omega \times \left(\frac{30V}{1.229V}\right) = 220k\Omega$$

All recommended inductors were 10μH, so that was a natural choice for L1. A Schottky rectifier with a reverse breakdown voltage of 40V was also recommended, so we chose one with 60V-rating because it was available at the ECE parts shop. Input capacitors in the range of 1μF to 4.7μF, and output ones in the range of 1μF to 10μF were recommended, so we chose both of them to be 4.7μF. Finally, an RC snubber of 10kΩ resistance and 100pF-10nF capacitance was recommended as optimal compensation, so our values were selected accordingly.

Since Texas Instruments provided a transient PSpice model of the TPS61170, we simulated our design. The results are shown below.

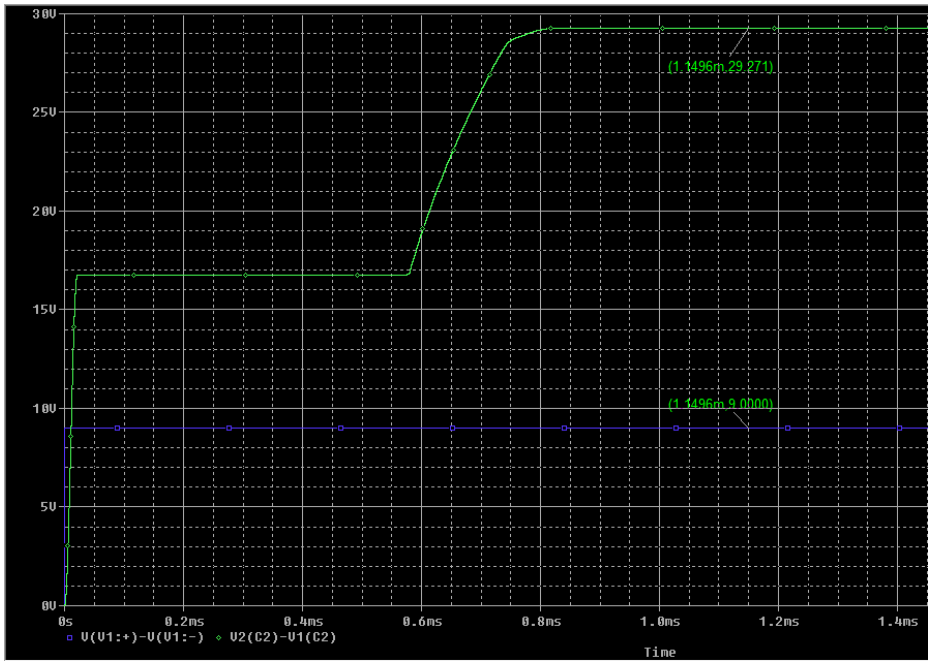


Figure 13. Simulation of the TPS61170 Boost Converter

As evident in the simulation, the 9V input voltage was successfully converted to approximately +30V.

TPS54286 Dual Buck Converter

This boost converter will be used to step the 9V battery voltage down to +5V and +1.8V. Its schematic is provided below, followed by a design procedure for its external components and a PSpice simulation:

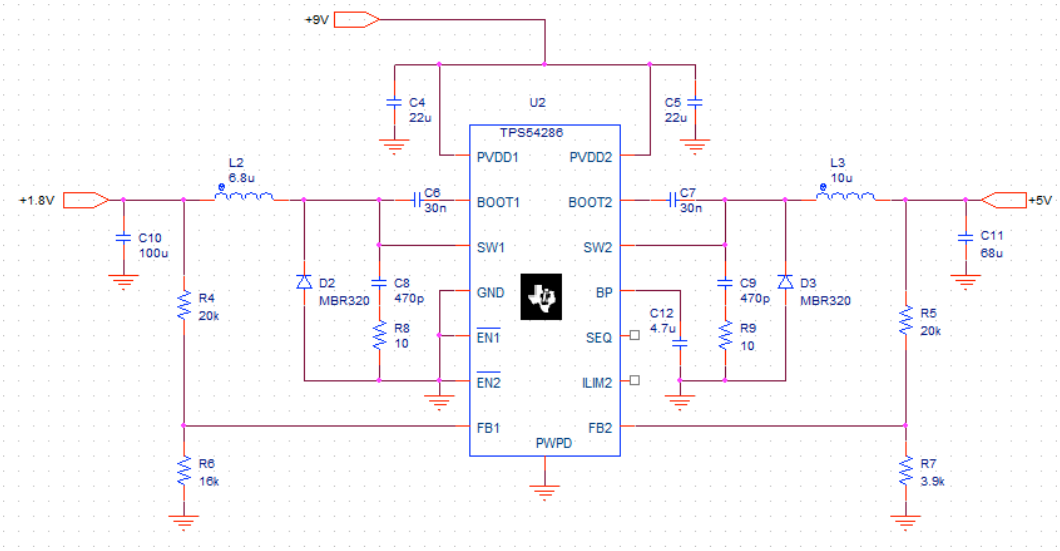


Figure 14. TPS54286 Dual Buck Converter Schematic

The data sheet provided by Texas Instruments outlined a general design procedure and external circuit set-up. The values of each analog component were chosen as follows:

The minimum duty cycle was found by

$$\delta_{min} = \frac{V_{OUT} + V_D}{V_{IN(max)} + V_D}$$

where V_D is the forward-bias voltage drop across the Schottky rectifier, 0.5V.
For the +5V and +1.8V designs, the minimum duty cycles were

$$\delta_{min,5V} = \frac{5V + 0.5V}{9.6V + 0.5V} = 54.5\%$$

$$\delta_{min,1.8V} = \frac{1.8V + 0.5V}{9.6V + 0.5V} = 22.8\%$$

In selecting appropriate inductors, we chose a maximum ripple current of 400mA and noted that the TPS54286 has a fixed switching frequency of 600kHz.

$$L = \frac{V_{IN(max)} - V_{OUT}}{I_{RIPPLE} \times f_{SW}} \times \delta_{min}$$

$$L_{5V} = \frac{9.6V - 5V}{0.4A \times 600kHz} \times 0.545 = 10.45\mu H \rightarrow 10\mu H$$

$$L_{1.8V} = \frac{9.6V - 1.8V}{0.4A \times 600kHz} \times 0.228 = 7.41\mu H \rightarrow 6.8\mu H$$

Since the breakdown voltage of the Schottky diodes had to only be greater than $1.2V_{IN}$, we chose the 1N5820, which has 20V reverse-breakdown voltage.
The output voltage was set by using the following relation:

$$R2 = \frac{0.8 \times R1}{V_{OUT} - 0.8V}$$

where R1 and R2 should be less than 50kΩ. In order to conform to standard resistor values, we ended up choosing R4=R5=20kΩ, R6=16kΩ, and R7=3.9kΩ.
To select input, bootstrap, and BP capacitors, we followed those chosen in the example designs provided. As a result, we set C1=C2=22µF, C3=C4=30nF, and C9=4.7µF.
To select the output capacitors, the datasheet provided the following equation:

$$C_{OUT} = \frac{1}{4\pi^2 f_{RES}{}^2 L}$$

Examining provided documentation, the resonant frequency occurred at approximately 6kHz. Therefore,

$$C_{OUT,5V} = \frac{1}{4\pi^2 (6kHz)^2 (10\mu H)} = 70\mu F \rightarrow 68\mu F$$

$$C_{OUT,1.8V} = \frac{1}{4\pi^2 (6kHz)^2 (6.8\mu H)} = 103.5\mu F \rightarrow 100\mu F$$

Fortunately, this converter employed internal compensation, so no compensation network was required. However, the documentation suggested adding an RC snubber at the SW pins to reduce ringing on the output. Following design examples, we chose R5=R6= 10Ω and C5=C6=470pF.

Since Texas Instruments provided a transient PSpice model of the TPS54286, we simulated our design. The results are shown below.

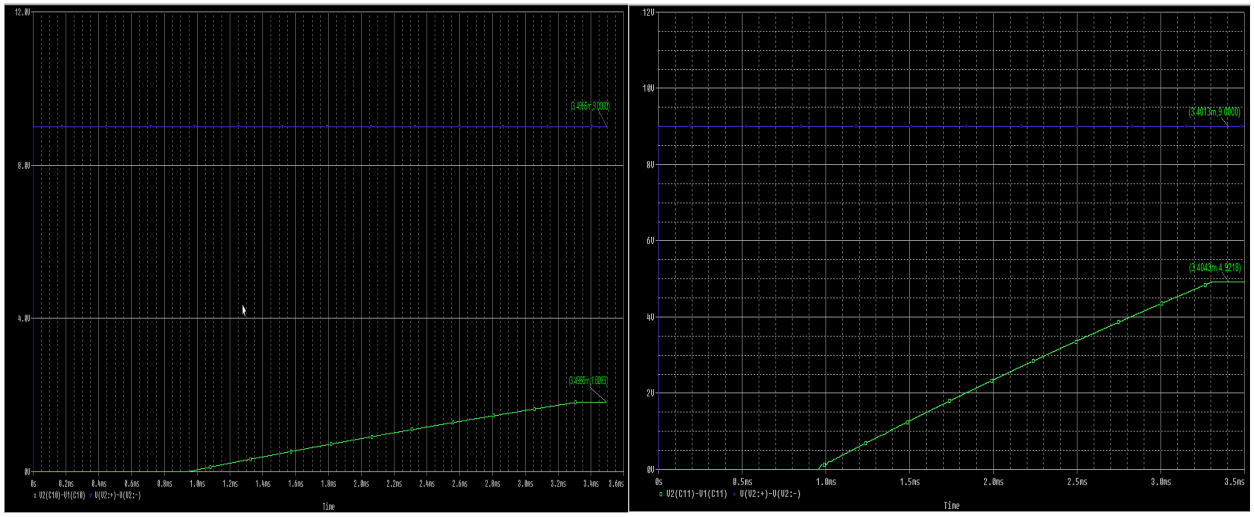


Figure 15. Simulations of the TPS54286 Dual Buck Converter

As evident in the simulation, the 9V input voltage was successfully converted to approximately +1.8V and +5V.

TL497A Inverting Regulator

This inverting regulator will be used to convert the 9V battery voltage to -10V. Its schematic is provided below, followed by a design procedure for its external components. Unfortunately, no PSpice model was available.

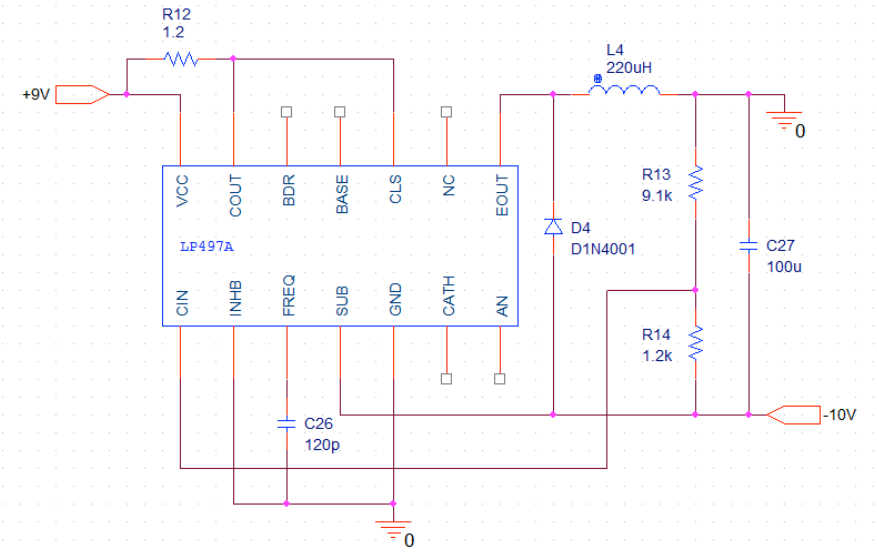


Figure 16. LP497A Inverting Regulator Schematic

The data sheet provided by Texas Instruments outlined a general design procedure and external circuit set-up. The values of each analog component were chosen as follows:

The following formulas were provided and employed in designing the external components for this regulator:

$$I_{(PK)} = 2I_{O(max)}\left[1 + \frac{|V_O|}{V_I}\right]$$

$$L(\mu H) = \frac{V_I}{I_{(PK)}} \times t_{on}(\mu s)$$

$$C_T(pF) = 12t_{on}(\mu s)$$

$$R1 = (|V_O| - 1.2V)k\Omega$$

$$R_{CL} = \frac{0.5V}{I_{(PK)}}$$

$$C_O(\mu F) = t_{on}(\mu s)\frac{\left[\frac{V_I}{|V_O|}I_{(PK)} + I_O\right]}{V_{RIPPLE(PK)}}$$

Choosing based on recommendations, I selected I_O=100mA, V_{RIPPLE}=50mV, t_{on}=10µs, and R14=1.2kΩ. This yielded L=220µH, C_T=120pF, R1=9.1kΩ, R_{CL}=1.2Ω, and C_O=100µF.

Linear Regulators

Five linear regulators will be used to convert regulated voltage levels to even lower voltages. Specifically, the negative LDO, TPS7A3001, will step the -10V down to -5V; the linear regulators, among the TPS769xx family, will step the +5V down to +3.3V, +2.5V, and +1.2V; the higher-voltage linear regulator, LP2985, will step the +30V down to +10V. The schematic of each regulator is provided below, followed by simple design procedures. Unfortunately, no PSpice models were available.

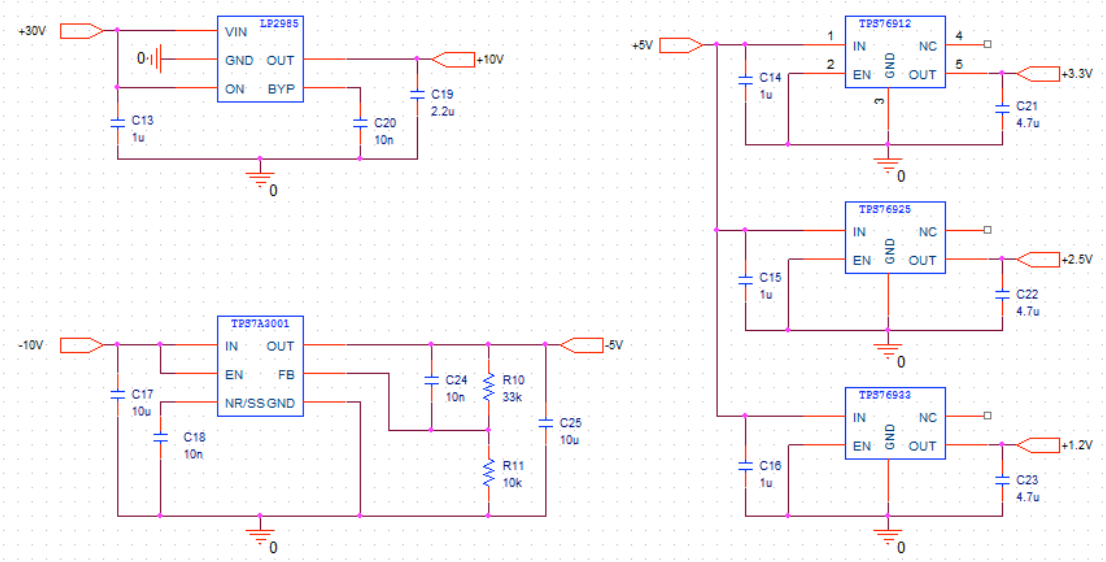


Figure 17. Linear Regulators Employed in the Power Management Module

The data sheets provided by Texas Instruments outlined general design procedures and external component wiring. Fortunately, all but the TPS7A3001 were fixed-output regulators, so only input and output capacitors were needed for them.

In the case of the TPS7A3001, the only extra components to select were voltage dividing resistors. These resistors were to be chosen such that

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where

$$\frac{V_{OUT}}{R1 + R2} \geq 5\mu A$$

Choosing R2=10kΩ, we calculated that a resistance of R1=33kΩ would be required to regulate -5V.

For input and output capacitance selections among all of the regulators, we simply adhered to the values recommended by Texas Instruments.

■ LM96550 Ultrasound Pulser

The transmit pulser is the only component in the transmitter circuit. Its primary function is to accept a digital pulse from a controller (in our case, the FPGA), and relay a high-voltage pulse to the transducer probe. The LM96550's design includes eight channels, as well as positive and negative high-voltage supplies up to +50V and -50V, respectively. Since we are implementing a one-dimensional scan, only one channel will be utilized. In addition, no complex beamforming (typical of multi-dimensional ultrasounds) will be required, so we can simply send one positive pulse. This allows us to avoid the need of a negative high voltage. For the positive high voltage, however, the DGH probe's specifications require that the pulse voltage be no higher than 32V. In accordance with this, we've selected +30V as the high-voltage supply. In order to operate correctly, the pulser also requires +10V and –10V power supplies, a -5V voltage as the negative high voltage (cannot simply ground it), and a +3.3V logic voltage level. Other than the positive digital pulse input from the FPGA (Pin0), all other digital input lines are grounded. Likewise, aside from channel 1's high-voltage output, all other high-voltage outputs are left floating. Finally, the enable and mode pins are tied high to always keep the chip enabled and allow for maximum output current. A PSpice model of the LM96550 does not exist, unfortunately, but the pin assignment schematic is illustrated below.

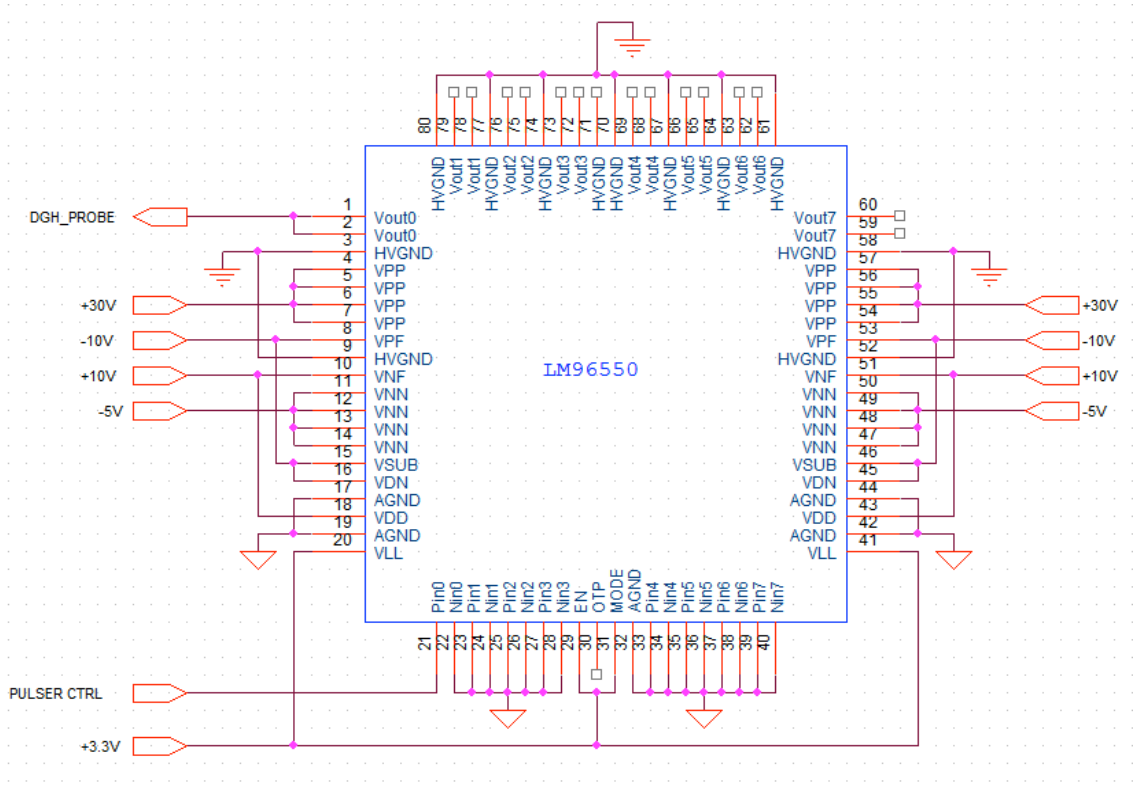


Figure 18. LM96550 Transmit Pulser Schematic

- **DGH Ultrasound Probe**

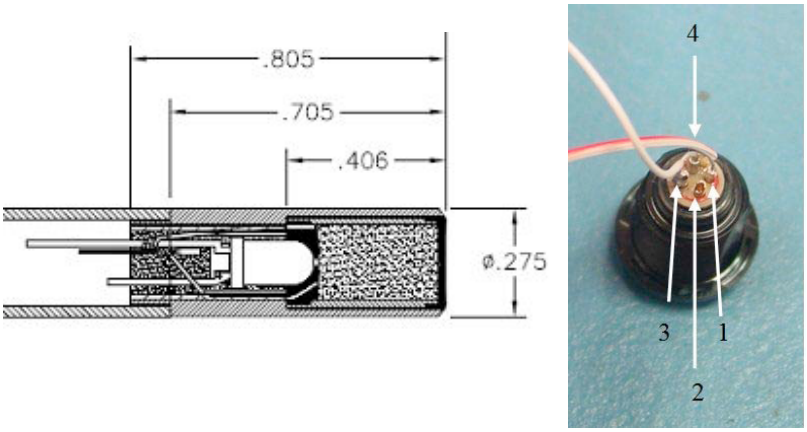


Figure 19. DGH Probe Dimensions and Pinouts

The DGH 6000 Scanmate A transducer consists of a single piezo-ceramic element that runs at a center frequency of 10.0 MHz nominal. It focuses an acoustic beam at 23.0 mm nominal and has a circular patient contact area 0.275" in diameter. It also contains a fixation LED to help center the patient's iris upon examination.

Pin Outs:
Pin 1: 3.3V LED power (connected to 100Ohm resistor in series to limit current)
Pin 2: Rx Pulser Circuit Input
Pin 3: GND
Pin4: NC

Simulations:
Impedance measurements were taken for the DGH ultrasound probe by creating a 50nS width, 5mS period pulse on a pulse generator, measuring the voltage (V_r) across a known series resistance (50.15Ohm) and the output voltage (V_p). V_r and V_p were measured to be 3.625V and 4.00V, respectively. Knowing this, the magnitude of the input impedance (Z_p) of the probe can be calculated as follows:

$$I = \frac{Vr}{R} = \frac{3.625\,V}{50.156\Omega} = 0.0723A$$

$$Z_p = \frac{Vp}{I} = \frac{4.00V}{00723A} = 55.33\,\Omega$$

- **TX810 T/R Switch**

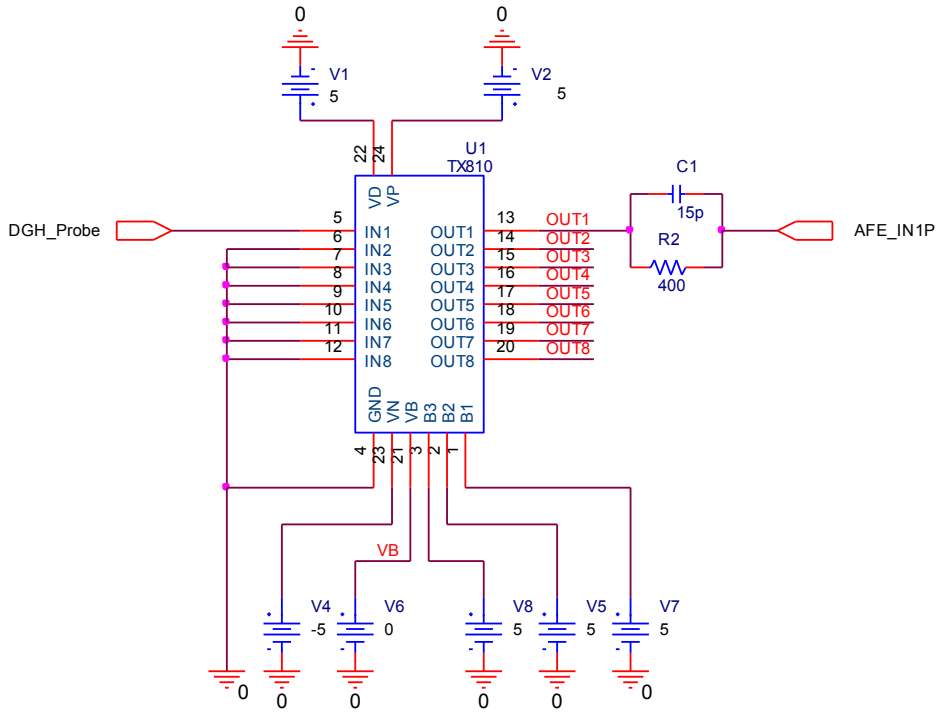


Figure 20. T/R Switch Schematic

The TX810 chip is an 8-channel, programmable T/R switch for medical ultrasound applications. Internally, it consists of a diode bridge, bias network, clamp diodes, and logic controller. This T/R switch can be programmed to allow for different bias currents, but for our purposes, the mode that allows for the minimum amount of insertion loss is the most ideal (B1,B2,B3 inputs set to HIGH).

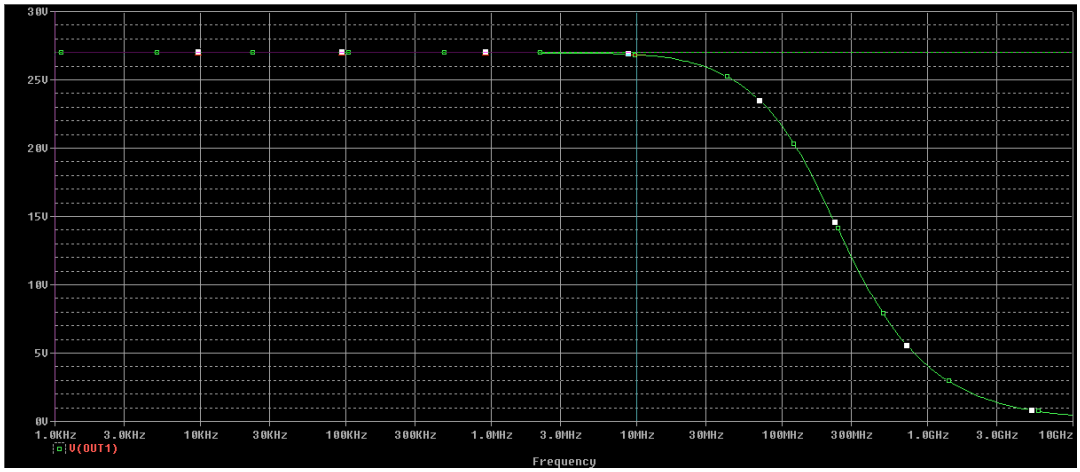


Figure 21. T/R Switch PSpice Simultion

The above simulation illustrates that the T/R chip is capable of receiving input pulses in the 1kHz to 15MHz range with little insertion loss. Since we are operating our device at a frequency of ~10MHz, one can see that the amount of internal signal attenuation from the input to the output is very minute at this input frequency.

- **AFE5801 Analog Front End**

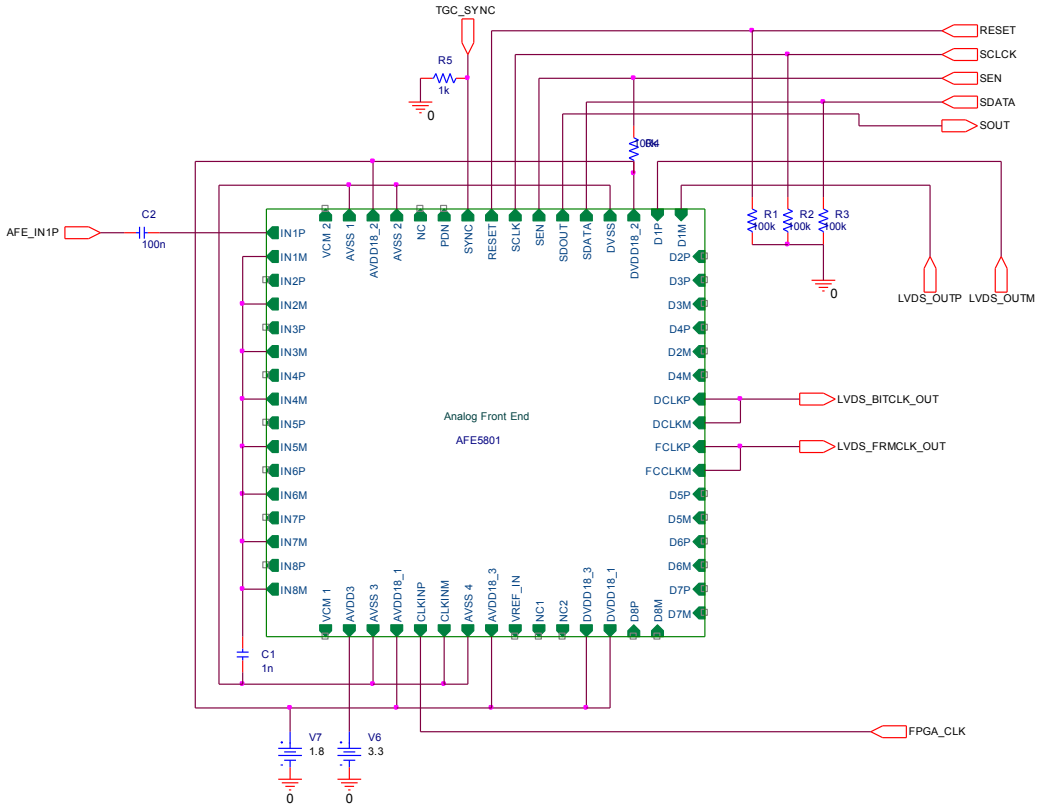


Figure 22. AFE Schematic

The AFE5801 is a low-power, CMOS-based analog front-end chip that includes an 8-channel variable-gain amplifier (VGA) and an 8-channel, 12bit, high-speed analog-to-digital converter (ADC) that is based on a switched-capacitor design. Since our design is only uses a single element transducer and makes a 1-D measurement, only one of these channels is implement, while pin-outs of other channels are grounded, or left floating.

TI does not provide PSPICE models for this chip. The above high-level schematic was built to show the pin-outs and connections between the T/R switch, AFE, and the FPGA board, as well as some DC block capacitors and pull-up/pull-down resistors specified by TI that are needed to drive some inputs/outputs. TI does provide documentation regarding the kind of output characteristics this AFE chip provides and the characteristic gain that the LNA part of the chip can provide, and they may be used for comparisons to measured outputs.

Programming the modes of operation for the AFE5801 occurs over a Serial Peripheral Interface bus and is controlled by the FPGA. Upon power-up, the chip's internal registers are initialized to the default (zero) value by applying a positive pulse to the Reset pin. The SPI bus is formed by the following pins: (SEN)', SCLK, SDATA, and RESET. Serial shifting of bits on the SDATA line into the device occur when (SEN)' is set to low. Input bits on the SDATA line are latched on rising edges of SCLK, loading a new instruction to completion on every 24th rising edge. The first 8 of the 24 bits comprise of a register address, while the remaining 16 comprise of the data to be loaded onto the addressed register. The following diagram illustrates this process:

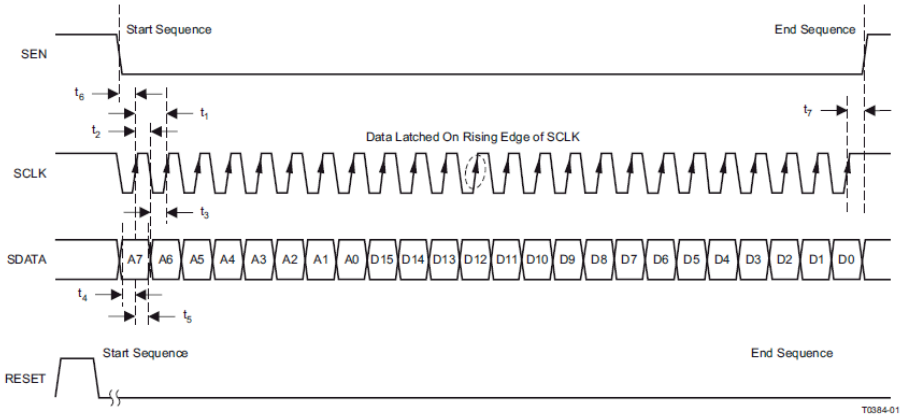


Figure 23. Timing Diagram for AFE Serial Data Protocol

Internal registers are divided into two groups: general-purpose registers and gain control operation registers. Access to gain control registers is granted when bit 2 of address zero (labeled "TGC_REGISTER_WREN" is set to 1. Various modes of operation are adjusted in this way.

On the output end of the AFE, sampled data from ADC is sent to the FPGA using Low Voltage Differential Signaling (LVDS). The LVDS output is sent out to the FPGA on pins D1P/M, along with LVDS frame clocks FCLKP/M and bit clocks DCLKP/M. In order to properly convert the analog input from the LNA side of the chip to digital data the sampling rate of our ADC can simply be calculated at the Nyquist Rate:

$$f_N = 2B = 2(10MHz) = 20MHz = 20MSPS$$

Achieving this data rate for the 10MHz probe operating frequency ensures a resolution of 0.075mm, well below our target accuracy of 0.1mm. Since our anti-aliasing filter will not attenuate signals above 10MHz perfectly, the next highest sampling rate is chosen instead (30MHz). Since each sample is 12 bits in resolution, the actual sampling rate equals 360MSPS – necessitating the use of an FPGA with LVDS to buffer data.

- **Software Flow Diagrams**

FPGA

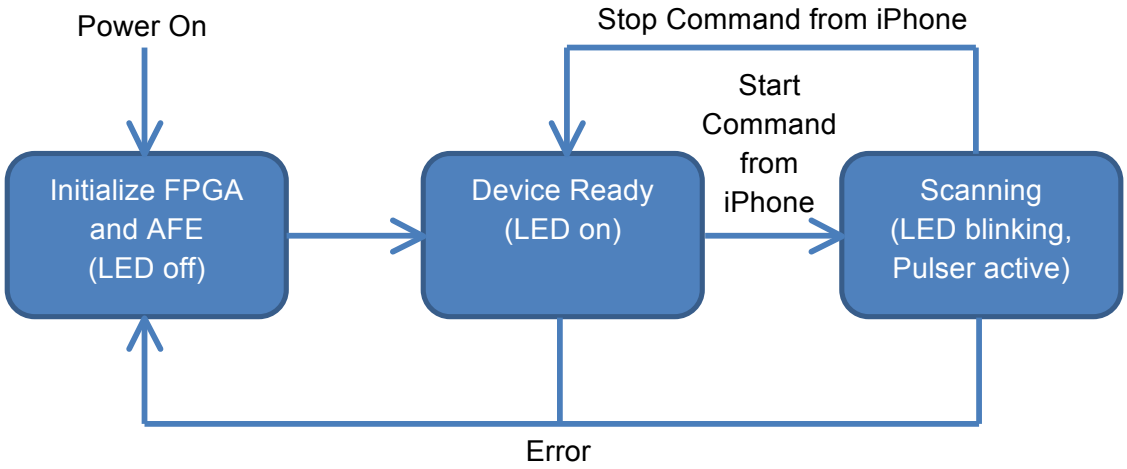


Figure 24. FPGA Software Flow Diagram

iPhone

The application will consist of a startup view (1) followed by two views accessible by a tab bar controller: patient data (2) and saved scan options (3). When a scan is initiated, a separate view will appear (4).

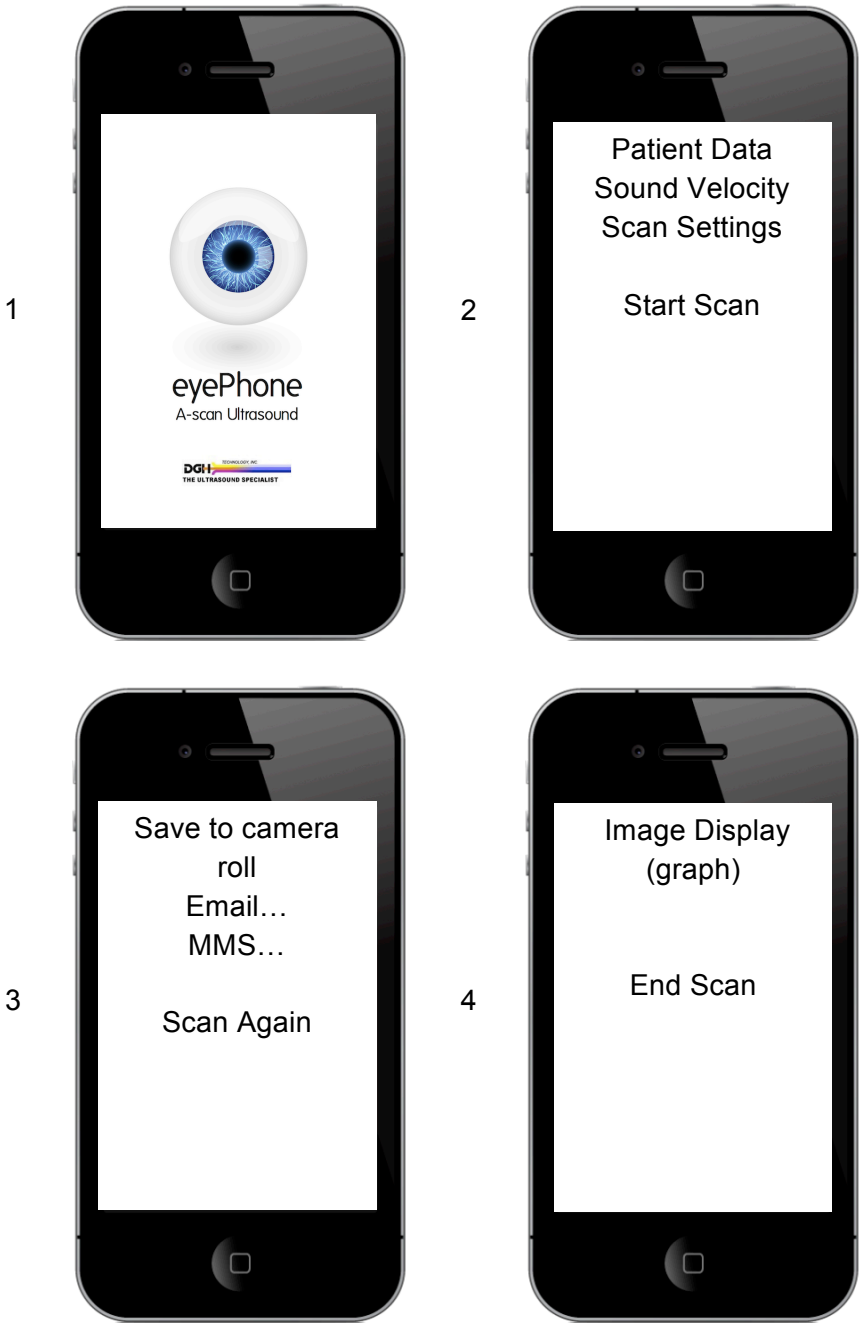


Figure 25. iPhone Software Flow Diagram

d. Performance Requirements:

- Resolution of 0.1mm or less AEL measurements
- Transmitted Pulse frequency of 9.5-10.5 MHz
- Provide at least one A-scan image to be displayed by the iPhone per second
- Low power consumption to operate on one 9V battery

3. Verification

a. Testing Procedure

Probe Requirements	Verification
1. Fixation LED must light up. a. LED must draw 16mA or less from 3.3V Power Electronics b. Probe must be attached to circuit ground	1. Observe that the Fixation LED lights up a. A current draw of 16mA or less is measured across the 100Ohm series resistor. b. The probe nodes are correctly connected to 3.3V and ground
2. Transducer must convert 30V pulse input into sound wave oscillating at 9.5-10.5 MHz	2. Use pulse generator to drive transducer using a 30V, 10MHz input pulse. Observe return echo voltage signal on an oscilloscope, noting their peak amplitude values and a nominal frequency of 9.5-10.5 MHz.
3. Transducer must convert return echo sound waves to voltage signal.	3. Use pulse generator to drive transducer using a 30V, 10MHz input pulse. Observe return echo voltage signal on an oscilloscope, noting their peak amplitude values and the nominal frequency.
Contingency Plan: Temporarily use Storz probe until DGH Technologies can send a replacement ultrasound probe.	

T/R Switch Requirements	Verification
1. Diode Bridge and Voltage Clamp must prevent high voltage input spikes (greater than 2 Vpp) to leak to the output.	1. Apply 30V pulse to the input end of Measure output voltage on DMM. Verify that the output signal does not exceed 2 Vpp.
Contingency Plan #1: Replace malfunctioning TX810 chip with spare TX810 Chip. *Contingency Plan #2: Implement LM96530 T/R Chip.*	

AFE Requirements	Verification
1. Input SPI data on SDATA bus must have: a. a logic level high voltage between 1.4-3.6V b. a logic level low voltage of less than 0.8V	1. Use a logic analyzer to observe data communications on the SPI bus. Verify logic levels are: a. between 1.4-3.6V for a high data bit b. less than 0.8V for a low data bit
2. SDATA must correctly latch on the rising edge of SCLK.	2. Use a logic analyzer to observe data communications on the SPI bus. Verify SDATA bits correctly latch on the rising edge of SCLK.
3. Output LVDS signal should have a common mode output voltage of 0.9-1.5V	3. Measure output voltage at nodes D1P and D1M on a DMM. Voltage output should read between 0.9-1.5V.
4. Output LVDS signal should maintain a data rate of between 25-35 MSPS .	4. Use a digital waveform analyzer to observe data communications on the LVDS bus. Verify data rate of between 25-35 MSPS.
Contingency Plan #1: Replace malfunctioning AFE5801 chip with spare AFE5801 Chip. *Contingency Plan #2: Implement LM96551 Analog Front End Chip.*	

FGPA Requirements	Verification
1. Clock must operate properly a. 30 MHz frequency ±1% b. $3.3V_{pp}$ ±5%	1. Connect oscillator pins to Vcc and GND. Probe clock output with oscilloscope. a. A clock frequency of 30 MHz frequency ±1% is measured at the clock output b. Clock logic level of $3.3V_{pp}$ ±5% is measured at the clock output.
2. Serial Programmer must program FPGA correctly with Active Serial (AS) programming.	2. Connect USB Blaster cable to board using 10pin connector. Use Quartus II software to load a sample program onto FPGA using AS programming. Quartus II loads the program successfully with no errors.
3. FPGA must receive and buffer incoming AFE data correctly.	3. Implement test RAM array (8x12bit) on FPGA. Send eight 12bit frames of known test data over LVDS protocol at 360MSPS into RAM. Memory array is read out correctly in 1bit increments to the FPGA's LED.
4. FPGA must correctly interpret Manchester encoded command signals sent at 8820 baud rate or higher. c. FPGA LED is turned on when x01 is received. d. FPGA LED is turned off when x02 is received.	4. Setup signal generator to make Manchester encoded bytes of x01 and x02 using an AC signal of 8820 baud and $2.76V_{pp}$. a. LED turns on when x01 is sent from signal generator. b. LED turns off when x02 is sent from signal generator.
5. FPGA must correctly send Manchester encoded data at 8820 baud rate or higher. a. DC offset of sent signal is within ±0.5mV. b. V_{pp} of sent signal is between 1mV and 2mV. c. Data is correctly encoded.	5. Connect oscilloscope to FPGA signal output. Send a known Manchester encoded byte using a digital signal at 8820 baud repeatedly once per second from the FPGA. Repeat this verification for several known bytes. a. DC offset of sent signal is measured on oscilloscope to be within ±0.5mV. b. V_{pp} of sent signal is measured on oscilloscope to be between 1mV and 2mV. c. Data byte waveform seen on oscilloscope is correct Manchester encoded byte.
6. FPGA must correctly send digital pulses to the Pulser CTRL line. a. V_p of pulse is 3V ±5%. b. Pulse width is 50ns ±1%.	6. Connect oscilloscope to Pulser CTRL signal output. Send pulse signal from FPGA repeatedly at a frequency of 1Hz. a. V_p of pulse measured with oscilloscope is 3V ±5%. b. Pulse width measured with oscilloscope is 50ns ±1%.
Contingency Plan: Use Altera DE2 Board instead of Cyclone III board.	

Transmit Pulser Requirements	Verification
1. The Vout0 node transmits a nominal +30V, 50ns-wide pulse upon receiving a 50ns-wide digital pulse on its Pin0 node.	1. Using a pulse generator, send a 50ns-wide pulse of +3.3V amplitude to Pin0. Verify that a +30V, 50ns-wide pulse is instantaneously transmitted from Vout0.
Contingency Plan: Replace malfunctioning Transmit Pulser, or use a different Transmit Pulser (TX734).	

Power Electronics Requirements	Verification
1. a. 9V lithium battery must provide a voltage between +6.5V and +9.5V b. Battery must be connected to the 30V boost converter c. Battery must be connected to the 5V buck converter d. Battery must be connected to the 1.8V buck converter e. Battery must be connected to the -10V inverting converter	1. a. A voltage between +6.5V and +9.5V is measured across the battery's terminals. b. A voltage between +6.5V and +9.5V is measured at the input node of the 30V boost converter. c. A voltage between +6.5V and +9.5V is measured at the input node of the 5V buck converter. d. A voltage between +6.5V and +9.5V is measured at the input node of the 1.8V buck converter. e. A voltage between +6.5V and +9.5V is measured at the input node of the -10V inverting converter.
2. a. The output node of the 30V boost converter must regulate a nominal voltage of +30V, within a tolerance of ±5% b. Boost converter must be connected to the Transmit Pulser c. Boost converter must be connected to the 10V LDO Regulator	2. a. A voltage between +28.5V and +31.5V is measured at the output node of the 30V boost converter. b. A voltage between +28.5V and +31.5V is measured at the VPP nodes of the Transmit Pulser. c. A voltage between +28.5V and +31.5V is measured at the input node of the 10V LDO Regulator.
3. a. The output node of the 5V buck converter must regulate a nominal voltage of +5V, within a tolerance of ±5% b. Buck converter must be connected to the T/R Switch c. Buck converter must be connected to the 3.3V LDO Regulator d. Buck converter must be connected to the 2.5V LDO Regulator e. Buck converter must be connected to the 1.2V LDO Regulator	3. a. A voltage between +4.75V and +5.25V is measured at the output node of the 5V buck converter. b. A voltage between +4.75V and +5.25V is measured at the VP node of the T/R Switch. c. A voltage between +4.75V and +5.25V is measured at the input node of the 3.3V LDO Regulator. d. A voltage between +4.75V and +5.25V is measured at the input node of the 2.5V LDO Regulator. e. A voltage between +4.75V and +5.25V is measured at the input node of the 1.2V LDO Regulator.
4. a. The output node of the 1.8V buck converter must regulate a nominal voltage of +1.8V, within a tolerance of ±5% b. Buck converter must be connected to the AFE c. Buck converter must be connected to the FPGA	4. a. A voltage between +1.71V and +1.89V is measured at the output node of the 1.8V buck converter. b. A voltage between +1.71V and +1.89V is measured at the AVDD18 and DVDD18 nodes of the AFE. c. A voltage between +1.71V and +1.89V is measured at the VCCIO3 node of the FPGA.
5. a. The output node of the -10V inverting converter must regulate a nominal voltage of -10V, within a tolerance of ±5% b. Inverting converter is connected to the Transmit Pulser	5. a. A voltage between -9.5V and -10.5V is measured at the output node of the -10V inverting converter. b. A voltage between -9.5V and -10.5V is measured at the VPF, VDN, and VSUB nodes of the Transmit Pulser.
6. a. The output node of the 10V LDO Regulator must regulate a nominal voltage of +10V,	6. a. A voltage between +9.5V and +10.5V is measured at the output node of the 10V LDO Regulator.

within a tolerance of ±5% b. LDO Regulator is connected to the Transmit Pulser	b. A voltage between +9.5V and +10.5V is measured at the VNF and VDD nodes of the Transmit Pulser.
7. a. The output node of the 3.3V LDO Regulator must regulate a nominal voltage of +3.3V, within a tolerance of ±5% b. LDO Regulator must be connected to the FPGA c. LDO Regulator must be connected to the AFE d. LDO Regulator must be connected to the T/R Switch e. LDO Regulator must be connected to the Transmit Pulser	7. a. A voltage between +3.135V and +3.465V is measured at the output node of the 3.3V LDO Regulator. b. A voltage between +3.135V and +3.465V is measured at the VCCIO1, VCCIO4, VCCIO5, VCCIO6, VCCIO7, VCCIO8, RUP1, RUP2, and RUP4 nodes of the FPGA. c. A voltage between +3.135V and +3.465V is measured at the AVDD node of the AFE. d. A voltage between +3.135V and +3.465V is measured at the VD node of the T/R Switch. e. A voltage between +3.135V and +3.465V is measured at the VLL, EN, and MODE nodes of the Transmit Pulser.
8. a. The output node of the 2.5V LDO Regulator must regulate a nominal voltage of +2.5V, within a tolerance of ±5% b. LDO Regulator must be connected to the FPGA	8. a. A voltage between +2.375V and +2.625V is measured at the output node of the 2.5V LDO Regulator. b. A voltage between +2.375V and +2.625V is measured at the VCCIO2, VCCA1, VCCA2 nodes of the FPGA.
9. a. The output node of the 1.2V LDO Regulator must regulate a nominal voltage of +1.2V, within a tolerance of ±5% b. LDO Regulator must be connected to the FPGA	9. a. A voltage between +1.14V and +1.26V is measured at the output node of the 2.5V LDO Regulator. b. A voltage between +1.14V and +1.26V is measured at the VCCINT, VCC_PLL1, and VCC_PLL2 nodes of the FPGA.
10. a. The output node of the -5V Negative Regulator must regulate a nominal voltage of -5V, within a tolerance of ±5% b. Negative Regulator must be connected to the T/R Switch c. Negative Regulator must be connected to the Transmit Pulser	10. a. A voltage between -4.75V and -5.25V is measured at the output node of the -5V Negative Regulator. b. A voltage between -4.75V and -5.25V is measured at the VN node of the T/R Switch. c. A voltage between -4.75V and -5.25V is measured at the VNN node of the Transmit Pulser.
Contingency Plan #1: Replace malfunctioning power electronics IC. *Contingency Plan #2: Choose a different power electronics IC.* *Contingency Plan #3: If a DC/DC converter continues to fail, choose to use a regulator instead; if a regulator continues to fail, choose to use a DC/DC converter instead.*	

iPhone 4S Requirements	Verification
1. Device must be charged above 50%.	1. Go to iPhone settings and turn on battery percentage under General->Usage. Verify percentage is above 50%. If not, charge device.
2. iPhone must correctly interpret Manchester encoded data received at 8820 baud rate or higher.	2. Setup signal generator to make a Manchester encoded byte of xA9 using an AC signal of 8820 baud and 1.5mV_{pp} with 0V DC offset. Connect the signal generator to the iPhone's microphone input. The iPhone will correctly display xA9 to the screen.
3. iPhone must correctly send Manchester encoded command signals at 8820 baud rate or higher. a. DC offset of sent signal is within ±0.5mV. b. V_{pp} of sent signal is 2.76V_{pp} ±5%. c. Data is correctly encoded.	3. Connect oscilloscope to iPhone left audio output. Turn iPhone volume to 100%. Send x01 using Manchester encoding from the iPhone at 8820 baud at a frequency of 1Hz. a. DC offset of sent signal is measured on oscilloscope to be within ±0.5mV. b. V_{pp} of sent signal is measured on oscilloscope to be 2.76V_{pp} ±5%. c. Data byte waveform seen on oscilloscope is the correct Manchester encoded byte.
4. User interface should handle user inputs correctly. a. Start scan b. Stop scan c. Save scan d. Email scan e. MMS scan f. Change sound velocity	4. Navigate between user interface views to access various commands. a. Pressing "start scan" switches to view 4. b. Pressing "stop scan" switches to view 3. c. Pressing "save scan" saves the last scan to the iPhone camera roll. d. Pressing "email scan" switches to compose email view with scan image attached. e. Pressing "MMS scan" switches to MMS view with scan image attached. f. Pressing "change sound velocity" allows the user to manually enter a value for sound velocity which changes subsequent scan data.
Contingency Plan: Use an Android phone.	

Overall AEL Measurement Requirements	Verification
1. Upon performing an A-scan with our device, calculated depths should be within 0.1mm of the actual thickness.	1. Two polystyrene test blocks will be used to verify the accuracy of our device. Each will be of known thickness (measured with digital calipers). One will have a thickness equal to a typical anterior chamber depth. The other will have a thickness equal to a typical axial eye length. These correspond to the smallest and largest length measurements to be calculated. The percent difference between expected values and measurements when performed in a sequential experiment should be minimal (<6.7% or within 3σ).
2. AEL Measurements must be performed on tissues similar to structures in the human eye.	2. AEL measurements will be taken on sample animal eyeballs procured from the Meat Sciences Laboratory or the College of Veterinary Medicine. Compare animal AEL lengths with known values for animal and

	human.

b. Tolerance Analysis:

Block name and Basic Description:
The Energizer 9V lithium battery advertises a nominal voltage supply of 9V. This is, however, highly dependent on the amount of current being drawn. In our case, the ultrasound device may draw up to 500mA (conservative estimate), which yields a true voltage supply of about 7V. In addition to this, the battery output voltage will drop slowly over time and usage, until near the end of its life. At this point, the output voltage decreases sharply. We wish to test for the lowest the battery voltage before the regulated voltage levels in the power electronics module outputs fail to maintain their nominal values. As mentioned above, the 9V battery feeds eight voltage converters to regulate nine voltage levels of +30V, +10V, -10V, +5V, -5V, +3.3V, +2.5V, +1.8V, and +1.2V. When one of the measured output levels falls outside of a 5% tolerance of its corresponding nominal value, the lower limit of our supply voltage has been reached.

Testing Focus:
We will replace the 9V battery with a DC power supply capable of supplying voltages from 0-9.5V. This will allow the input voltage to the power electronics to be varied in small steps of 0.1V, starting from 9.5V down to the lower limit (where a regulated voltage fails to remain within 5% of its nominal value).

Table 2. Acceptable Result Ranges Confirming Operation

	+30V	**+10**	**-10V**	**+5V**	**-5V**	**+3.3V**	**+2.5V**	**+1.8V**	**+1.2V**
High Tolerance	+31.5V	+10.5V	-10.5V	+5.25V	-5.25V	+3.465V	+2.625V	+1.89V	+1.26V
Low Tolerance	+28.5V	+9.5V	-9.5V	+4.75V	-4.75V	+3.175V	+2.375V	+1.71V	+1.14V

4. Cost and Schedule

a. Labor:

Name	Hourly Rate	x 2.5	Hours*	Total
Jonathan	$40/hr	$100/hr	240 hrs	$24,000
Adam	$40/hr	$100/hr	240 hrs	$24,000
Dean	$40/hr	$100/hr	240 hrs	$24,000
			Labor total	$72,200

*20 hrs/wk x 12 wks = 240 total hours per person

b. Parts (Received):

Part Name	Qty.	Cost	Total
iPhone 4S (without contract)	1	$700	$700
iPhone Developer License (1-year)	1	$99	$99
DGH 6000 Scanmate A Ultrasound Transducer Probe	1	$700	$700
AFE5801 (Ultrasound Analog Front End Chip)	1	$40	$40
TX810 (High Voltage Transmit/Receive Switch)	1	$8	$8
LM96550 (High Voltage Pulser Chip)	1	$20	$20
LMV331 (Comparator)	1	$0.26	$0.26
QFN Breakout Boards	6	$10	$60
TPS54286 (Dual Buck Converter)	1	$7.20	$7.20
TL497ACN (Inverting Regulator)	1	$1.57	$1.57
		Parts Total:	$1,636.03

c. Parts (Needed):

Part Name	Qty.	Cost	Total
Altera Cyclone III EP3C10E144 FPGA	1	$19.20	$19.20
Altera EPCS16 Serial Programmer	1	$15	$15
Mini Altera FPGA USB Blaster Programmer Cable	1	$10	$10

Abracon ASV-30.000MHZ-EJ-T Clock	1	$2.89	$2.89
CUI SJ-43514-SMT 4-pole 3.5mm Phone Port	1	$1.47	$1.47
PCBs	1	$20	$20
LEDs, R, L, C, etc. (in schematics)	~	$20	$20
TPS61170 (Boost Converter)	1	$4.95	$4.95
TPS76912 (Linear Regulator)	1	$0.99	$0.99
TPS76925 (Linear Regulator)	1	$1.12	$1.12
TPS76933 (Linear Regulator)	1	$1.04	$1.04
LP2985 (Linear Regulator)	1	$0.83	$0.83
TPS7A3001 (Negative Linear Regulator)	1	$4.50	$4.50
		Parts Total:	$101.99

GRAND TOTAL = LABOR + PARTS = $**73,940.91**

d. Schedule:

Week	Jonathan	Adam	Dean
1/30	• Research iPhone Programming • Order BLE chips and breakout board *(BLE removed week of 2/13)*	• Research Ultrasound Probe and A-Scan Procedure • Put BNC connector on Probe	• Draft Proposal • Research Tx/Rx Circuitry for Ultrasound
2/6 (Prop. Due)	• Characterize Probe • Look for corporate sponsorships and submit TI design competition entry	• Download and inspect part datasheets for design feasibility • Select battery to power device	• Order TI Tx/Rx Chips & breakout boards
2/13	• Begin iPhone programming, integrate HiJack Audio libraries • Begin FPGA programming	• Research FPGAs/CPLDs and feasible sampling data rates	• Research SPI chip programming and check all pin-outs of FE chips
2/20 (DR Due)	• Draft Design Review • Implement basic communications on iPhone and Cyclone II • Order Cyclone III FPGA	• Design Review Revision 1 • Design Battery Power Supply Circuit • Order power electronics and passive components not in ECE parts shop	• Design Review Revision 2 • Solder Tx/Rx Chips to breakout boards
2/27	• Make Cyclone III breakout board • Implement LVDS and control code on Cyclone II	• Design PCB for power module • Provide ECE parts shop with PCB design and components • Buy a lithium 9V battery	• Connect front end circuit ICs to ad hoc power supply, wire pin-outs and enable
3/5	• Test and debug Cyclone III board • Connect FPGA to Receiver Circuit and iPhone, debug	• Test and debug power module • Connect power module to entire front-end circuitry, debug	• Test and debug front end circuit ICs • Connect front end ICs to Probe and FPGA, debug
3/12 (IPR Due)	• Individual Progress Report • Debug data from Receiver, begin sending data to iPhone memory	• Individual Progress Report • Finish debugging Transmitter/Probe coupling	• Individual Progress Report • Finish debugging Receiver/Probe coupling
3/19 (Spr. Break)	• Design application user interface	• Write preliminary Matlab code for DSP filtering and AEL calculations • Begin design of device PCB	• Design Test Setup • Begin design of Device Housing
3/26 (Mock-Up Demo)	• Implement application user interface	• Finish designing device PCB • Submit PCB design and components to ECE parts shop	• Prepare device and eyeball for mock-up demonstration • Request help from Machine Shop for device housing
4/2	• Translate Matlab code into Objective-C and integrate it into application software	• Explain filtering and calculations in Matlab code for translation/integration • Test and debug device PCB	• Begin construction of device housing • Request 1st Revision PCB Fabrication from Parts Shop
4/9	• Implement IOL calculator, graphics, etc.	• Test and debug device PCB • Request Final Revision PCB Fabrication from Parts Shop	• Finish construction of device housing
4/16	• Device testing and debugging	• Device testing and debugging	• Device testing and debugging
4/23 (*Demo and Presentation)*	• Final debugging • Prepare slides on iPhone and FPGA	• Final debugging • Prepare slides on Probe and Transmitter Circuit	• Final debugging • Prepare slides on Receiver Circuit and T/R Switch
4/30 (*Final Paper and Checkout)*	• Final Paper Revision 1	• Draft Final Paper	• Final Paper Revision 2

5. Ethical Considerations

Because the end-goal of this device is for medical uses, there are many ethical points we must consider in its design.

The following portions of the IEEE Code of Ethics are especially pertinent to our project:

1. "to accept responsibility in making decisions consistent with the safety, health and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;"

   Though a-scan ultrasound probes are non-invasive when used properly, incorrect operation or a faulty probe could potentially cause damage to the eye. Special care must be taken to ensure our device is not used on humans until approved by the FDA, and only operated by trained physicians after FDA approval. The probe circuitry must also be designed to emit sound waves within amplitude and frequency limits.

2. "to avoid real or perceived conflicts of interest whenever possible, and to disclose them to affected parties when they do exist;"

   Since we are using a donated probe from DGH Technologies, it is important we avoid discussing our project with other medical companies to avoid conflicts of interest.

3. "to be honest and realistic in stating claims or estimates based on available data;"

   Our device's tested performance metrics must be stated clearly and not exaggerated to ensure physicians know what to expect from our device.

9. "to avoid injuring others, their property, reputation, or employment by false or malicious action;"

Our device's intent is not malicious, but rather potentially beneficial for several groups. We will not falsify any information regarding the device that may lead to personal injury.

6. Citations

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[4] Probe document provided by DGH

[5] Serial Configuration (EPCS) Devices Datasheet. Altera Inc., California. [Online] Available: http://www.altera.com/literature/hb/cfg/cyc_c51014.pdf

[6] Hijacking Power and Bandwidth from the Mobile Phone's Audio Jack. Kuo, Verma, et. al. [Online] Available: http://www.eecs.umich.edu/~prabal/pubs/papers/kuo10hijack.pdf

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[12] TPS769xx Data Sheet. Texas Instruments Inc., Texas. [Online] Available: http://www.ti.com/lit/ds/symlink/tps76933.pdf

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[15] Ultrasound of the Eye and Orbit, 2nd ed. Byrne and Green. Page 250.