

DIKI-DIKI Design Document

By

Curtis Lam

Jayden Dang

Mark Sorial

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TA: Lukas Dumasius

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1 Introduction

1.1 Problem

As emissions regulations tighten across major markets, automakers have begun electrifying and hybridizing their vehicles. The electrification pathway delivers meaningful efficiency gains and emissions reductions, whether the platform retains a combustion engine or not. Such vehicles still need a 12 V rail to power legacy safety-critical and comfort electronics, such as power steering assist modules, infotainment, lighting control, and in many platforms ADAS sensors. A 48 V-to-12 V DC-DC converter is therefore needed in vehicles that use both voltage rails; galvanic isolation is a design choice for this project rather than a feature of every such converter [15].

Mild-hybrid systems recover energy that would otherwise be lost during braking and coasting, with a published 48 V study describing fuel-economy benefits of up to 10–15% in passenger vehicles [16]. But the need for a low-voltage rail is not specific to mild-hybrids. Full high-voltage EVs also use a DC-DC converter to supply lower-voltage accessories and recharge an auxiliary battery [17].

Despite this growing importance, published 48 V-to-12 V converter designs still use analog controller ICs, with compensation set by circuit components rather than firmware [19]. An analog-only control circuit would need additional electronics to provide the fault-specific CAN reporting and system-health data planned for this project. As vehicle power electronics move toward higher voltage classes, control and magnetics design approaches that can be adapted across those classes are valuable. The 48 V-to-12 V case is an immediate, tractable learning platform, but the digital control architecture and magnetics-design methodology are intended to inform higher-voltage isolated DC-DC stages, not to be a mild-hybrid-specific solution.

1.2 Solution and Visual Aid

DIKI-DIKI uses a transformer-isolated half-bridge power stage to convert a 20–60 V input to a nominal 12 V output. A secondary-side STM32G474 samples voltage and current, computes a peak-current command, and reports operating state and faults over CAN. Hardware comparators and HRTIM fault inputs stop switching on fast electrical faults independently of the software voltage loop. This architecture lets the team evaluate both the electrical performance of the isolated converter and the diagnostic value of digital control at the proposed laboratory scale.

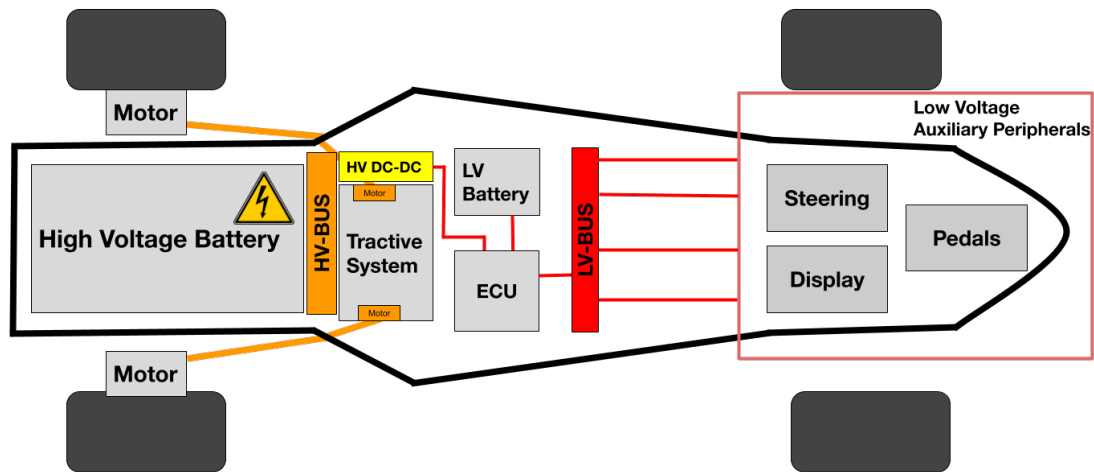


Figure 1. Application of Isolated DC-DC in Automotive EV Power Distribution

1.3 High-level Requirements

- The converter shall regulate a 12V DC output within $\pm 5\%$ across the full input voltage range of 20V to 60V.
- The converter shall deliver at least 125W of continuous output power while maintaining a minimum efficiency of 90%, measured at 48V input.
- The converter shall maintain a galvanic isolation resistance of at least 10 M Ω between the high-voltage and low-voltage domains.
- The converter shall publish its sensed quantities, board temperatures, and controller state over CAN at least 100 times per second, and report the cause of a latched fault within 10 ms of detection.

2 Design

2.1 Block Diagram

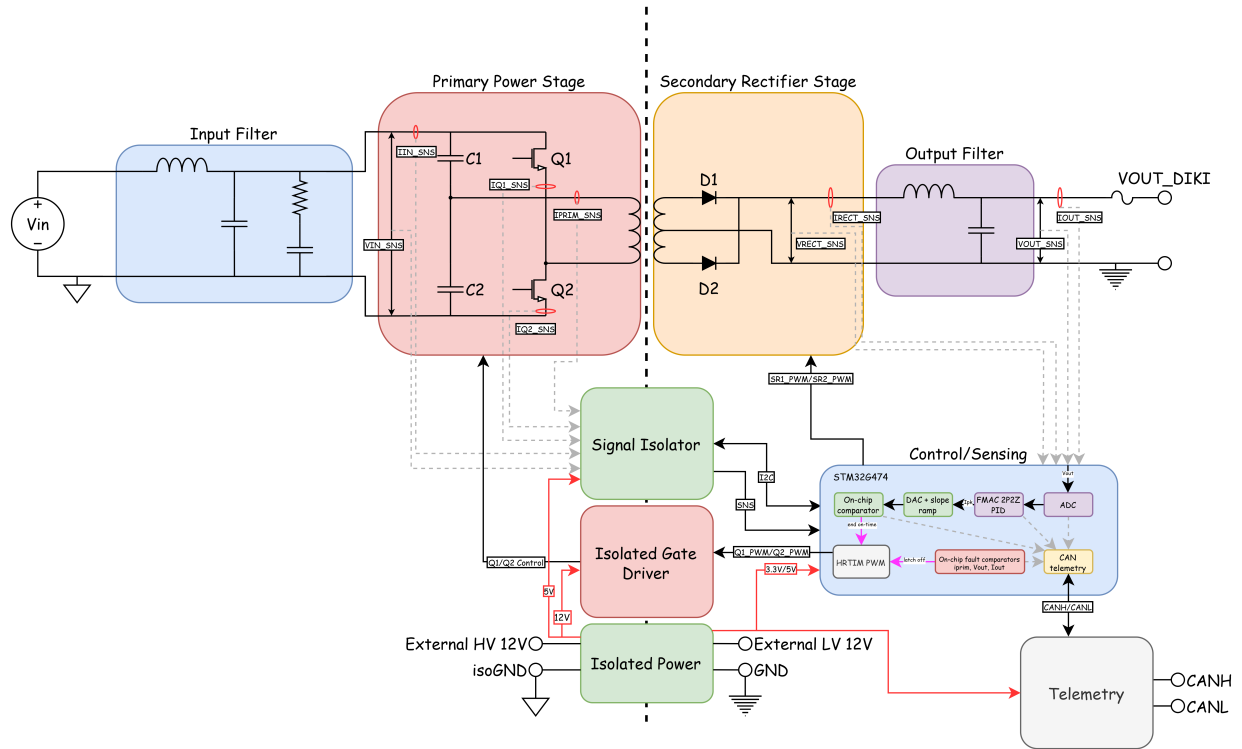


Figure 2. System block diagram of the isolated half-bridge DC-DC converter.

2.2 Physical Design

Our DC-DC converter is a compact design for automotive applications meant. Electric vehicle systems contain two electrical domains: high voltage and low voltage. Our converter is meant to be able to transfer energy stored in the high voltage system to be used on low voltage vehicle controllers and peripherals. Thus, the design consists of two galvanically isolated sections, the HV side, which contains the primary windings, switches, and capacitors, and the LV side which contains the sensing and controls. Our current PCB revision is roughly 180mm x 250mm. There will be a high voltage connector and low voltage connector on either side, with a programming header near the middle. The low voltage connector will contain the auxiliary power, output rails, and telemetry communications.

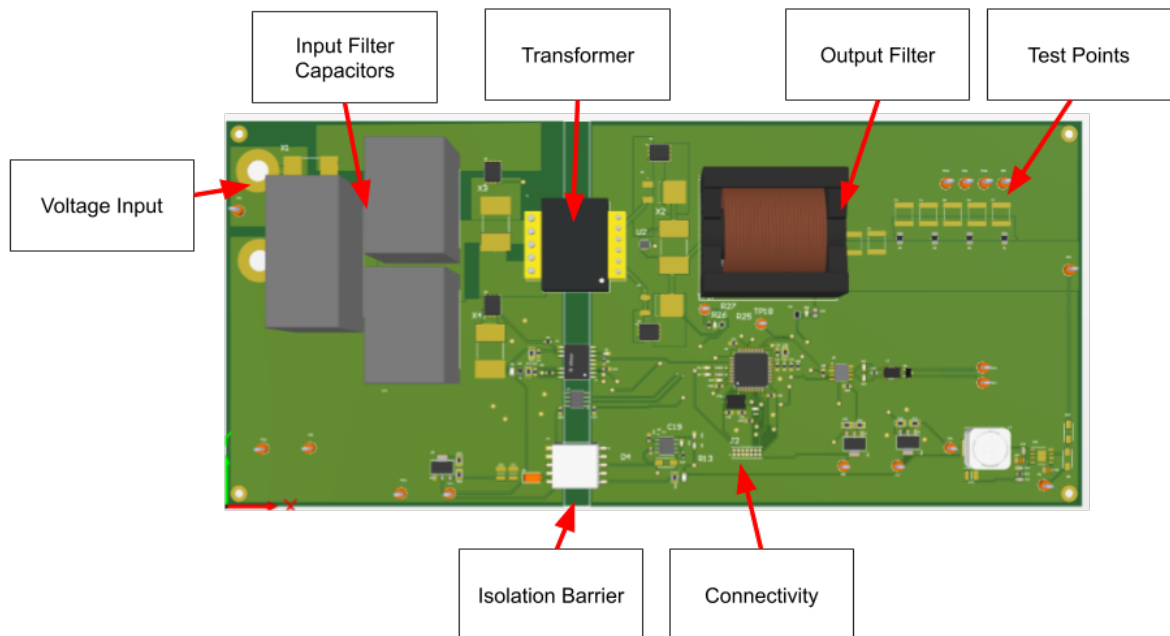


Figure 3. System block diagram of the isolated half-bridge DC-DC converter.

2.3 Input Filter

The input filter provides bidirectional filtering for both the DC power source and the power converter. The filter will prevent noise from the DC power source from getting into the converter, and also the noise from the converter getting back out onto the DC power source. To achieve this, we designed an LC filter with an RC damper targeted to heavily attenuate frequencies above 200kHz. The RC damper attenuates the frequency response at the resonant frequency of the LC filter.

Table 1. Input filter requirements and verification plan.

Requirement	Verification procedure and pass criterion
The input filter shall attenuate switching ripple current back to the DC source by at least 20 dB at 150 kHz.	Connect a wideband current probe to the DC source input lines and measure input AC current ripple under full 125 W load with and without the LC filter engaged; the attenuation at 150 kHz shall exceed 20 dB.
The input capacitor array shall handle the RMS ripple current without exceeding a 20°C temperature rise above ambient.	Run the converter at full load (125 W) for 30 minutes at $V_{in} = 20$ V and record capacitor case temperatures using thermal imaging or thermocouples; temperature rise shall be below 20°C.

2.4 Primary Power Stage

The primary power stage converts the DC input voltage into an AC square wave to transfer power across the transformer. It does this using a half-bridge topology with two switches (Q1, Q2) and a pair of split-bus capacitors (C1, C2) that set the primary's return reference and block DC bias current from reaching the transformer. This section resides entirely in the high voltage domain. Since we are using a digitally controlled topology, this means that the switches in this domain must interface with the microcontroller through a galvanically isolated barrier. To do this, we are controlling our switches with the isolated gate driver, 2ED3144MC12L. The primary side switches must be able to switch fast enough to satisfy the transformers maximum volt second rating.

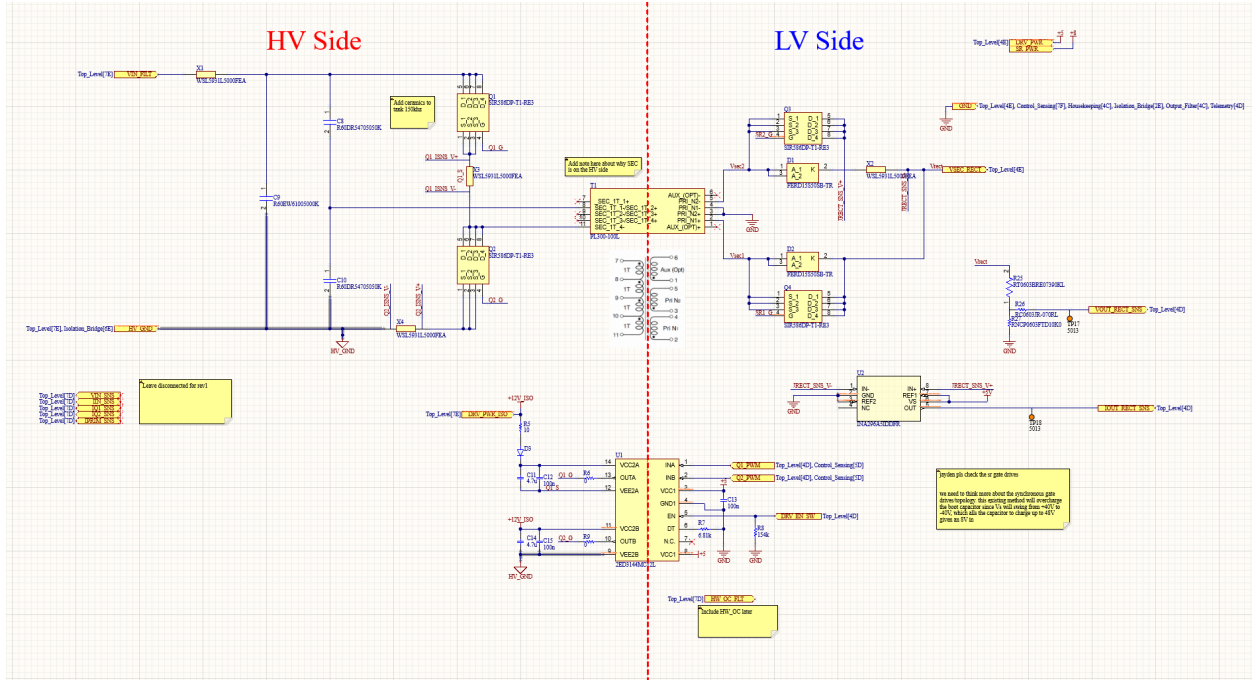


Figure 4. System block diagram of the isolated half-bridge DC-DC converter.

Table 2. Primary power stage requirements and verification plan.

Requirement	Verification procedure and pass criterion
Split-bus capacitors (C_1, C_2) shall keep the primary midpoint voltage stable at $0.5 \times V_{in} \pm 5\%$ under all operating duty cycles to balance volt-second product and prevent transformer flux saturation.	Measure DC voltage across C_1 and C_2 across full duty cycle sweeps ($V_{in} = 20\text{--}60\text{ V}$); midpoint shall stay within $0.5 \times V_{in} \pm 5\%$. Verify transformer primary current waveform on oscilloscope under maximum volt-second stress ($V_{in} = 60\text{ V}, f_{sw} = 150\text{ kHz}$); waveform shall exhibit symmetric magnetizing current without non-linear saturation spikes.
Primary switches (Q_1, Q_2) shall feature total gate charge $Q_g \leq 38\text{ nC}$ (at $V_{GS} = 10\text{ V}$) and achieve voltage transition times (t_r, t_f) under 30 ns at 150 kHz operation.	Capture V_{GS} and V_{DS} switching edges on a 200 MHz oscilloscope at maximum 150 kHz operating frequency; rise and fall transition times (10%–90%) shall be $\leq 30\text{ ns}$, limiting total switching losses to under 10% of total stage dissipation.
Primary MOSFETs (Q_1, Q_2) shall not exceed 85°C under worst-case continuous rated operating load (125 W).	Apply thermal probes to Q_1 and Q_2 cases during a 30-minute full-power burn-in run at $V_{in} = 20\text{ V}$; maximum recorded temperature shall stay under 85°C .

2.5 Secondary Rectifier Stage

The secondary rectifier stage converts the AC waveform coming out of the transformer back into a DC waveform. The two diodes (D1, D2) are selected to have a quick response to the high-frequency waveform of the transformer secondary, and to block the reverse voltage up to 50V, while maintaining a low forward voltage to minimize power loss. To further diminish power loss through the rectifier, additional switches (Q3, Q4) were added to support synchronous rectification, which drops the "forward voltage" of the rectifier practically down to 0V.

Table 3. Secondary rectifier stage requirements and verification plan.

Requirement	Verification procedure and pass criterion
Synchronous switches (Q_3, Q_4) shall maintain gate drive synchronization with the transformer secondary AC waveform without cross-conduction shoot-through.	Observe V_{GS} and V_{DS} waveforms on an oscilloscope during continuous switching; ensure non-overlapping gate signals with a minimum of 50 ns dead time.

2.6 Output Filter

The output filter is used to take the switching waveform of the rectifier, and turn it into a stable DC voltage source. The output filter will store a significant amount of energy, and therefore, needs to be sized relatively large. The output filter will determine the current and voltage ripple of the converter, which are key metrics of determining the converters performance and stability. The inductive and capacitive system that the output filter forms will meet our ripple targets.

Table 4. Output filter requirements and verification plan.

Requirement	Verification procedure and pass criterion
Output voltage ripple shall not exceed 120 mV _{p-p} ($\leq 1\%$ of nominal 12 V output) at full rated load of 10.4 A.	Connect an AC-coupled oscilloscope probe with a 20 MHz bandwidth limit directly across the output terminals at full load; peak-to-peak ripple shall be under 120 mV.

2.7 Signal Isolator

Primary-side measurements, input voltage and current, Q1/Q2 and transformer-primary currents, cross the galvanic barrier through an isolated amplifier stage before reaching the STM32G474's ADC and comparator inputs as scaled 0–3.3 V signals. Temperature sensors follow a separate I²C bus, crossed via an ISO1640BQDRQ1 bidirectional isolator. These isolated paths' propagation delay is included in the Signal Propagation Analysis.

Table 5. Signal isolator requirements and verification plan.

Requirement	Verification procedure and pass criterion
The primary analog sense isolators shall transmit primary-side voltage and current signals across the galvanic barrier with a total propagation delay $t_{pd} \leq 250$ ns and a full-scale signal linearity error below $\pm 1.0\%$.	Inject a step voltage and a 10 kHz sine wave onto the primary sensing node using a function generator. Probe the input signal and the isolated analog output on an oscilloscope; latency between input and output edges shall be ≤ 250 ns, and linear regression of the output vs. input shall yield an error within $\pm 1.0\%$.
The bidirectional digital signal isolator (ISO1640) shall maintain error-free I ² C bus communication at 400 kHz across the isolation barrier without corrupting temperature telemetry data.	Connect an I ² C protocol analyzer to both sides of the isolator during continuous temperature sampling over 100,000 transactions. Verify zero bus arbitration failures, zero NACK errors due to edge distortion, and 100% packet integrity.

2.8 Isolated Gate Driver

The isolated gate driver enables high peak current sourcing and sinking into and from the switches' gates, since the gates have relatively high gate capacitance to achieve a low R_{ds} ($5m\Omega$) and minimize conduction loss. By bootstrapping the power supply into the gate drive for the high-side switch, V_{gs} reaches 12V no matter what the source voltage is relative to HV GND.

Table 6. Isolated gate driver requirements and verification plan.

Requirement	Verification procedure and pass criterion
The gate driver shall deliver a minimum peak output current of ± 2.0 A to drive primary MOSFET gates (Q_1, Q_2), maintaining V_{GS} switching rise (t_r) and fall (t_f) times below 30 ns at 150 kHz.	Connect high-bandwidth voltage probes to V_{GS} of Q_1 and Q_2 while switching at 150 kHz under nominal load. Measure 10%–90% edge transition times on an oscilloscope; rise and fall times shall both measure ≤ 30 ns.
The driver's hardware dead-time logic shall enforce a non-overlapping hardware dead time between high-side and low-side switch signals ($t_{dead} \geq 85$ ns) to eliminate cross-conduction shoot-through currents.	Capture high-side and low-side gate signals simultaneously on an oscilloscope during continuous 150 kHz operation. Verify that the measured delay between high-side turn-off and low-side turn-on (and vice-versa) is at least 85 ns under all duty cycles.

2.9 Isolated Power

The isolated power supply provides regulated 12 V and 5 V bias rails across the galvanic isolation barrier to power the primary-side gate drivers and isolated sensing circuitry. We have chosen an

auxiliary flyback converter topology capable of continuously supplying up to 0.8 A (9.6 W) to the primary-side isolated domain.

The gate driver represents the primary dynamic load on this isolated supply. Its average current draw ($I_{\text{drv,avg}}$) is equivalent to the average charge delivered to continuously switch the primary MOSFETs (Q_1, Q_2) at $f_{\text{sw}} = 150 \text{ kHz}$:

$$I_{\text{drv,avg}} = 2 \times Q_g \times f_{\text{sw}} \quad (1)$$

For two primary MOSFETs with total gate charge $Q_g = 38 \text{ nC}$ per device at $V_{\text{GS}} = 10 \text{ V}$:

$$I_{\text{drv,avg}} = 2 \times (38 \times 10^{-9} \text{ C}) \times (150 \times 10^3 \text{ Hz}) = 11.4 \text{ mA} \quad (2)$$

Table 7. Isolated power supply requirements and verification plan.

Requirement	Verification procedure and pass criterion
The auxiliary flyback converter shall provide a steady-state isolated $12 \text{ V} \pm 5\%$ bias rail supplying up to 0.8 A (9.6 W) to the primary-side driver and sensing circuitry across the full input voltage range (20–60 V).	Connect an adjustable DC power supply (20–60 V) to the flyback input and an electronic load set to 0.8 A on the 12 V output. Sweep the input voltage across the full range; the output rail shall remain strictly within 11.4 V and 12.6 V.

2.10 Control/Sensing

Digital control on the DIKI-DIKI will be implemented with an STM32G474 microcontroller. The STM32 will be on the secondary side referenced to the 12V output voltage. It receives nine analog inputs directly into the on-chip ADCs: input voltage and current; Q1, Q2, and transformer-primary currents; rectified voltage and output-inductor current; and output voltage and current. Measurements from the primary side will pass through the Signal Isolator subsystem to the STM32. Digital temperature sensors on an I²C bus monitor the rectifier, primary switches, and transformer for safety and faults. Analog channels must be scaled appropriately before entering the STM. For current channels, a current-sense amplifier shunt resistor and a voltage divider will be used to ensure a safe 0-3.3V signal can be measured by the STM. The measurement ranges, divider ratios, current-sense gains, and isolation-channel transfer functions will be finalized with the analog schematics.

Output-inductor current, primary current, output voltage, and output current are routed to the MCU's ADC and comparator paths for control and fast protection. Separate Q1 and Q2 current measurements allow detection of developing flux imbalance. The remaining channels support monitoring, power calculations, and diagnostics.

2.10.1 Voltage Loop & Peak-Current Control

The DIKI-DIKI converter will be controlled by a dual-loop control system, with an outer voltage loop running an integer-multiple slower than the internal peak-current controller. The STM32G4's HRTIM (High-Resolution Timer) generates complementary gate signals to drive the half bridge converter. The HRTIM also triggers the ADCs to sample at a fixed point every switching cycle, preventing switching transients from having a significant effect on the measurements. During a switching cycle where the voltage loop will run, firmware calculates the voltage error $e[k] = V_{\text{ref}} - V_{\text{out}}[k]$ from a 12V reference and the measured output voltage. It then uses a two-pole, two-zero compensator to convert the error into a peak-current setpoint for the inner control loop. The STM32G4's internal DAC will then turn that peak-current setpoint into a comparator threshold. When the sensed output-inductor current crosses the peak-current setpoint, the comparator will send a signal to the HRTIM to end the active gate pulse. A DAC ramp can then be used to add slope compensation each cycle, preventing instability at higher duty cycles and killing oscillations within a single cycle. The entirety of the inner peak-current controller runs on hardware peripherals within the STM32G474 allowing a single control cycle to run comfortably within a switching cycle of the converter. [1]

At reset/power-on the controller keeps both gates disabled. It enables switching only after running through a few safety checks such as checking temperatures, rail voltages, ADC calibrations, gate-driver status and finally the CAN command state. During initial start-up, firmware will ramp up the target output voltage, clamp the setpoint to 11-13V and limit the peak-current command. This is to ensure the converter can reach 12V within 20ms without allowing inrush current to exceed 150% of the rated value.

The switching-frequency target is 150 kHz, or $6.67 \mu\text{s}$ per cycle. Ensuring the control cycle can finish within a switching period is one of the largest risks of our project and will be discussed in the Tolerance Analysis section.

2.10.2 Protection and Fault Handling

Separate STM32 comparators will be used for hardware fault protection. The comparators will monitor primary overcurrent, output overvoltage, and output overcurrent. The planned trip thresholds are 150% of the rated primary peak current, 14 V, and 15 A, respectively. These fault signals will disable the gate outputs through the HRTIM without waiting for software to recognize and process the signal.

Firmware handles slower faults such as undervoltage, overtemperature, gate-driver faults, and loss of critical measurements. Both hardware trips and firmware-detected faults latch switching off. Firmware records the fault cause and a snapshot of the latest measurements for CAN reporting. After the fault condition is gone, a valid CAN command can clear the latch.

2.10.3 Requirements and Validation

Table 8. Control/sensing requirements and validation plan.

Requirement	Verification procedure and pass criterion
Voltage readings shall be within $\pm 1\%$ and current readings within $\pm 2\%$ of reference measurements over the intended measurement range.	Apply at least five known points across each channel's range with a calibrated voltage or current source and read raw and calibrated values. Record a table of reference, reported value, and percent error; every point shall meet its limit.
With the steady-state reference fixed at 12.0 V, the output shall remain between 11.4 and 12.6 V as input varies from 20 to 60 V at a 5.2 A load, and as load varies from 5.2 to 10.4 A at 48 V input.	First hold the load at 5.2 A and sweep input from 20 to 60 V. Then hold input at 48 V and sweep the load from 5.2 to 10.4 A. Measure output voltage at the converter terminals and record the minimum and maximum steady-state values; all points shall stay within the band.
The voltage-loop computation shall run once every N switching cycles and update the DAC before the required HRTIM event.	Toggle a debug pin around the voltage-loop ISR, capture the HRTIM trigger and DAC output on an oscilloscope across the specified input and load ranges, and record worst-case execution and ADC-trigger-to-DAC latency over at least 10^5 switching cycles. No scheduled update may miss its deadline.
A 5.2 A to 10.4 A load step shall cause less than 5% output deviation, settle to within $\pm 2\%$ of 12 V in under 1 ms, and show no sustained oscillation.	Use a switched electronic load and oscilloscope at 20, 48, and 60 V input. Save labeled waveforms, calculate deviation and settling time, and check the steady-state trace for sustained oscillation.
Primary overcurrent, output voltage above 14 V, or output current above 15 A shall disable all gate outputs within 2 μ s of the corresponding comparator-input threshold crossing.	With the primary side unpowered and secondary side powered, inject a calibrated ramp at each comparator input. Measure threshold crossing and the last gate-driver output edge with a scope. Record delay and threshold for repeated trials; both gate outputs shall be off within 2 μ s.
Soft start shall bring the output into the 11.4–12.6 V band within 20 ms with measured inrush below 150% of rated input current.	Capture input current, output voltage, and gate enable at 20, 48, and 60 V under the specified load.

2.11 Telemetry

The STM32G474 FDCAN peripheral and a 3.3 V CAN transceiver sit on the secondary side of the isolation barrier. The current configuration uses classic CAN at a nominal 500 kbit/s but supports CAN-FD at rates up to 8 mbit/s. The transceiver connects to an externally terminated CAN bus in accordance with the selected physical-layer implementation [?]. No CAN conductor crosses the primary-to-secondary barrier. The firmware publishes status, announces latched faults, and accepts enable, disable, and fault-clear commands.

The planned DBC will define a group of up to six periodic status frames with fixed scaling, units, signedness, identifiers, and update counters. Together these frames will carry the nine analog measurements, at least three board temperatures, peak-current command, computed input and output powers, efficiency, and controller state. Each member of the group is transmitted at least every 10 ms. A provisional budget of six 160-bit worst-case wire-time frames per 10 ms is 96 kbit/s, about 19% of a 500 kbit/s bus.

2.11.1 Requirements and Verification

Table 9. Telemetry requirements and verification plan.

Requirement	Verification procedure and pass criterion
Every defined status signal shall be updated at least every 10 ms and decoded with the supplied DBC.	Connect a CAN dongle (PCAN) and log at least 60 s of steady operation at each of three load points. Decode using the project DBC, compare selected values to bench instruments, and report the maximum time for every status frame. No required signal may be stale beyond 10 ms.
A latched fault shall produce a cause and measurement snapshot within 10 ms.	Trigger each fault input while logging the fault pin and CAN bus with an oscilloscope and CAN analyzer. The complete record shall arrive within 10 ms under the stated test load.
Valid enable, disable, and fault-clear commands shall be acted on within 10 ms; unknown or malformed commands shall not change the controller state.	Send commands from a CAN interface with timestamps while probing gate enable and recording the controller state. Log each response time and unchanged-state rejection.
After induced bus-off, communication shall recover within 1 s while power conversion remains latched off until explicit clear and enable commands.	Use a controlled CAN bus disconnection (no ACK frames). Record bus-off detection, gate-off, first valid frame after restoration, and converter state.

2.12 Tolerance Analysis

2.12.1 Project Risk

Given our hard-switched half-bridge topology, switching loss and component non-idealities pose the primary risk to hitting our efficiency target. Digital control at our target frequency range also compresses our available timing margin. The full signal path from sensing through the microcontroller to gate-drive output must complete well within a single switching period, leaving limited room for propagation delay before it begins to affect regulation accuracy and, at the extreme, loop stability.

2.12.2 Signal Propagation Analysis

Table 10. Voltage feedback path delay (Vout sense → PWM update)

Stage	Delay
ADC sample + convert (12-bit, 40 MHz)	0.35 μs
Interrupt entry latency (~ 10 – 20 cycles)	0.2 μs
ADC read + compensator execution	0.2–0.3 μs
DAC register write	0.1 μs
DAC output settling	0.5–1 μs
Total (with margin)	$\sim 2.5 \mu\text{s}$

Table 11. Current sensing path delays

Signal	Delay
Primary current: CT	50 ns
Primary current: analog summer	~ 200 ns
Primary current total	~ 250 ns
Output inductor current: current-sense amp	~ 100 ns

At 100 kHz, $T_{sw} = 10 \mu\text{s}$. The voltage feedback path's $\sim 2.5 \mu\text{s}$ delay consumes roughly 25% of the switching period, making it the dominant contributor to overall loop delay. The current-sensing paths (~ 250 ns for primary current, ~ 100 ns for output inductor current) are an order of magnitude smaller by comparison, confirming that digital signal-path delay—not analog sensing—is the limiting factor and primary consumer of available timing margin in this design. This analysis emphasizes the importance of peak current detection through the analog comparator, as that variable will drive the T_{on} of the half bridge switches. It is worth noting that this propagation timing analysis assumes a full-scale (0 to maximum) DAC step, whereas in practice the control loop will not command such large step changes, meaning the actual available timing margin is greater than this calculated worst case.

2.12.3 Gate Drive Analysis

With an input voltage target of 20 V–60 V and an output voltage target of 12 V–24 V, the primary gate-drive circuitry, transformer turns ratio, and switching MOSFETs must be sized to maintain adequate duty-cycle margin. To ensure reliable soft-switching transients and account for driver dead time, the design targets a maximum effective conversion duty cycle $D_{\max} \leq 0.85$ and a minimum duty cycle $D_{\min} \geq 0.10$.

The design specifies an effective transformer turns ratio $N_s/N_p = 1.50$ (e.g., 2 primary turns to 3 turns

per active secondary winding) and an Infineon 2ED3144MC12L dual-channel isolated driver with dead-time resistor $R_{DT} = 10 \text{ k}\Omega$ (providing 85–115 ns dead time). At $f_{sw} = 150 \text{ kHz}$, the required duty cycle spans 14.28%–82.83% across all input/output voltage extremes. MOSFET selection targets a V_{DS} breakdown rating matched to input transient margins and a total gate charge $Q_g \leq 38 \text{ nC}$ at $V_{GS} = 10 \text{ V}$.

The relationship governing the power stage forward conversion, including the secondary rectifier drop $V_D = 0.85 \text{ V}$, defines the required duty cycle D_{req} :

$$D_{req} = \frac{V_{out} + V_D}{V_{in} \left(\frac{N_s}{N_p} \right)} = \frac{V_{out} + 0.85}{V_{in} \left(\frac{N_s}{N_p} \right)}. \quad (3)$$

To enforce the design boundaries $0.10 \leq D_{req} \leq 0.85$ across all operational extremes ($V_{in} \in [20, 60] \text{ V}$ and $V_{out} \in [12, 24] \text{ V}$), the nominal active turns ratio N_s/N_p must satisfy:

$$\left(\frac{N_s}{N_p} \right) \geq \frac{V_{out,max} + V_D}{V_{in,min} D_{max}} = \frac{24 + 0.85}{20(0.85)} = 1.462, \quad (4)$$

$$\left(\frac{N_s}{N_p} \right) \leq \frac{V_{out,min} + V_D}{V_{in,max} D_{min}} = \frac{12 + 0.85}{60(0.10)} = 2.142. \quad (5)$$

Selecting $N_s/N_p = 1.50$ places the operating window comfortably within bounds. Table 12 details the resulting calculated duty cycles and switch conduction times ($T_{on} = D_{req} T_{sw}$) across the operating corners at $T_{sw} = 6.667 \text{ }\mu\text{s}$.

Table 12. Calculated power-stage duty cycles ($N_s/N_p = 1.50$, $V_D = 0.85 \text{ V}$).

V_{in}	V_{out}	$V_{out} + V_D$	D_{req}	$T_{on} = D_{req} T_{sw}$
20 V	12 V	12.85 V	42.83%	2.856 μs
20 V	24 V	24.85 V	82.83%	5.522 μs
60 V	12 V	12.85 V	14.28%	0.952 μs
60 V	24 V	24.85 V	27.61%	1.841 μs

2.12.4 Initial Simulation

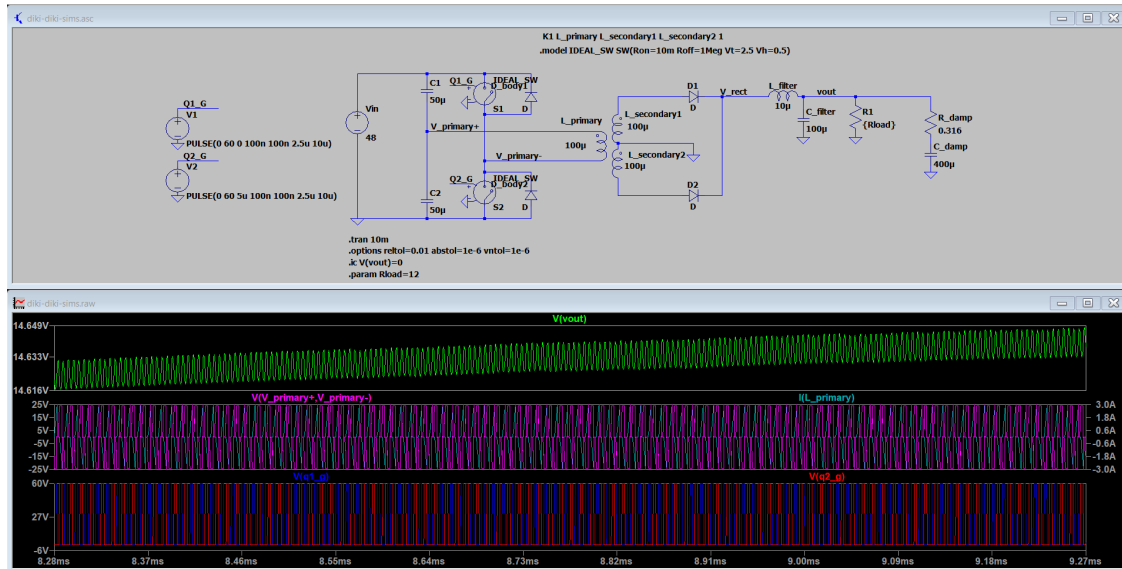


Figure 5. Initial LTspice simulations with open-loop control.

3 Cost and Schedule

3.1 Cost

The following labor calculation is a planning estimate for the three-person team. The course design-review guidance recommends approximately \$50/hour and a 2.5 overhead multiplier [10]. We estimate 120 hours per person, or about 12 hours per week over 10 weeks, for design, assembly, integration, testing, and documentation.

$$C_{\text{labor}} = \sum_{i=1}^3 (\$50/\text{h})(2.5)(120 \text{ h}) = \$45,000. \quad (6)$$

Table 13 is a procurement checklist for the custom prototype. This includes the full BOM cost of the PCB sourced from the exact part selection used in the design. We do not predict needing any lab resources not already possessed by the ECE445 Senior Design Lab.

Table 13. Preliminary bill of materials with itemized description, unit cost, and extended cost.

Item Part No.	Description	Designator(s)	Qty	Unit Cost	Total Cost
Part number (LibRef)	Description	Designator	Qty.	Unit (USD)	Extended (USD)
GMC55X7R226M100NTD	CAP2220 X7R 22UF 20% 100V	C1, C2, C3, C4, C5, C6, C7	7	\$2.95	\$20.65
R60DR54705050K	Film capacitor 47 uF 10% 63VDC	C8, C10	2	\$12.25	\$24.50
R60EW61005000K	Film capacitor 100 uF 10% 100VDC	C9	1	\$24.50	\$24.50
CC0603KRX7R8BB104	0.1 uF +/-10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	C12, C13, C15, C23, C24, C25, C26, C27, C28, C32, C34, C38, C39	13	\$0.14	\$1.82
CC0603MRX5R8BB106	CAP CER 10UF 25V X5R 0603	C19	1	\$1.35	\$1.35
GMC31X5R476M25NT	CAP1206 X5R 47UF 20% 25V	C20, C21	2	\$1.51	\$3.02
CC0603KRX7R8BB105	1 uF +/-10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	C22	1	\$0.35	\$0.35
CC0603KRX7R8BB103	10000 pF +/-10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	C30	1	\$0.10	\$0.10
CC0603KRX7R8BB105	1 uF +/-10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	C31, C33	2	\$0.35	\$0.70
CC0603JRNPO9BN160	0603 16 pF 50 V +/-5 % Tolerance NP0 SMT Multilayer Ceramic Capacitor	C35, C36	2	\$0.13	\$0.26
CC0603KRX7R8BB473	Ceramic capacitor 47 nF 25V X7R 0603	C37	1	\$0.13	\$0.13
CMP-050-000000-3	CAP CER 0.1UF 50V X7R 0603	C40	1	\$0.10	\$0.10
CMP-050-000008-2	0805 1.8 nF 50 V +/-5 % Tolerance NP0 SMT Multilayer Ceramic Capacitor	C41	1	\$0.24	\$0.24
CMP-050-000003-2	CAP CER 4.7uF 50V X7R 0805	C42	1	\$0.59	\$0.59
EMK325ABJ107MM-T	TAIYO YUDEN - EMK325ABJ107MM-T - CAP, MLCC, X5R, 100UF, 16V, 1210	C43	1	\$2.14	\$2.14
CMP-050-000002-4	CAP CER 2.2uF 100V X7R 0805	C44	1	\$0.64	\$0.64
MM3Z3V3B	Zener diode 3.3V 200mW SOD-323F	CR1	1	\$0.24	\$0.24
FERD15S50SB-TR	Diode	D1, D2	2	\$1.37	\$2.74
BAT201M3RRG	Diode Schottky 20V 1A 2-Pin SOD-323F T/R	D3	1	\$0.28	\$0.28
Schottky-Diode	DIODE SCHOTTKY 40V 3A DO214AC	D5	1	\$0.35	\$0.35
CMP-041-000000-3	LED GREEN CLEAR 0603 SMD	D6	1	\$0.15	\$0.15
CMP-051-000000-2	LED RED CLEAR 0603 SMD	D7	1	\$0.15	\$0.15
CMP-051-000562-2	CAN TVS diode; priced as Nexperia PESD1CAN,215	D8	1	\$0.54	\$0.54
SK54A-LTP	Schottky rectifier 40V 5A SMA	D9, D10	2	\$0.33	\$0.66
FTSH-107-01-S-D-K	Header 14 positions 1.27mm dual row	J2	1	\$3.16	\$3.16
7443763540470	Inductor 47 uH 32A through hole	L1	1	\$21.43	\$21.43
CMP-053-000017-1	CMC 300NH 2A 2LN 90OHM SMD	L2	1	\$1.80	\$1.80
SIR872ADP-T1-GE3	N-channel MOSFET 150V 53.7A PowerPAK SO-8	Q1, Q2, Q3, Q4	4	\$2.71	\$10.84
RNCP1206FTD4R70	Resistor 4.7 Ohm 1% 0.5W 1206	R1, R2, R3, R4	4	\$0.10	\$0.40
RNCP0805FTD10R0	10 Ohms +/-1% 0.25W, 1/4W Chip Resistor 0805 (2012 Metric) Anti-Sulfur, Moisture Resistant Thin Film	R5	1	\$0.10	\$0.10
RC0603JR-070RL	0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	R6, R9, R26	3	\$0.10	\$0.30
CMP-055-000041-1	RES SMD 154K OHM 1% 1/10W 0603	R8, R23	2	\$0.10	\$0.20
RK73B2ATTD390J	RES 39 OHM 5% 1/4W 0805	R10	1	\$0.10	\$0.10
RMCF0603FT750K	RES 750K OHM 1% 1/10W 0603	R11	1	\$0.10	\$0.10

Table 13. Preliminary bill of materials with itemized description, unit cost, and extended cost.

Item Part No.	Description	Designator(s)	Qty	Unit Cost	Total Cost
AC0603FR-07232KL	RES SMD 232K OHM 1% 1/10W 0603	R12	1	\$0.10	\$0.10
RC0603FR-07187KL	RES 187K OHM 1% 1/10W 0603	R13	1	\$0.10	\$0.10
RNCP0603FTD10K0	Resistor 10 kOhm 1% 0.125W 0603	R14	1	\$0.10	\$0.10
RNCP0603FTD10K0	Resistor 10 kOhm 1% 0.125W 0603	R15, R18, R27	3	\$0.10	\$0.30
RNCP0603FTD499R	Res Thin Film 0603 499 Ohm 1% 0.125W(1/8W) +/- 100ppm/C Sulfur Resistant Pad SMD T/R	R16, R17	2	\$0.10	\$0.20
RNCP0805FTD9K09	Resistor 9.09 kOhm 1% 0.25W 0805	R19	1	\$0.10	\$0.10
RNCP0603FTD10K0	Res Thin Film 0603 1K Ohm 1% 0.125W(1/8W) +/- 100ppm/ deg C Sulfur Resistant Pad SMD T/R	R20	1	\$0.10	\$0.10
CMP-055-000040-2	RES SMD 22.1K OHM 1% 1/10W 0603	R24	1	\$0.10	\$0.10
CMP-03412-014743-1	RES SMD 390K OHM 0.1% 1/10W 0603	R25	1	\$0.10	\$0.10
PL300-100L	Planar power transformer 300W	T1	1	7.31	7.31
750311624	WE-FB Flyback Transformer suitable for LT3575 & LT3748, SMT, EP13, 10-40Vin, Uo1 = 15V/1A, 15W	T2	1	\$6.36	\$6.36
CMP-1672-00005-4	Test Point, Orange, Through Hole, RoHS, Bulk	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	18	\$0.35	\$6.30
2ED3144MC12L	Dual-channel isolated gate driver	U1	1	\$2.49	\$2.49
INA296A5IDDFR	-5-V to 110-V, bidirectional, 1.1-MHz 8-V/us ultraprecise current sense amplifier 8-SOT-23-THIN -40 to 125	U2	1	\$3.76	\$3.76
CMP-0062-01635-4	800mA Low-Dropout Linear Regulator, 4-pin SOT-223, Pb-Free	U5, U12	2	\$1.21	\$2.42
LT8302HS8EWTRPBF	No-opto isolated flyback converter	U6	1	\$12.68	\$12.68
ISO1640BQDRQ1	Automotive, hot-swappable, robust-EMC bidirectional I2C isolator with bidirectional clock 8-SOIC -40 to 125	U7	1	\$4.76	\$4.76
STM32G474RET6	ARM Cortex-M4F STM32G4 Microcontroller IC 32-Bit Single-Core 170MHz 512KB (512K x 8) FLASH 64-LQFP (10x10)	U8	1	\$10.00	\$10.00
CMP-053-000272-2	Automotive grade-0 enhanced CAN FD transceiver with standby 8-SOIC -40 to 150	U9	1	\$1.60	\$1.60
CMP-125-000000-4	IC REG BUCK ADJ 3A 8SOPWR	U10	1	\$3.77	\$3.77
CMP-0062-01639-4	800mA Low-Dropout Linear Regulator, 4-pin SOT-223, Pb-Free	U11	1	\$1.21	\$1.21
WSL5931L5000FEA	0.5 mOhms +/-1% 5W Chip Resistor Nonstandard Anti-Sulfur, Automotive AEC-Q200, Current Sense, Moisture Resistant, Pulse Withstanding Metal Element	X1, X2, X3, X4	4	\$1.73	\$6.92
ABM3-8.000MHZ-D2Y-T	Crystal 8MHz 18pF SMD	XTAL1	1	\$0.68	\$0.68
				Total	\$196.09

The grand total is $C_{\text{grand}} = C_{\text{labor}} + C_{\text{PCB}} + C_{\text{Parts}} = \$45,000 + \$50.00 + \$196.09 = \$45,246.09$.

3.2 Schedule

Date Range	Task	Person
GATE 1: Project Proposal & Architecture		
9/7 – 9/8	High-Level Block Diagram: Visualize core system architecture	Everyone
	System Requirements Definition: System constraints & targets	Everyone
9/8 – 9/16	High-Level Architecture Refinement: Sub-system expansion	Curtis & Jayden
	Hardware Requirements: Component Sizing & Simulations	Curtis & Jayden
	Software Requirements: features, sensor counts, and MCU selection	Mark
	Control Research: MATLAB Modeling & control strategies	Jayden & Mark
GATE 2: First PCB Order		
9/16 – 9/24	Schematics and Component selection	Curtis & Jayden
	Sensing and Timing requirements	Mark
	Order Prototype / Development Components	Mark
9/24 – 9/29	Complete PCB Layout & Pass DRC	Jayden & Curtis
	Internal Layout Review	Everyone
	9/29 Submit First PCB Order	Everyone
GATE 3: PCB Revision 2		
9/30 – 10/4	Breadboard Validation: Verify control algorithm on dev board	Mark
	Begin revision 2 schematics	Curtis & Jayden
10/5 – 10/14	Prepare Breadboard Demo	Everyone
	Finalize Revision 2	Curtis & Jayden
	Internal Layout Review & DRC	Everyone
	10/15 Submit Revision 2	Everyone
GATE 3: Progress Demo		
10/15 – 10/26	Revision 1 Hardware Bring-Up	Everyone
	Test Plan & Hardware Performance Characterization	Curtis & Jayden
	Verify Connectivity & Timing Spec	Mark
	Verify Controls with Asynchronous Rectification	Mark
10/26 – 11/2	Bring Up software viewer for progress demo	Mark
	Prepare Hardware for Progress Demo	Curtis & Jayden
	Revision 2 Hardware Bring-Up	Curtis & Jayden
	11/2 Progress Demo	Everyone
GATE 3: Mock Demo		
11/3 – 11/9	Verify Hardware Spec on Revision 2	Curtis & Jayden
	Validate Hardware Protections	Everyone
	Voltage Mode Control	Everyone
	3D Print Enclosure	Curtis & Everyone
11/9 – 11/16	Current Mode Control & Load Regulation	Everyone
	Synchronous Rectification	Everyone
	Finalize Data Viewer	Mark
	Mock Demo Prep and Presentation	Everyone
11/16 – 11/20	Mock Demo and Presentation	Everyone
GATE 3: Final Demo		
11/23 – 11/29	Asynchronous Work / Final Bugs	Everyone
11/30 – 12/4	FINAL DEMO	Everyone

Table 14. Project Schedule Grouped by Project Gates

4 Ethics, Safety, Societal Impact, and Standards

The 48V to 12V converter is one of the components that makes mild-hybrid vehicles cheaper than full hybrids, which is the reason the architecture is spreading fastest in markets where a full EV is too costly. A converter that reports its own health over CAN also supports repair rather than replacement, since a fault code pointing to a specific stage lets a technician fix pinpoint issues rather than swap symptomatic modules. Digital control also opens the door for detailed fault response algorithms that improves safety and reliability. The trade is that a digital control brings new difficulties in compute and control requirements, as well as the potential for code bugs. We treat that as a design obligation to keep the hard protection paths in hardware, independent of software, so a firmware bug cannot cause a hazardous output.

The IEEE Code of Ethics asks engineers to hold safety standards and to be honest in stating claims based on available data [9]. Two places in this project call for care. First, we are validating at 48V and arguing the approach scales to higher voltage classes. We will report only what we measure and state clearly which conclusions are demonstrated and which are extrapolated. Second, efficiency figures are easy to inflate through selective test conditions. We will report efficiency across the full load range and input range, including the worst case, not only the peak. The 48V input sits below the 60V DC threshold that IEC 61140 treats as hazardous live [7], which is the reason 48V was chosen as the lab scale for this project. A 48V bus with several amps available can sustain a DC arc, damage a probe tip or heat a ring or tool shorted across it. The input and output capacitors hold enough charge to spark when shorted after power is removed. The rectifier diodes will dissipate several watts at full load and can run hot enough to burn on contact. Our mitigations are a bench supply with current limit for all early testing, a discharge procedure, a simple enclosure or standoff keeping exposed copper away from hands, insulated probes, and the hardware over-current, over-voltage and over-temperature trips. The converter latches off on any fault and does not restart without an explicit command, so a fault cannot cycle unattended. Isolation between the HV and LV domains is verified with an insulation resistance test. ANSI/AAMI ES1-1993, the safe current limits standard used by the ECE 445 course, caps the risk current that may flow from an exposed conductive surface to ground at 100 μA under normal conditions and 500 μA under a single fault [?]. With a 48 V bus and the 10 M Ω isolation resistance required in Section 1.3, the leakage across the barrier is below 5 μA , so a person touching the LV side while the HV side is energized is well inside these limits.

The design targets the operating voltage range of ISO 21780, which defines the 48V electrical system for road vehicles [3], and the electrical load and transient conditions of ISO 16750-2 [4]. The CAN interface follows ISO 11898-1 for the data link layer and ISO 11898-2 for the physical layer [5, 6]. Isolation and protection against electric shock follow the principles of IEC 61140 [7], and the ISO 6469-3 requirements for electrical safety in electrically propelled road vehicles inform the isolation resistance requirement in Section 1.3 [8].

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