

NFC Selector and Flip Display

AgentDock

ECE 445 Design Document

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Team 17

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Section numbers follow the course design-document format. Appendix schematics reproduce the current KiCad source; the accompanying vector PDFs retain full zoom resolution. Cost and physical dimensions labeled as estimates remain planning inputs.

1 Introduction

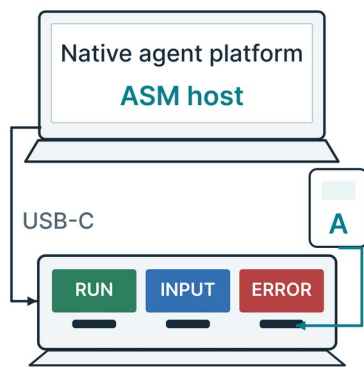
Concurrent AI-agent work spreads status across native conversation windows. A user can miss an agent waiting for input or lose track of the project associated with a visible session. Moving to another computer also separates the user from local context and code state. Research on interrupted work reports a cost in stress and effort, which motivates a lower-interaction way to notice project state; it does not establish that this prototype improves productivity. [1]

AgentDock provides three fixed NFC card slots, each paired with a five-state mechanical display. Inserting a project card identifies a project; the ASM host maps explicitly followed agent sessions to a physical state. A printed project label and persistent color make the three projects visible from across a room. An optional authorized context archive supports a card-mediated transfer between two computers. The native agent platform continues to run the work. The proposed improvement is a stable physical project-to-display association and a readable ambient cue, assessed through binding reliability, response time and visual recognition. [2]

1.1 Visual aid

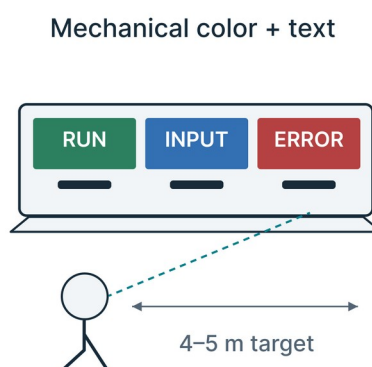
Using AgentDock

1 Bind a project



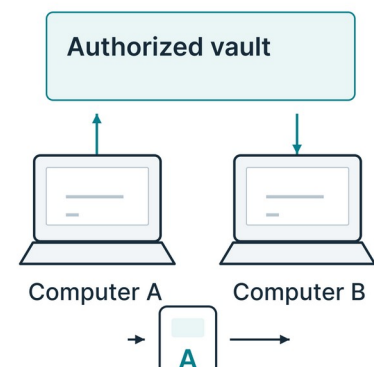
Insert a project card into one of three fixed NFC slots.

2 Glance at status



Read three project states without opening a window.

3 Continue elsewhere



Move the card and dock. Authenticate on computer B.

The card carries a project locator. Context access remains authorized on each computer.

Figure 1. Intended use: insert a project card, observe three states, and move the card with the dock to another authorized computer. Team-authored illustration.

This document expands the proposal into an assembly specification and verification plan using the course format. [3] The external context vault is optional; a local manual project binding can operate without it.

1.2 High level requirements

- H1 — The device shall maintain three concurrent card-project-display bindings. Over 100 complete insertion/removal cycles per slot, it shall correctly detect at least 98% of events and make zero wrong-slot assignments.
- H2 — For each slot, at least 95% of 100 commanded transitions shall reach the correct, stable display state within 15.0 seconds of host control receipt, including tests in which all three slots change simultaneously.
- H3 — At least three consenting testers shall each correctly identify at least 95% of 60 randomized slot-state presentations at 5 m under 300–500 lux, with viewing azimuths of 0° and ±30°; the test shall be repeated at 4 m. Project-name readability at these distances is not required.

These requirements preserve the proposal acceptance conditions. The test allocation below makes them reproducible without weakening the targets. Results will be reported by slot and by tester, rather than pooled to conceal an individual failure. [2] [4]

Table 1. System acceptance sampling

Test	Allocation and measurement	Pass rule
H1	100 cycles = 200 insertion/removal events per slot, 600 events total. Rotate at least three tagged project cards across all slots; record physical action and resulting binding.	Each slot ≥196/200 correct events; no wrong-slot binding across the run.
H2	All 20 ordered unequal state pairs × 5 repetitions = 100 per slot. Schedule the three slot commands together in each trial. Synchronized logs plus ≥60 fps video measure stable display completion.	Each slot ≥95/100 at ≤15.0 s; incorrect states fail regardless of speed.
H3	At each distance: 20 trials at each of three azimuths; balance the five states and slot positions. Measure light at the display and randomize presentation order.	Each tester ≥57/60 at each distance. Record actual lux, angle, distance and every response.

State vocabulary

State	Physical color	Interpretation
Running	Green	Followed work is active
Warning	Yellow	Attention or uncertain source state; inspect host
Error	Red	Unresolved error episode
Waiting for input	Blue	Explicit user input is requested
Blank or idle	White	No active work or unbound slot

A validity indicator is separate from the five state colors. A retained mechanical page after power loss is stale; it must not be interpreted as a new confirmed state.

2 Design

2.1 System overview

System architecture and boundaries

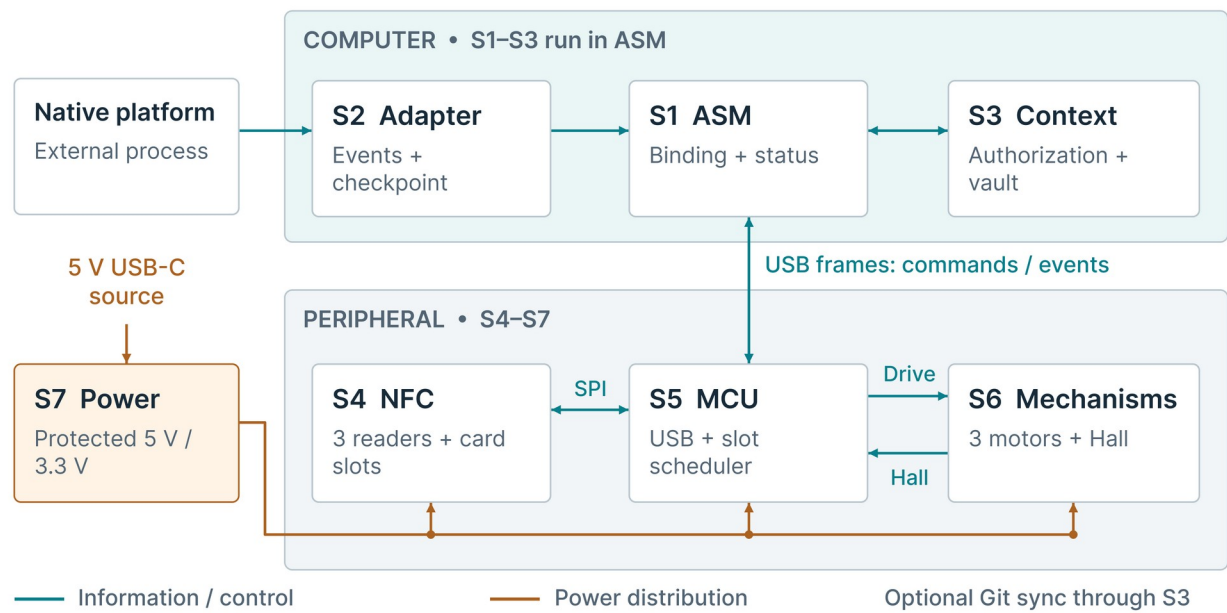


Figure 2. Modular S1-S7 architecture. Teal paths convey information; brown paths distribute power. S3 is an optional host-side context service.

S1 selects project status; S2 normalizes platform reports and prepares checkpoints; S3 protects and stores context. These functions now reside in one ASM host architecture. S4 identifies fixed-slot cards, S5 handles USB and three concurrent motion schedules, S6 produces the visible mechanical states, and S7 powers and protects the peripheral. All card and motor operations must remain associated with a slot generation so a delayed event cannot affect a replacement card. [5] [6]

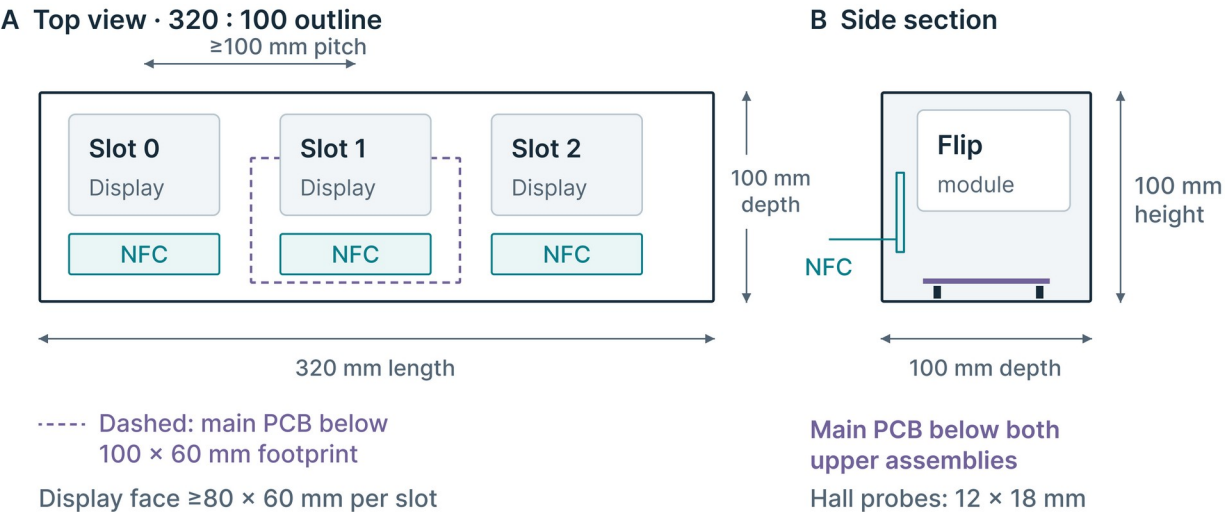
Table 2. Version and evidence boundary

Baseline	Included evidence	Remaining boundary
Hardware v0.1.0	60 × 100 mm four-layer mainboard; three 12 × 18 mm two-layer Hall probes. Current source and BOM snapshot archived.	Physical validation and fabrication readiness are false. Two active silkscreen DRC items remain; electrical checks do not prove operation.
ASM host foundation	Git cd3f558; manual bindings, authorization, persistence and production codec with virtual peer.	Serial hardware, native observer/wake and physical NFC workflows are not implemented.
Mechanical concept	Proposal display area and slot pitch; current PCB outlines and separate modules.	No complete current enclosure CAD or measured mechanism load exists. Drawn envelope is provisional.

Hardware source Git 415e3b7 and host Git cd3f558 were read without modifying either checkout. The source manifest records full commit IDs, file hashes and existing local procurement-note changes.

2.2 Physical design

Physical layout and vertical stack



2.3 S1 ASM project and status management

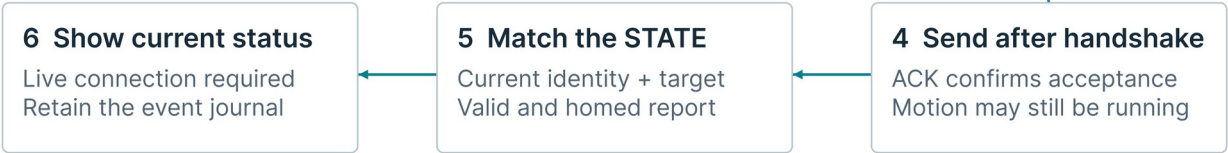
S1 contributes to H1 by maintaining explicit project-to-slot ownership, and to H2/H3 by converting current reports into a stable five-state target. A project UUID is the identity; a workspace path is optional metadata. The current host supports three ordered slots 0, 1 and 2 with manual binding. NFC-driven binding is a planned input to the same ownership transaction. [6]

From an agent event to a confirmed display state

TARGET SELECTION



DEVICE CONFIRMATION



Rebinding, disconnecting or receiving stale identity clears the current confirmation.

Figure 4. Desired state, command acceptance and observed mechanism state have separate meanings. Old epochs, generations and revisions cannot confirm a current target.

Table 4. S1 inputs and outputs

Interface	Quantitative contract
Project inputs	Explicitly enrolled main conversations; producer credential scoped to source, source epoch and session. Newly accepted events require increasing source sequence.
Status reduction	Priority: error > waiting_input > warning > running > idle. Unknown source information maps to warning/yellow only when a valid homed device can display it.
Slot output	Three slots; uint32 binding generation and target revision; 32-hex-digit command identity on the device link. A rebind clears prior ACK and observation.
Freshness	Device heartbeat interval ≤1000 ms; three missed intervals invalidate the device. Producer report lease is separately 60 s; host maintenance runs every 500 ms.

Transactional SQLite storage commits input receipt, projection, attention episode, desired target and outbox together. An attention acknowledgment names the current episode; it cannot erase a newly arrived error. A transport write or ACK never establishes a completed mechanical transition. The host UI must show pending confirmation after a bind or reconnect.

S1 verification and failure handling

Table 5. Requirements and verification

Requirement and pass threshold	Equipment and verification procedure	Record
S1-R1 Zero wrong-slot confirmations across 1,200 interleaved events; three independent bindings.	Use the host Test Lab and virtual peer. Bind three projects, interleave reports and slot rebinding, then compare each accepted observation with current project, generation, revision and command. Repeat with delayed prior-generation ACK and STATE frames.	Event journal, seed and expected/observed slot CSV.
S1-R2 All five priorities and fresh attention episodes are preserved.	Use API fixture producers. Exercise all ten distinct two-state combinations and five single states, then acknowledge an old episode immediately before a new error. Verify the priority result and that the new episode stays active.	15-case matrix and episode IDs.
S1-R3 No valid observed color after disconnect or three missed 1 s heartbeats.	With virtual link then serial hardware, stop heartbeats in ten trials. Record monotonic receipt and invalidation times; require stale by 3.5 s. Replay old heartbeats and duplicate frames; neither may renew freshness.	Timing log and stale-state snapshots.
S1-R4 A 60 s producer lease cannot be refreshed by device heartbeats.	Create a running source, cease reports, keep device heartbeat alive. In ten trials require the source to become stale by 60.5 s and the host to stop presenting its running report as fresh. Retain raw history.	Source/device freshness comparison.

Evidence already available

The archived final review reports 100 Python API tests, 13 frontend unit tests, 39 browser tests plus 2 isolated browser checks, and 1,200 interleaved virtual-device events with no wrong-slot confirmation. This is existing software evidence at the recorded host baseline, not a new physical test or a live native-platform acceptance result. [7]

After binding or test-lease changes, S1 rechecks ownership immediately before sending. Bytes already on the wire still require generation and revision checks at the receiver. Loss of the host, source or device is represented explicitly; a retained historical color remains visible in the journal but cannot become a fresh current observation.

2.4 S2 Platform adapter and checkpoint builder

S2 translates a native platform observation into an ASM source report and prepares an optional project checkpoint. It contributes to H2 by promptly reporting state and supports the cross-computer use case. Normalization remains separate from authorization: a credential proves who may report, not that a native turn was independently observed. The implemented HTTP boundary currently accepts labeled manual or skill reports; a verified native observer is future integration work. [6]

Table 6. S2 boundary and proposed timing

Input or output	Design definition
Conversation identity	Tuple of platform, host_id and native_thread_id. Session-tree IDs and workspace paths cannot substitute for conversation identity. Child observations cannot silently become followed main conversations.
Event record	Source identity and epoch, event ID, monotonic source sequence, native status, normalized status, provenance, optional native turn ID and verification flag. Duplicates do not renew freshness.
Checkpoint	Project and vault identifiers, creation date/revision, source-version qualifier, context body, digest and referenced code state. Context Git commit and project code commit are distinct.
Proposed timing allocation	Host receive, normalization, scheduling and USB handoff together ≤ 0.35 s for the H2 budget; verify timestamps at the same monotonic clock boundary.

Table 7. Requirements and verification

Requirement and pass threshold	Equipment and verification procedure	Record
S2-R1 Five normalized states map correctly; unsupported or ambiguous native reports become unknown.	Use one chosen native platform and a labeled event capture. Generate ten examples per state plus ten ambiguous reports. Compare captured source state, normalized state and provenance; require all 60 mappings correct before enabling automatic observation.	Mapping table and redacted native evidence.
S2-R2 No source/epoch replay changes a different project; proposed receive-to-dispatch ≤ 0.35 s in $\geq 95/100$ trials.	Inject 100 reports with monotonic host timestamps, including duplicate IDs and old epochs. Compare outbox and device write times; require no unauthorized projection, and measure accepted new-report latency separately from rejected cases.	Identity rejection log; 100 timing samples.
S2-R3 Ten two-computer round trips recover the intended checkpoint without conflating code and context versions.	On A save a known checkpoint; execute the sequence in Figure 5. On B verify its digest and identifiers, explicitly prepare the required code state, and manually resume the native platform. Reverse the trip; count ten complete round trips.	Checkpoint IDs, both code heads, digest and outcome.

2.5 S3 Authorization and context storage

S3 keeps sensitive context behind an authenticated boundary and makes a card a locator rather than a credential. It protects the association underlying H1 and the optional continuity workflow. Current context data is stored locally in immutable records; optional Git synchronization publishes selected project records to an authorized vault. No full context body or secret belongs on the tag. [8]

Table 8. S3 authorization and storage boundaries

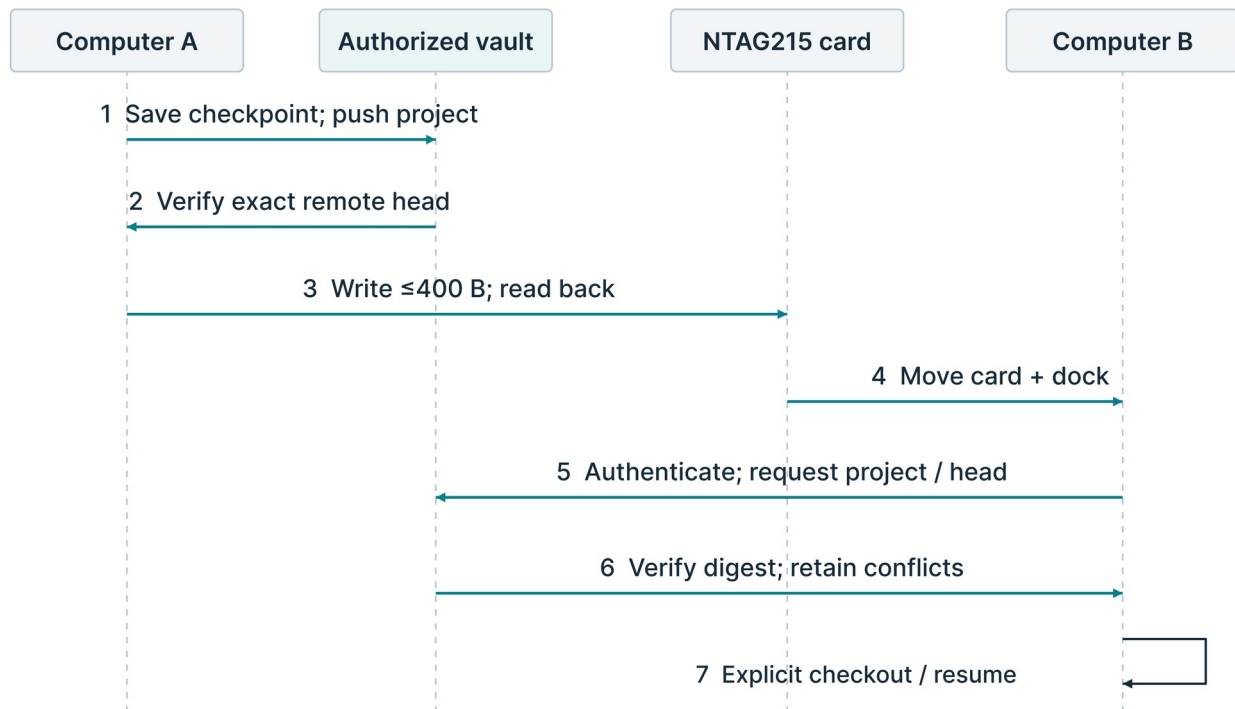
Boundary	Implemented contract or required extension
Local service	Loopback Host and Origin restrictions. Mutations and context/sync reads require the operator capability; ordinary runtime reads are not a confidential multi-user boundary. Store operator credentials with owner-only file permissions.
Project scope	Producer credentials only ingest enrolled-source events. Context project keys must resolve to registered projects; an arbitrary tag cannot grant access to a foreign vault or project.
Commit and sync	Write immutable local records and retain conflicts. Only after the exact remote checkpoint head is verified may the host generate a card pointer. A local commit or queued push is insufficient.
Pointer budget	Version, vault, project, head, date, revision and SHA-256 digest. Planned physical storage budget ≤400 bytes including Type 2 TLV and terminator; detailed accounting in S4.

Table 9. Requirements and verification

Requirement and pass threshold	Equipment and verification procedure	Record
S3-R1 All 10 unauthenticated and 10 foreign-project attempts disclose no protected context.	Use two registered project fixtures and an unauthorized client. Omit or corrupt the operator credential, then supply a foreign vault or unregistered project key. Inspect HTTP responses and returned files; require no protected payload.	20-case access log; redacted request metadata.
S3-R2 No card-write eligibility until the exact remote head is verified; conflicts preserve both records.	Use an isolated test Git remote. For ten trials interrupt sync, change the remote head or create concurrent records. Inspect card-preview eligibility, both source files and conflict UI; require no silent overwrite or stale success.	Local/remote heads, conflict IDs and eligibility result.
S3-R3 Interrupted physical writes never authorize a partial record as valid.	After S4 exists, cut NFC field or remove card at each chunk boundary over 20 writes. Reinsert, read the entire payload and validate length/digest. Reject incomplete content and retain the last cloud checkpoint for explicit recovery.	Byte dumps, failure phase and recovery result.

Cross computer transaction and recovery

Checkpoint handoff across two computers



Context version $\neq$ code version. Physical card I/O and native resume remain planned.

Figure 5. Optional checkpoint handoff. Storage and preview exist in the host foundation; physical card write/read and verified native resume remain to be implemented.

A save first creates an immutable context record under the authorized project. The host distinguishes a dirty or unpushed code tree from a verified code head and never advertises those states as interchangeable. After synchronization, it verifies the intended remote head, encodes the pointer and requests a bounded NFC write. Readback must match the exact bytes before the interface reports card-update success.

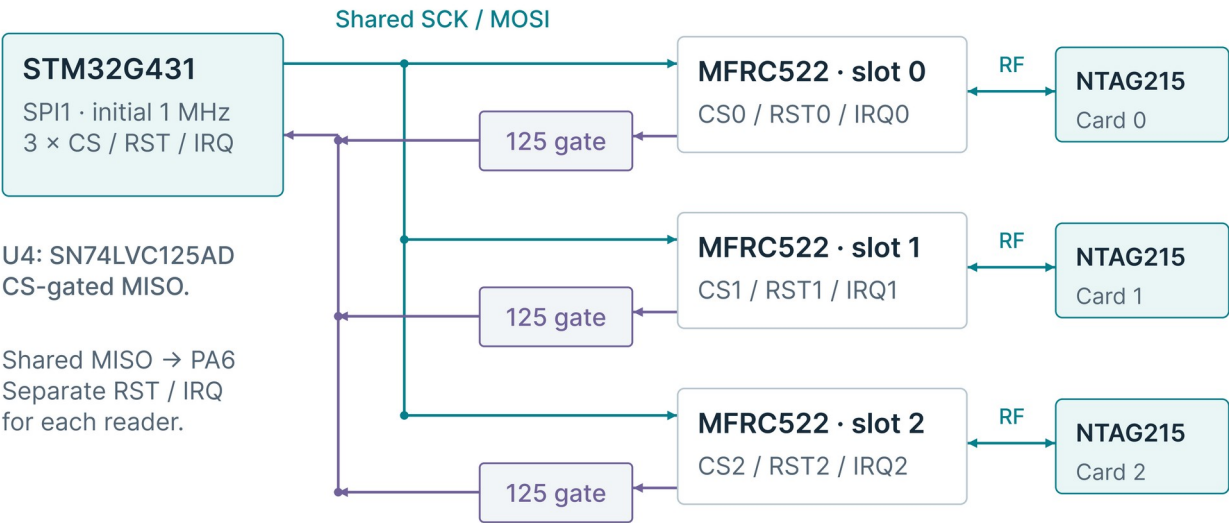
On computer B, possession of the card does not establish vault access. The user authenticates, retrieves the referenced record, verifies its digest and selects the intended local project. If B has a conflicting record, both versions remain visible and automatic continuation pauses. The user prepares code separately and explicitly resumes the native platform; the current system does not restore a hidden model process or promise identical internal agent state.

The SHA-256 field detects accidental corruption of a canonical pointer. It is unkeyed and is not authentication. A readable or copied NFC tag must not expose a bearer token, SSH credential, prompt body or private workspace path.

2.6 S4 NFC read write and fixed slots

S4 detects a project card in each fixed slot and exchanges its compact locator with S5. Three HiLetgo RC522 modules use the MFRC522 13.56 MHz frontend and three NTAG215 tags retain the proposal choice. NTAG215 provides 504 bytes of user memory. The design reserves only 400 bytes including framing, leaving room beyond the application record. Cards remain stationary and only one RF field is enabled at a time to reduce adjacent-slot coupling. [9] [10]

Three readers share one buffered MISO bus



13.56 MHz • Shared 3.3 V supply • Only one reader RF field is enabled at a time

Figure 6. Separate raw MISO lines pass through CS-enabled U4 buffers into one shared SPI1_MISO input at MCU PA6. RF activity is sequenced in firmware.

Table 10. S4 electrical and polling interface

Signal or operation	Quantitative design
Power and logic	3.3 V switched NFC rail; all readers remain electrically powered during normal polling. Start SPI at 1 MHz; MFRC522 bus capability is not a guarantee for the assembled harness.
MISO and control	J6/J7/J8 pin 5 feed separate NFC1/2/3_MISO_RAW nets into U4 pins 2/5/9. U4 outputs 3/6/8 share SPI1_MISO at U1 pin 20 (PA6). CS drives U4 enables 1/4/10. Three RST and IRQ lines remain separate. Raw outputs are not directly joined; isolation means tri-state buffering, not galvanic isolation.
Reset and startup	RST is push-pull low for ≥1 ms then driven high. At nominal 3.3 V, bench targets are ≤0.4 V low and ≥2.9 V high. Wait at least 30 ms after NFC power enable before initialization.
Polling target	Poll all three slots within 300 ms with only one RF field active. Require two consecutive matching polls before a stable insertion/removal event; report within 1 s. These are firmware targets to verify.

RST uses a 100 kΩ weak pulldown; a module pullup may defeat passive reset. Confirm the received module bias and active-drive current rather than assuming the resistor guarantees reset. Before disabling NFC power, place SPI and controls in safe states to avoid back-powering the reader. [11]

S4 record size and verification

Table 11. Computed canonical pointer sizes

Record case	JSON	NDEF	Type 2 framing	Stored total
40-character checkpoint head	266 B	304 B	5 B	309 B
64-character checkpoint head	290 B	328 B	5 B	333 B
Application hard limit	Variable	≤395 B when extended TLV is used	4 B TLV header + 1 B terminator	≤400 B

The calculation uses two 36-character UUIDs, a maximum 10-digit revision, an ISO date, a 64-character SHA-256 digest and MIME type application/vnd.asm.pointer+json. The current host preview checks NDEF length ≤400 bytes. Physical firmware must add a stricter preflight for TLV plus terminator ≤400 bytes; this is a required extension, not an already implemented check. Proposed 128-byte NFC chunks fit the 512-byte complete USB envelope; the representative maximum-counter frame is 375 bytes.

Table 12. Requirements and verification

Requirement and pass threshold	Equipment and verification procedure	Record
S4-R1 H1 detection ≥196/200 events per slot, zero wrong-slot assignment.	Use three labeled NTAG215 cards, timestamped host/device logs and video. Execute 100 insertion/removal cycles per slot; rotate project identities and test neighboring occupied slots. Compare physical action, card UID/record and assigned slot.	600-event CSV with false, missed and duplicate events.
S4-R2 100% exact readback in 100 full writes per tag; all oversized or malformed records rejected.	Use the three readers and tags on a current-limited supply. Write known records spanning 309–400 stored bytes, read all pages back and compare byte for byte. Attempt 401-byte records and bad digests; require explicit rejection.	300 write/read pairs; length and digest logs.
S4-R3 Reset succeeds in 100 cold starts and 100 reset pulses per reader.	Probe RST at each module header with an oscilloscope. Verify low/high levels, ≥1 ms low pulse and ≤2 mA steady GPIO drive target. Read the device version after every cycle; inspect back-power behavior with NFC rail off.	600-cycle result and representative waveforms.
S4-R4 Only one active RF field; scan ≤300 ms and stable event ≤1 s.	Use a near-field pickup loop and oscilloscope at all three antennas, with logic-analyzer CS/RST traces. Run 100 scans with adjacent tags, motors off then moving. Require no wrong-slot record and no simultaneous field enable.	Field timeline, scan percentiles and RF failure log.

Module UID selection alone is insufficient to prove the physical slot if adjacent antennas read the same card. Fixed geometry, sequential RF control and the complete H1 test must establish that association.

2.7 S5 MCU communication and state control

The STM32G431RBT6 in LQFP64 provides the GPIO budget, USB Full Speed interface, timers and serial peripherals required to control three independent slots. It replaces board-specific assumptions with an explicit 64-pin interface map in Appendix B. Internal HSI16/PLL and HSI48/CRS are the clock plan; USB clock accuracy and enumeration are acceptance items. The MCU owns motion timing and protection while the host owns project meaning. [12] [5]

Table 13. S5 resource and identity budget

Resource	Allocation and constraint
Motor outputs	12 GPIOs PC0–PC11 in three groups of four. These are phase inputs to external ULN2003 boards, not STEP/DIR. Maximum two phases per motor energized.
NFC	SPI1 PA5/PA6/PA7 plus 9 independent CS/RST/IRQ lines. PB9 switches the common reader rail.
Feedback and safety	PA0–PA2 Hall inputs; PA15 conditioned VBUS presence; PB7 shared fault; PB5 motor enable; PA3/PA4/PA8 validity, qualification and heartbeat indications.
USB and debug	PA11/PA12 D–/D+; internal UCPD/DBCC sink network uses PA9/PB6 and PA10/PB4. PA13/PA14 SWD, PG10 reset, PB8 BOOT0.
Connection identity	New host epoch per connect and device boot identity per reboot, each 32 lowercase hex digits. Three bounded snapshots reconcile before any target dispatch.

Binary wire format

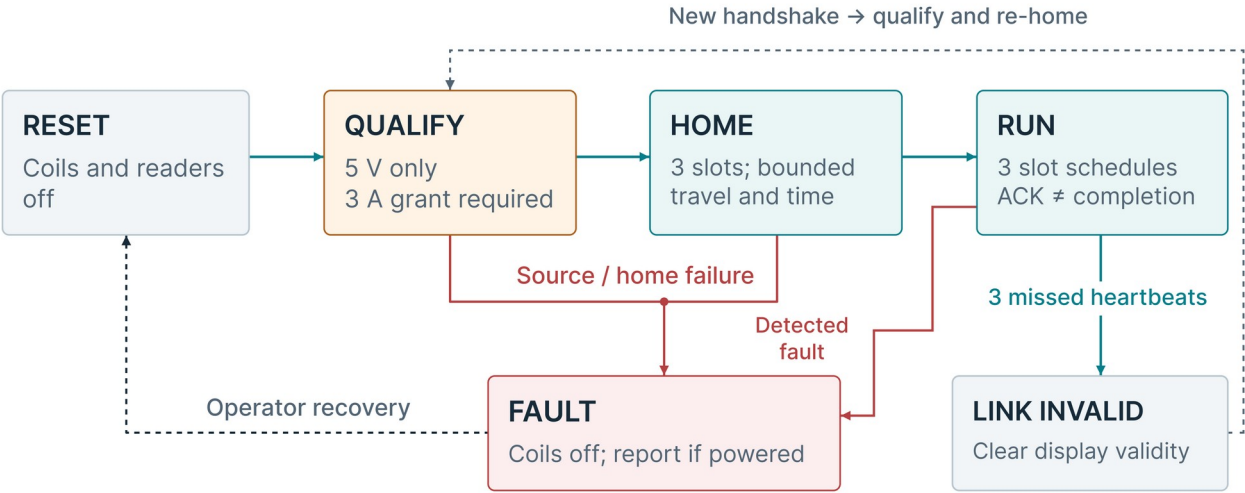
Table 14. Complete frame is at most 512 bytes

Field	Bytes	Encoding
Magic / version / type	2 + 1 + 1	ASCII AS; version 1; enumerated message type
Payload length / sequence	2 + 4	Little-endian unsigned integers
Payload	0–498	Compact UTF-8 JSON object
CRC	4	Little-endian CRC-32/ISO-HDLC over 10-byte header and payload

Types 1–10 cover hello, capabilities, heartbeat, snapshot, set, ack, state, home, stop and fault. Types 11–12 reserve NFC write/read chunks. CRC detects transport corruption; it does not authenticate a host. The current codec rejects unknown types, duplicate JSON keys, invalid Unicode, oversized payloads and stale sequence/identity combinations. [6]

S5 scheduling and fault states

Proposed MCU lifecycle and recovery paths



Homing establishes a reference; pulse counting cannot detect every mid-travel jam.

Figure 7. Proposed MCU lifecycle. Loads default off; recovery is bounded and never treats an ACK as mechanical completion.

After source qualification and reader initialization, the firmware homes each display and then exchanges snapshots. A SET for the current epoch, boot, generation and revision is accepted with an ACK target of 100 ms. A separate STATE report is emitted only after movement, settling and a valid position estimate. The parser retains at most 512 candidate bytes, times out incomplete candidates after 250 ms and advances one byte on corrupt framing to resynchronize.

Each slot has its own target, calibrated position, phase index and timer deadline. A shared scheduling tick services all three channels without waiting for a complete move on one channel. At the 300 pulses/s candidate rate, timer events are approximately 3.33 ms apart. Firmware must bound work per tick and maintain USB parsing and 1 Hz heartbeats during motion. Homing first backs away if the Hall signal is active, then approaches the reference in a fixed direction; travel beyond 1.2 calibrated revolutions or 20 s, whichever occurs first, causes a fault.

A missing expected Hall edge, motion deadline or stop request invalidates position and disables coils. Pulse counting cannot detect every stall between Hall crossings: STATE reports a calibrated position estimate, not independent optical confirmation. S6-R4 must test non-home stalls; additional feedback or a revised mechanism is needed if faults escape detection. One controlled rehome may follow obstruction removal; no endless restart is allowed. An eFuse latch can remove MCU power and require external power removal.

Table 15. Compact payload keys used by the existing contract

Wire aliases	Meaning
e, b, c	connection_epoch, device_boot_id, command_id; 32 lowercase hex digits
s, g, r	slot_id 0–2, binding_generation uint32, target_revision uint32
t, k, h, v	status, color, homed, display_valid
NFC extension	offset, total ≤400 and base64 data; schema exists but physical workflow is reserved

S5 verification

Table 16. Requirements and verification

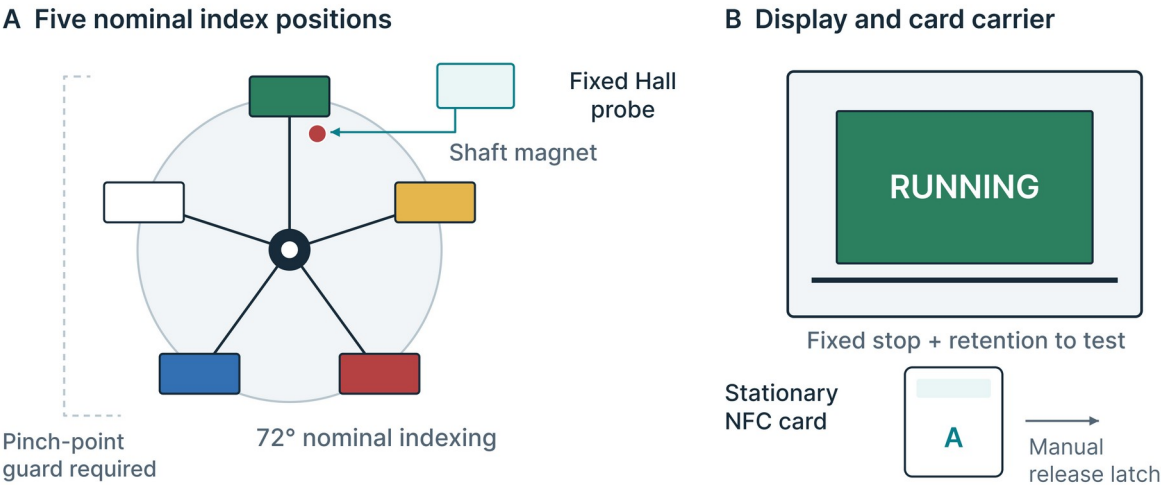
Requirement and pass threshold	Equipment and verification procedure	Record
S5-R1 Accept valid complete frames up to 512 B; reject 513 B and all corrupted or stale frames.	Use codec fixtures, then a USB/serial bench peer. Construct schema-valid 511/512 B frames; reject a 14 B empty payload and 513 B frame. Split header boundaries, corrupt CRC, inject duplicate keys and replay old epoch, boot, generation and revision. Require zero unauthorized state applications.	Frame corpus, rejection reason and parser memory bound.
S5-R2 ACK ≤ 100 ms for 100 accepted SET commands; ACK cannot mark motion complete.	On actual hardware record host send, ACK and final STATE monotonic timestamps while ≥ 60 fps video records the face. Use mixed short/long moves. Require every ACK within 100 ms and no fresh observation before valid completion.	100-command timeline and video alignment.
S5-R3 H2 $\geq 95/100$ transitions per slot finish correctly within 15.0 s while all three change.	Use the 20 ordered state pairs $\times 5$ plan for each slot, permuted across simultaneous commands. Time from host control receipt to a stable correct face; check the separate validity indicator and final matching STATE.	300 slot timings; per-slot success counts.
S5-R4 All 10 forced home failures stop within 20 s or 1.2 revolutions, whichever occurs first.	Use a current-limited bench source and guarded mechanism. Hold Hall high/low or disconnect it in ten trials; monitor phase outputs and MOTOR_EN. Require coils off, invalid state and explicit fault, with no endless restart.	Fault code, pulse count and shutdown time.
S5-R5 Reconnect never replays old motion as current; link loss removes validity by 3.5 s.	Disconnect USB during ten moves, reboot during ten more and rebind before ten delayed reports. After reconnect accept new identity and all snapshots first. Require old ACK/STATE rejected and explicit rehome when position is unknown.	30 recovery traces and observed face checks.

Verification uses a bench peer before a real computer port is exposed to the assembled circuit. A virtual transport validates serialization and ordering but cannot establish USB electrical behavior, firmware deadlines or mechanism position. Current firmware implementation and serial bring-up are still required deliverables.

2.8 S6 Flip mechanisms and position feedback

S6 provides the room-visible state required by H3 and the repeatable movement required by H2. Each slot uses a purchased 5 V 28BYJ-48 geared stepper and a separate ULN2003AN driver module. The driver module is included in the motor-kit cost. The old proposal motor resistance, step count and ULN2003LV assumptions do not describe this assembly. [13] [14]

Flip mechanism concept and home reference



Concept only. One Hall reference does not measure every page or detect every mid-travel stall.

Figure 8. Five-position flip concept. Shaft magnet and fixed Hall sensor establish a home reference; final leaf geometry, stops and retention must be prototyped.

Table 17. Motor and mechanism design basis

Parameter	Design basis or assumption
Motor	Family guide: 50 Ω ±7% per winding at 25 °C, nominal 1:64 gearbox. Approximately 2048 full steps or 4096 half-steps per output revolution; measure the received gearbox ratio.
Drive	Four 3.3 V phase inputs per module; at most two coils per motor energized. Verify module input response and Darlington loss under load. A printed 5–12 V module marking does not permit 12 V on a 5 V motor.
Geometry	Five nominal 72° positions; ≥80 × 60 mm visible color. Fixed stops, gravity or a passive latch must retain a stable selected leaf.
Position feedback	One DRV5023AJELPGMQ1 home sensor per slot; step counting estimates intervening positions. Hall alone does not independently identify every visible leaf.

The candidate movement rate is 300 half-step pulses/s with a ramp allowance. Rated low-speed torque cannot be assumed at that rate or after the ULN2003 voltage drop. Actual leaf inertia, friction and required holding power remain unmeasured.

S6 Hall margin and verification

The Hall probe uses 3.3 V power, local 100 nF bypass and an open-drain output. The mainboard adds a 4.7 k Ω pullup and 220 Ω series resistor; optional 1 nF capacitors C12–C14 are DNP. For the AJ magnetic option, the published operate threshold reaches 12 mT and release threshold falls to 1 mT. Position the correct magnet pole so the home field exceeds 12 mT and the away field is below 1 mT across assembly tolerances. Without a field model, those are test conditions, not a justified fixed gap. [15]

Table 18. Requirements and verification

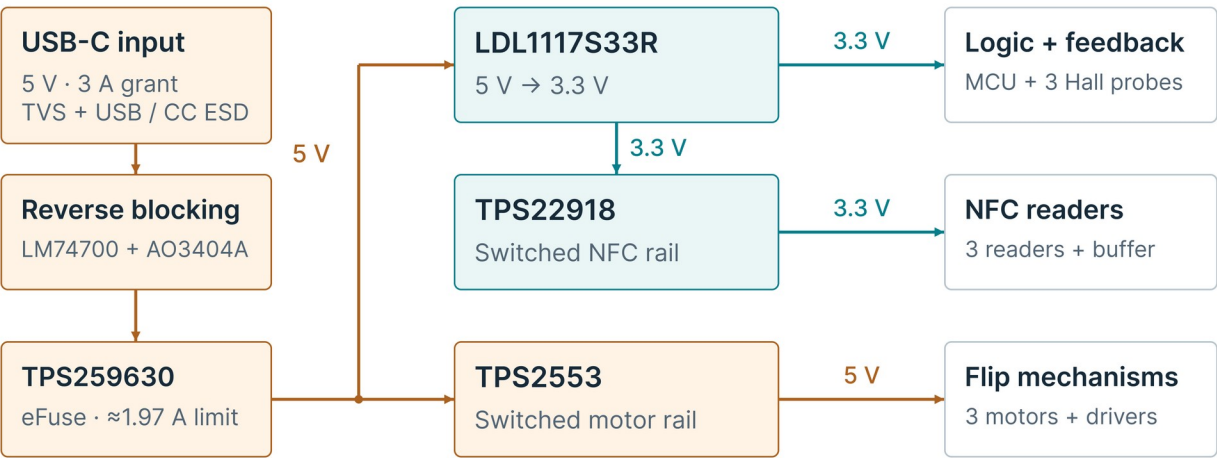
Requirement and pass threshold	Equipment and verification procedure	Record
S6-R1 H3 $\geq 57/60$ correct identifications per tester at both 4 m and 5 m.	Use ≥ 3 consenting testers, lux meter, tape measure and azimuth marks. Run 60 randomized presentations per tester per distance under 300–500 lux, 20 at each of $0^\circ/\pm 30^\circ$. Allow no host UI cue; score the five states.	≥ 360 responses with light, angle and distance records.
S6-R2 Homing repeatability within $\pm 2^\circ$ and no missed reference in 100 cycles per slot.	Mark a shaft reference and use a calibrated protractor or video angle measurement. Approach Hall from the same direction 100 times from randomized starts. Check trip position, full turn count and independent visible leaf alignment.	300 angle samples and worst-case error.
S6-R3 Selected leaf remains stable for 60 s in 20 trials per state and slot.	With the assembled guarded mechanism, command each state, settle and remove coil holding power if passive retention is intended. Observe for 60 s. Require no unintended leaf change; if holding coils are necessary, repeat the S7 thermal/current test.	300 retention trials and actual holding-current decision.
S6-R4 All 10 intentional stalls enter a safe invalid state; manual recovery returns correct home.	Use a guarded nonconductive obstruction at low bench current; include stalls away from home. Require fault shutdown and no false completed STATE. A timeout without feedback may miss these stalls; record failure and revise sensing/mechanics if so. Disconnect power to clear, inspect and explicitly rehome.	Fault latency, damage inspection and recovery face.
S6-R5 Magnetic and wiring margins remain valid through assembly tolerance.	Check three probes with adjustable gap and magnet orientation. Measure field using a calibrated meter if available; otherwise record operate/release positions and reserve adjustable travel. Test cable open and stuck-low cases; high alone cannot distinguish absence from open circuit.	Per-slot gap/angle limits and failure classification.

The $\pm 2^\circ$ home target is an engineering allocation to be discussed with the TA. A repeatable Hall edge is necessary but is not proof of adequate visible leaf alignment or all-state absolute feedback.

2.9 S7 Power distribution

S7 uses one USB-C cable for data and 5 V power. Source-current permission is separate from overcurrent protection: the selected eFuse threshold can exceed a 1.5 A port grant, so full operation requires a verified 3 A Type-C advertisement or an explicitly negotiated 5 V / 3 A supply. No higher USB PD voltage may be requested. Default and startup operation keeps motors and NFC off within the applicable attach/enumeration limits. [16] [17]

Protected input and switched power domains



MCU enables default off. The eFuse latch can remove MCU power; faults are reported when powered.

Figure 9. Selected v0.1.0 power tree. The load switches are controlled by MCU enables with default-off pulldowns.

Table 19. Power selection rationale

Stage	Selection and design reason
Input and reverse blocking	SMF6.0A-T13 TVS, LM74700QDBVTQ1 controller and AO3404A MOSFET. Block reverse current into the source and protect the downstream rail; verify polarity and reverse behavior.
Main protection	TPS259630DDAR eFuse controls current, voltage thresholds and rise time. Fault indication is shared with the motor switch.
Logic	LDL1117S33R LDO supplies 3.3 V. Provisional sustained logic load ≤0.20 A pending measured thermal qualification.
Branches	TPS2553DBVR-1 supplies three external motor boards. TPS22918DBVT soft-starts three readers and their MISO buffer. Hall probes remain on the logic rail.

Primary part data: eFuse [18], reverse controller [19], MOSFET [20], LDO [21], motor switch [22] and NFC switch [23]. TVS and ESD components do not establish USB, ESD or fault certification.

S7 protection settings and load budget

Table 20. Power settings from the current source and calculations

Setting	Current schematic value	Calculated meaning and limitation
eFuse current	R39 = 464 Ω , 1%	Nominal 1.97 A; reviewed screening range approximately 1.75–2.20 A. Confirm the actual trip spread on hardware. Rmin = 459.36 Ω exceeds the cited 453 Ω recommendation.
Voltage windows	249 k Ω / 100 k Ω UVLO; 374 k Ω / 100 k Ω OVLO	Nominal 4.188 V and 5.688 V using a 1.2 V threshold. Resistor-only 1% ranges 4.129–4.248 V and 5.599–5.779 V exclude comparator tolerance.
eFuse slew	C16 = 220 nF	Reference calculation $\approx$ 0.201 V/ms or 24.9 ms to 5 V. Measure startup with all real branch capacitances.
Motor limit and bulk	R42 = 26.1 k Ω , 1%; C24 = 220 μ F $\pm$ 20%, 10 V	Predicted limit 0.908/0.989/1.081 A min/nom/max. Latched fault needs enable cycling. Wait $\geq$ 20 ms after rail enable before energizing coils.
NFC slew and discharge	C26 = 4.7 nF; R44 = 100 Ω	Typical rise $\approx$ 8–9 ms; allow 30 ms before reset/init. With 100 μ F assumed downstream and 25 Ω typical switch discharge resistance, 90%–10% fall $\approx$ 27.5 ms.
Presence signal	47 k Ω / 150 k Ω divider, 1 nF, SN74LVC1G17	Divider ratio 0.761 and RC $\approx$ 35.8 μ s. PA15 is digital VBUS presence, not an ADC voltage or a source-current permission measurement.

Table 21. Provisional full-system load allocation

Load	Budget	Reason
Three motors and driver modules	0.80 A on motor rail	Six energized 46.5 Ω windings at 5.5 V bound coil current at 0.710 A ignoring driver loss; remaining allowance covers module indicators and variation.
All 3.3 V consumers	$\leq$ 0.20 A sustained provisional	Must include MCU, all powered readers, Hall probes, MISO buffer and indicators. Three Hall sensors alone can require 10.5 mA at the data-sheet maximum.
Input allocation	Approximately 1.0 A plus protection losses under the provisional logic limit	A 10 W connector-level ceiling is an upper project budget, not measured demand. 3 A permission is required by protection coordination, not this arithmetic alone.

The earlier 0.60 A logic allocation comprised 0.15 A MCU, 0.30 A readers, 0.03 A Hall, 0.02 A buffer/LED and 0.10 A margin. That allocation is not demonstrated compatible with the present LDO. Disabling RF on two readers does not remove their board idle current. If measured sustained load exceeds 0.20 A, revise the regulator or power architecture and repeat qualification before full operation.

S7 power verification

Table 22. Requirements and verification

Requirement and pass threshold	Equipment and verification procedure	Record
S7-R1 Full operation only after a verified 3 A grant; no requested voltage above 5 V.	Use a Type-C source analyzer or controlled source emulator. Test default, 1.5 A and 3 A advertisements in both cable orientations, ten attachments each. Monitor MOTOR_EN/NFC_EN and startup draw; require inhibited full operation below the accepted grant.	60 attach traces and measured source permission.
S7-R2 3.3 V remains 3.135–3.465 V; motor distribution loss ≤ 0.25 V during H2.	Use a current-limited supply at 4.75, 5.00 and 5.25 V, oscilloscope at TP1, TP3, TP5 and the farthest module ground/rail. Run all three worst-case moves; capture extrema and startup. Require no MCU reset or false Hall/NFC event.	Rail waveforms, cable/board drops and total current.
S7-R3 Sustained 3.3 V load ≤ 0.20 A and estimated junction ≤ 100 °C at 40 °C ambient.	Measure current and regulator case temperature after ≥ 20 min worst steady operation, with enclosure fitted. Use a justified thermal model to bound junction temperature; surface temperature alone is insufficient. Repeat readers on, moving and holding cases.	Ambient, case, current, thermal model and pass margin.
S7-R4 Overload and branch shorts disable power without uncontrolled restart or reverse source current.	Use bench supply and electronic load, never a laptop as fault source. Increase input/branch load to map trip thresholds, then inject a limited branch short in ten trials. Test output energized/input removed with safe current limiting; measure reverse current target < 1 mA.	Trip/current/temperature traces and latch recovery.
S7-R5 No unsafe back-power path through NFC, SWD or USB.	With normal power disconnected, exercise each auxiliary interface under current limitation. Check 3.3 V and 5 V rails, supply current and pin levels. Require no unintended MCU/reader operation and no component absolute-maximum violation.	Power-state matrix and leakage measurements.

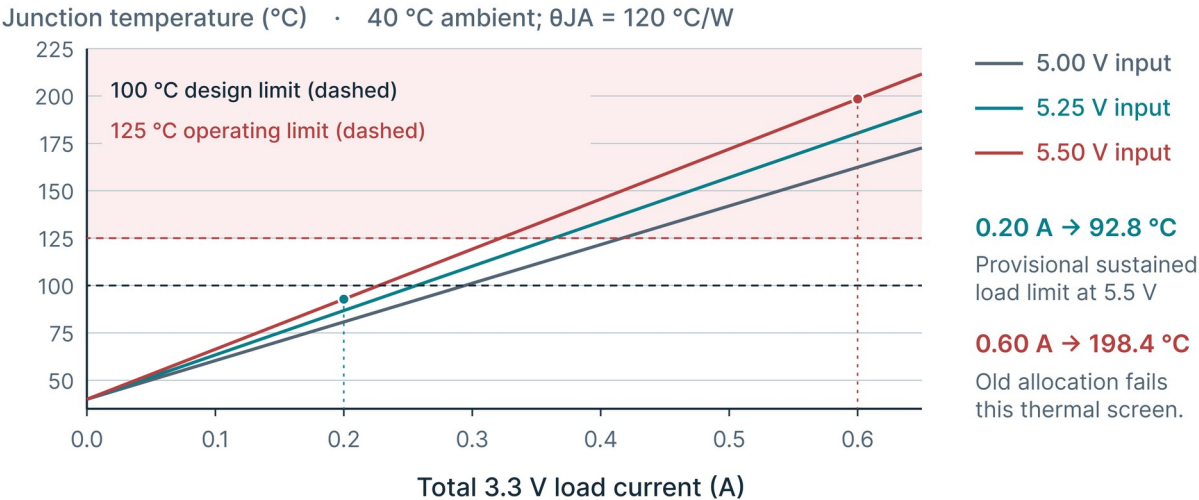
Preserve the MCU internal sink/dead-battery Rd scheme through firmware handover. Do not parallel external 5.1 k Ω Rd resistors. Release PB4 from full JTAG while retaining SWD. U6 tab is the 3.3 V output, not ground. The CC ESD array does not provide a DC short-to-VBUS guarantee.

2.10 Tolerance analysis of the power path

The 3.3 V thermal path is the primary tolerance analysis because a regulator that overheats would invalidate NFC, USB and all three status displays together. The following calculation screens feasibility using 40 °C internal ambient and the data-sheet 120 °C/W junction-to-ambient reference. Board copper and enclosure airflow may change that resistance; it is not a measured property of this board.

$$P_{LDO} = (V_{IN} - 3.3 \text{ V}) I_{3V3}; T_J = T_A + \theta_{JA} P_{LDO}$$

LDO thermal margin under the screening assumptions



Calculated screening model; board thermal resistance and actual load still require measurement.

Figure 10. Calculated LDO screening temperature versus current. Values above the operating limit indicate an infeasible allocation under these assumptions, not a predicted safe operating state.

Table 23. LDO corner calculations

Input	Current	Dissipation	Screening junction	Assessment
5.00 V	0.20 A	0.34 W	80.8 °C	Below 100 °C target
5.00 V	0.60 A	1.02 W	162.4 °C	Fails screening
5.25 V	0.20 A	0.39 W	86.8 °C	Below 100 °C target
5.25 V	0.60 A	1.17 W	180.4 °C	Fails screening
5.50 V	0.20 A	0.44 W	92.8 °C	Below 100 °C target
5.50 V	0.60 A	1.32 W	198.4 °C	Fails screening

At 5.5 V, a 0.60 A load dissipates 1.32 W. Keeping junction temperature below 125 °C at 40 °C ambient would require effective thermal resistance $\leq 64.4 \text{ °C/W}$; the 100 °C design target requires $\leq 45.5 \text{ °C/W}$. No such board-level measurement exists. At 0.20 A, the screening estimate is 92.8 °C; the calculated 100 °C current ceiling is 0.227 A, leaving only 27 mA of current margin. The 5.5 V case is a stress screen, not the normal USB input target.

Power transient and voltage margin

Dropout and distribution

At the lowest 4.75 V qualified input and a 0.25 V total upstream drop, the LDO sees 4.50 V. Headroom above a 3.3 V output is 1.20 V, exceeding the published 0.60 V maximum dropout at 1.2 A under the specified data-sheet conditions. The 0.25 V loss allowance must be measured across cable, reverse path, eFuse, connectors and traces; route geometry alone cannot prove it. [21]

$$V_{HEADROOM} = 4.75 - 0.25 - 3.30 = 1.20 \text{ V}$$

Motor inrush and reservoir

For C24 = 220 μF ±20%, minimum capacitance is 176 μF and maximum is 264 μF. Using the lower 0.908 A switch limit, ideal charging of 264 μF to 5.5 V takes 1.60 ms, below the 5 ms minimum fault deglitch reference. The result neglects extra module capacitance, source impedance and coil load; coils stay off during the ≥20 ms branch-enable wait.

$$t_{CHARGE} = C_{MAX} V / I_{LIMIT, MIN} = 264 \text{ }\mu\text{F} \times 5.5 \text{ V} / 0.908 \text{ A} = 1.60 \text{ ms}$$

A 0.20 A supply deficit lasting 0.20 ms produces 0.227 V of capacitive droop at the minimum C24 value, before ESR. This nearly consumes the 0.25 V distribution allowance. Stagger phase edges if needed, but maintain three concurrent motion schedules; serializing complete slot moves could violate H2. Record rail droop and phase timing on the same oscilloscope capture.

$$\Delta V = \Delta I \Delta t / C_{MIN} = 0.20 \text{ A} \times 0.20 \text{ ms} / 176 \text{ }\mu\text{F} = 0.227 \text{ V}$$

Table 24. Conditions needed to close the power analysis

Uncertainty	Why it matters	Decision rule
Actual logic current and thermal resistance	The old 0.60 A allocation fails the screening model.	Measure every powered reader and MCU case; revise regulation if ≤0.20 A or ≤100 °C cannot be established.
Motor module loss and harness resistance	Darlington and wire losses reduce torque and increase time.	Measure voltage at the motor module during maximum move; validate H2 at the lowest permitted rail.
Comparator and switch tolerances	Resistor-only voltage calculations omit IC threshold tolerance.	Sweep the bench input and loads; record actual UVLO/OVLO/current limits before computer attachment.
Transient interactions	Three motor steps can corrupt NFC or reset the MCU.	Repeat H1/H2 with readers polling and all motors moving; revise decoupling, routing or scheduling on any error.

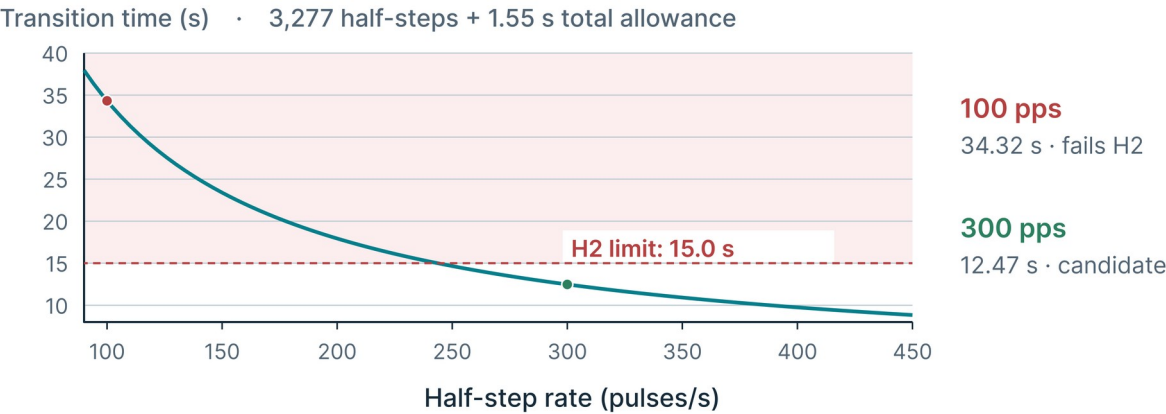
This analysis identifies a feasible conditional operating point, not a closed full-system power proof. The team must resolve the measured load and regulator thermal path with the TA before releasing the assembled configuration.

Motion time and home position tolerance

For a unidirectional five-position mechanism, the longest commanded move is four of five output revolutions. A nominal 4096-half-step gearbox therefore needs $\text{ceil}(4096 \times 4/5) = 3277$ pulses. This is a screening model until the actual gearbox ratio and leaf stop positions are calibrated.

$$T_{TOTAL} = T_{HOST} + N_{MOVE} / f_{STEP} + T_{RAMP} + T_{SETTLE}$$
$$f_{MIN} = 3277 / 13.65 \text{ s} = 240.1 \text{ pulses/s} \quad \text{before ramp allowance}$$

Worst-case transition time versus step rate



The 300 pps candidate requires loaded-motion validation, including simultaneous three-slot operation.

Figure 11. Calculated worst-case transition at several rates. The curve includes 0.35 s host/USB allowance, 0.20 s ramp allowance and 1.00 s settling.

Table 25. Motion calculation and calibration

Case	Calculated time	Conclusion
100 half-step pulses/s	32.77 s movement alone	Fails 15 s requirement.
300 half-step pulses/s	$10.923 + 0.20 + 0.35 + 1.00 = 12.47 \text{ s}$	2.53 s timing margin if the real mechanism sustains the rate.
Nominal indexed offsets	0, 819, 1638, 2458, 3277 half-steps	Use rounded absolute offsets; do not repeat one rounded increment indefinitely.

Half-step quantization alone is $\pm 0.044^\circ$ at a nominal 4096 steps/revolution. It is much smaller than the provisional $\pm 2^\circ$ home repeatability allocation, but backlash, Hall threshold spread, magnet geometry and leaf friction are not included. Always approach home from one direction. Calibrate page positions using visible leaf alignment and periodically rehome to detect accumulated lost steps.

The motor guide gives a $>34.3 \text{ mN}\cdot\text{m}$ torque reference at 120 Hz and no-load pull-in/pull-out frequencies; neither guarantees loaded operation at 300 Hz. Measure stall margin using the real leaf assembly at minimum motor voltage, then run all H2 ordered-pair trials. If the timing and retention tests fail, reduce inertia/friction or change the mechanism/drive before claiming H2 compliance.

3 Cost and schedule

3.1 Complete project cost

Every material item is valued as if purchased online, including parts already purchased and components supplied by the school. The ledger starts with the current native assembly quantities and consolidates repeated MPNs. It adds three NTAG215 tags, all mechanism and enclosure printing, interconnect, fasteners, fabrication and one dedicated development board. DNP capacitors, copper test pads and drilled mounting holes have no separate component charge. [24]

Table 26. Full project budget in USD

Category	Unit use / dedicated tool	From-zero budget
Electronics	\$50.43	\$50.43
Mechanical and interconnect	\$54.35	\$67.19
PCB fabrication	\$7.09	\$60.93
Dedicated development equipment	\$20.13	\$20.13
3D printing material	\$14.02	\$48.98
Subtotal before tax and freight	\$146.02	\$247.66
Shipping budget	—	\$66.55
Tax planning reserve	—	\$24.77
Nonlabor project outlay	—	\$338.98
Budget labor	—	\$36,000.00
Grand total	—	\$36,338.98

Unit-use cost allocates only the material consumed by one device, plus the dedicated development tool: \$146.02 before freight and tax. From-zero spend accounts for full supplier packages and quoted PCB batches; unused pack/batch value is \$101.64. The 54 BOM cost lines and separate filament calculations retain supplier URLs, dates, quantities and formulas in `cost_analysis.xlsx` and the cost ledgers.

The mainboard quote is \$55.93 for ten boards, plus \$26.55 estimated freight, and remains subject to audit. It is a known quoted batch, not a proven minimum order. Three Hall boards use a provisional \$5 ten-board manufacturing allowance; a project-specific quote and any panelization charge are still needed. [25]

The \$24.77 tax reserve is 10% of the \$247.66 goods/fabrication/equipment budget. Shipping is \$26.55 mainboard + \$10 Hall PCB allowance + \$30 other supplies, including a \$15 filament-freight reserve. School printing adds no commercial service charge. Reserves are planning allowances, not tax determinations or checkout quotes.

Exact USB cable, fastener and consumable selections are explicit allowances. The motor listing was sold out when observed; its price is a benchmark. The costed NTAG215 inlay is a candidate for encapsulation in the printed carrier, not evidence that tags have already been received.

Printing assumptions and labor budget

Table 27. Provisional 3D printing mass

Printed assembly	Qty	Net g each	Net g
Three complete flip mechanisms including leaves and supports	3	120	360
Complete enclosure	1	400	400
NFC tag housings and card carriers	3	20	60

$$m_{PRINT} = (3 \times 120 + 400 + 3 \times 20) \text{ g} \times 1.20 = 984 \text{ g}$$

An existing school printer is used; only filament is charged at online replacement value. The mass allowance is conservative. A closed 320 × 100 × 100 mm shell with assumed 2 mm walls and 1.24 g/cm³ density weighs about 357 g before cutouts; 400 g allows for mounting features. Kevin’s final CAD slicing will replace these assumptions.

Fifteen nominal 5 g leaves allocate 60 g net to four nonwhite states; the remaining 760 g is white structure and leaves. With 20% support/trials: 912 g white at \$13.99/kg plus 72 g colored at \$34.99/2 kg costs \$14.02 consumed. A from-zero basket is one white spool plus one eight-color mini bundle: \$48.98, with unused filament retained. The bundle includes red, yellow, green and blue. Printer electricity and depreciation remain shared laboratory overhead. [26]

Labor budget

The budget is 12 active weeks × 8 hours per week per person: 96 hours each and 288 hours total. The \$50/hour rate and 2.5 multiplier follow the course convention. These are estimates, not timesheets; roles follow the October 2 team update. [27] [28]

$$C_{LABOR} = \sum_i (\$50 / hour \times 2.5 \times h_i)$$

Table 28. Estimated labor by partner

Partner	Principal responsibility	Hours	Cost
Ziyan Zeng	Software and PCB design; joint testing	96	\$12,000.00
Achintya Mohan	Firmware and drivers; print execution; joint testing	96	\$12,000.00
Kevin Wiszowaty	Mechanical CAD, soldering and assembly; joint testing	96	\$12,000.00

Total labor is 288 × \$50 × 2.5 = \$36,000. Ziyan has completed PCB design and is continuing software implementation. All three share full-system integration and final acceptance testing.

Equipment and unresolved purchases

One NUCLEO-G431KB is counted as project-specific development equipment. Computers, bench oscilloscope, DMM, logic analyzer, current-limited supply, electronic load, lux meter and calipers are shared laboratory infrastructure; reserve access rather than charge a complete new laboratory purchase to one prototype. A Type-C analyzer and magnetic-field meter may be borrowed; if unavailable, add their rental/service quotation before executing the corresponding tests. No machine-shop labor is currently planned.

3.2 Weekly schedule and ownership

Ziyan owns software and PCB design; Achintya owns firmware, drivers and print execution; Kevin owns mechanical CAD, soldering and assembly. All three conduct integrated and final tests. Twelve weeks from September 14 through December 7, excluding fall break, each carry 8 hours per person. Earlier milestones remain calendar context outside this allowance; zero budget hours do not assert zero actual work. Course dates follow the Fall 2026 calendar. [28] [29]

Table 29. Weekly work and acceptance evidence

Week of and milestone	Assigned work and budget hours	Completion evidence
08-24 Team setup; calendar context	Ziyan (unbudgeted): Define use cases. Achintya (unbudgeted): Review device control scope. Kevin (unbudgeted): Review assembly constraints.	Prior preparation; outside the 12-week labor allowance
08-31 Project approval; calendar context	Ziyan (unbudgeted): Review ASM and circuit scope. Achintya (unbudgeted): Review driver feasibility. Kevin (unbudgeted): Survey mechanical packaging.	Prior preparation; no actual hours inferred
09-07 Proposal; calendar context	Ziyan (unbudgeted): Outline host and PCB design. Achintya (unbudgeted): Outline firmware interfaces. Kevin (unbudgeted): Outline housing and assembly.	Proposal goals retained; outside budget weeks
09-14 Proposal revision	Ziyan (8 h): Revise proposal and software contracts. Achintya (8 h): Plan MCU drivers and bring-up. Kevin (8 h): Review enclosure and mechanism concept.	September 18 proposal baseline; planned allocation
09-21 Host foundation and PCB design	Ziyan (8 h): Develop ASM and complete PCB layout. Achintya (8 h): Prepare USB, NFC and motor drivers. Kevin (8 h): Plan stacked packaging and soldering.	Archive host/PCB design evidence; no physical pass claimed
09-28 Design document due October 2	Ziyan (8 h): Document completed PCB design; continue ASM. Achintya (8 h): Review firmware state machine and print setup. Kevin (8 h): Update 320 x 100 x 100 mm CAD concept.	PCB design complete and software in progress per team update
10-05 Design Review	Ziyan (8 h): Present host and PCB; resolve review items. Achintya (8 h): Bring up drivers; print Kevin's fit coupons. Kevin (8 h): Refine CAD; prepare soldering and fixtures.	Review actions assigned; one-slot bring-up plan agreed
10-12 Breadboard Demo	Ziyan (8 h): Connect ASM to firmware; joint slot test. Achintya (8 h): Implement NFC, Hall and motor control; print trial. Kevin (8 h): Wire one slot; check fit and joints; joint test.	All three test one slot and record power/motion evidence

Integration schedule and contingency

Table 30. Weekly work and acceptance evidence

Week of and milestone	Assigned work and budget hours	Completion evidence
10-19 Board assembly and enclosure fit	Ziyan (8 h): Integrate host protocol; support PCB bring-up. Achintya (8 h): Integrate firmware; execute enclosure prints. Kevin (8 h): Solder boards; finish CAD and assemble enclosure.	Joint connector, homing and ACK/completion checks
10-26 Three-slot integration and rework	Ziyan (8 h): Integrate live status and bindings; joint test. Achintya (8 h): Tune three-slot scheduling; reprint corrections. Kevin (8 h): Assemble mechanisms and harness; fix CAD fit.	All three run simultaneous-motion and rail checks
11-02 Progress Demo	Ziyan (8 h): Demonstrate ASM and context handoff. Achintya (8 h): Demonstrate firmware; capture device logs. Kevin (8 h): Demonstrate assembly; record mechanical issues.	Joint integrated demo and H1/H2 pilot trials
11-09 Reliability and correction	Ziyan (8 h): Fix host fault isolation; analyze joint tests. Achintya (8 h): Fix firmware faults; execute revised prints. Kevin (8 h): Correct mechanical fit and solder defects.	Joint H3 pilot, thermal, RF and fault recovery checks
11-16 Mock Demo	Ziyan (8 h): Run integrated cases; analyze host evidence. Achintya (8 h): Run integrated cases; analyze firmware evidence. Kevin (8 h): Run integrated cases; analyze assembly evidence.	All three execute H1-H3 and fault tests; record failures
11-23 Fall break	Ziyan (unbudgeted): No scheduled work. Achintya (unbudgeted): No scheduled work. Kevin (unbudgeted): No scheduled work.	No budgeted hours or assumed laboratory access
11-30 Final Demo November 30 to December 2	Ziyan (8 h): Lead software demo; joint system test. Achintya (8 h): Lead firmware demo; joint system test. Kevin (8 h): Lead assembly demo; joint system test.	Joint final system test, demo and presentations Dec 3-4
12-07 Final papers due December 9	Ziyan (8 h): Integrate report; archive host and PCB design. Achintya (8 h): Archive firmware and printing records. Kevin (8 h): Archive CAD, assembly and soldering records.	All three review test results and submit final papers

October 19 provides soldering, printed-part fitting and firmware integration. October 26 and November 9 reserve correction time within the 8-hour weekly allocations. Fall break carries no budgeted work or assumed lab access. Failed thermal, motion or reader-bus tests take priority over cosmetic changes. Work beyond 288 hours requires a budget revision.

Course dates: Design Document October 2; Design Review week of October 5; Breadboard Demo week of October 12; Progress Demo week of November 2; Mock Demo week of November 16; Final Demo November 30–December 2; presentations December 3–4; final papers December 9.

4 Societal impact standards ethics and safety

4.1 Societal impact and ethics

The intended benefit is a visible, low-interaction aid for a person managing concurrent work. A persistent physical display may reduce repeated window checking, but this is a design motivation rather than a proven health or productivity outcome. H3 is a small engineering readability check; three team testers cannot establish accessibility or effectiveness for a wider population.

Economically, replaceable motors, readers and printed parts can extend service life. An existing school printer reduces fabrication expense to consumed material; reproduction elsewhere may require printer access or commercial service fees. Replacement-part availability and shipping also affect cost. Globally distributed teams may use different host platforms and languages, so the three-slot design should expose plain state labels and user-selected project names.

Socially and culturally, colors have different meanings and are inaccessible to some users. Preserve the five-color contract while adding a redundant word or simple symbol to each leaf and a matching host legend. These markings are a planned accommodation requiring testing, not a change that excuses the original color-recognition requirement. The display should support its owner’s awareness rather than rank employees or expose private work to bystanders.

Environmentally, serviceable connectors and reusable modules reduce replacement of an entire device. Limit prototype printing to fit coupons before full enclosures, record actual scrap, and keep metal, PCB assemblies and plastic parts separable for appropriate disposal. No lower-carbon or lower-energy claim is made without measurements; passive retention only saves holding energy if the mechanism passes its stability test.

Table 31. Ethical duties and design actions

Ethical obligation	Application to AgentDock
Honest technical claims	Label software tests, calculations, design targets and physical measurements separately. Publish failures and remaining uncertainty; never present a stored color as a confirmed current state.
Privacy and informed control	Keep context optional and authenticated; use non-sensitive project labels, store no credentials on tags, and make synchronization selection explicit.
Fairness and accessibility	Use redundant visual labels and voluntary testing. Record recognition failures without attributing them to personal inadequacy.
Respect for others’ work	Cite borrowed diagrams, specifications and code; retain source versions. The supplied sample informs structure, not this project’s results.

These actions apply IEEE duties concerning public welfare, privacy and truthful estimates, and ACM duties concerning harm, privacy and quality. They also address the course requirement to consider the broader consequences of the project. [30] [31] [32]

4.2 Engineering standards and operating safety

Table 32. Applicable standards and evidence boundary

Standard or guidance	Applicable design action and current limit
USB 2.0 / USB Type-C	Use the specified Full Speed data path and sink attach/current-advertisement behavior; verify clock, orientation and source permission. The cited Type-C Release 2.0 is the design reference, not a claim to the newest revision or certification.
ISO/IEC 14443 Type A and NFC Forum Type 2	MFRC522 and NTAG215 provide the intended card interface. Validate NDEF/TLV encoding, readback and adjacent-slot RF behavior; module selection alone does not certify the integrated device.
IEC 62368-1 hazard-based safety	Use the standard’s ICT-equipment scope as design guidance for electrical, thermal and moving-part hazards. No compliance evaluation or product listing has been performed.
FCC Part 15 RF applicability	13.56 MHz intentional-radiator rules are relevant to a reader system. Confirm current applicable limits and module authorization before distribution; no RF emissions testing or certification is claimed here.
Course laboratory safety	Complete required training, work with at least one other person in the lab, and follow equipment and fabrication access rules. This device has no battery, high voltage or intended body-current interface.

Sources: USB [16], NXP NFC interface data [9] [10], IEC public scope [33], FCC RF rulemaking [34] and course safety guidance [35].

Bench and demonstration procedure

Table 33. Operational hazard controls

Stage	Required action
Before power	Inspect polarity, solder bridges, connector orientation and insulated mounting. Confirm U6 tab clearance, motor voltage, Hall pin order and no SWD power backfeed. Fit guards and secure magnets.
First energization	Use a current-limited bench source with branches disabled. Check rails and unexpected current, then qualify one reader and one motor before three-slot operation. Do not connect a laptop until power-path checks pass.
Motion and fault tests	Keep fingers, hair and loose items clear. Use a nonconductive test obstruction under low current. Disconnect power before clearing a jam; inspect for loose parts and explicitly rehome.
Thermal or power fault	Stop for odor, discoloration, excessive temperature, repeated resets or latched faults. Remove source power and investigate; do not increase limits to hide a failure.
Demonstration	Explain the validity indicator and stale-page behavior, verify supply permission, place the dock on a stable surface, and keep an accessible USB disconnect. Do not use it for safety-critical decisions.

Risks added since the proposal include the selected LDO thermal constraint, Darlington motor losses, independent reader reset bias, pin-order mismatches and a retained stale mechanical page after power loss. The tests in S4–S7 are the acceptance evidence for these mitigations.

5 References

Online documents were consulted on October 2, 2026 unless a saved price observation carries another date. Local project evidence is frozen under sources/local and indexed with SHA-256 hashes.

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Appendix A Complete costed BOM

Quantities cover one mainboard, three Hall probes and all external parts. Unit use is rounded per line. Purchase cost buys full stated packs; fabrication uses quoted or assumed batches. Exact quote links, dates, reference designators and limitations are in the matching workbook rows.

ID	Part number and description	Manufacturer	Use / pack	Unit \$	Use cost	Buy cost
E01	SN74LVC125AD SOIC-14	Texas Instruments	1 / 1	\$1.110	\$1.11	\$1.11
E02	USB4085-GF-A GCT USB4085-GF-A	GCT	1 / 1	\$0.910	\$0.91	\$0.91
E03	61300511121 Würth 61300511121, 1x5, 2.54 mm vertical male header	Würth Elektronik	1 / 1	\$0.250	\$0.25	\$0.25
E04	LDL1117S33R 3.3 V LDO / SOT-223	STMicroelectronics	1 / 1	\$0.410	\$0.41	\$0.41
E05	TPS2553DBVR-1 Motor current-limited switch / SOT-23-6	Texas Instruments	1 / 1	\$1.060	\$1.06	\$1.06
E06	TPS22918DBVT NFC load switch / SOT-23-6	Texas Instruments	1 / 1	\$1.260	\$1.26	\$1.26
E07	TPD2E2U06DRLR ESD arrays / SOT-553	Texas Instruments	4 / 1	\$0.990	\$3.96	\$3.96
E08	SMF6.0A-T13 VBUS TVS / SOD-123F	Littelfuse	1 / 1	\$0.530	\$0.53	\$0.53
E09	EEE-FK1A221P 220 uF 10 V SMD aluminum capacitor	Panasonic	1 / 1	\$0.930	\$0.93	\$0.93
E10	61300611121 Würth 61300611121, 1x6, 2.54 mm vertical male header	Würth Elektronik	3 / 1	\$0.330	\$0.99	\$0.99
E11	61300811121 Würth 61300811121, 1x8, 2.54 mm vertical male header	Würth Elektronik	3 / 1	\$0.380	\$1.14	\$1.14
E12	61300311121 Würth 61300311121, 1x3, 2.54 mm vertical male header	Würth Elektronik	6 / 1	\$0.130	\$0.78	\$0.78
E13	LTST-C170KGKT , green 0805 LED	Lite-On	4 / 1	\$0.190	\$0.76	\$0.76
E14	C0805C104K3RACTU 100 nF, 25 V X7R, 0805 bypass	KEMET	16 / 1	\$0.090	\$1.44	\$1.44

Complete BOM continued

ID	Part number and description	Manufacturer	Use / pack	Unit \$	Use cost	Buy cost
E15	C0805C475J3RACTU 4.7 uF, 25 V X7R, 0805	KEMET	1 / 1	\$1.090	\$1.09	\$1.09
E16	C0805C105K3RACTU 1 uF, 25 V X7R, 0805 analog bypass	KEMET	6 / 1	\$0.190	\$1.14	\$1.14
E17	RC0805FR-0710KL 10k, 1%, 1/8 W, 0805 reset/boot resistors	Yageo	6 / 1	\$0.100	\$0.60	\$0.60
E18	RC0805FR-07100KL 100k, 1%, 1/8 W, 0805 pull-downs	Yageo	22 / 1	\$0.036	\$0.79	\$0.79
E19	TPS259630DDAR Input eFuse / SO-PowerPAD-8	Texas Instruments	1 / 1	\$0.950	\$0.95	\$0.95
E20	RC0805FR-074K7L 4.7k, 1%, 1/8 W, 0805 Hall pull-ups	Yageo	3 / 1	\$0.100	\$0.30	\$0.30
E21	RC0805FR-07220RL 220 ohm, 1%, 1/8 W, 0805 Hall series	Yageo	3 / 1	\$0.100	\$0.30	\$0.30
E22	RC0805FR-071KL 1k, 1%, 1/8 W, 0805 LED resistors	Yageo	5 / 1	\$0.100	\$0.50	\$0.50
E23	61300211121 Würth 61300211121, 1x2, 2.54 mm vertical male header	Würth Elektronik	1 / 1	\$0.130	\$0.13	\$0.13
E24	RC0805FR-07249KL 249k 1% / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E25	RC0805FR-07374KL 374k 1% / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E26	RC0805FR-07464RL 464R 1% / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E27	C0805C224K3RACTU 220nF 25V X7R / C_0805_2012Metric	KEMET	1 / 1	\$0.240	\$0.24	\$0.24
E28	GRM31CR71C106KAC7L 10uF 16V X7R / C_1206_3216Metric	Murata	2 / 1	\$0.990	\$1.98	\$1.98

Complete BOM continued

ID	Part number and description	Manufacturer	Use / pack	Unit \$	Use cost	Buy cost
E29	GRM32ER61C226KE20L 22uF 16V X5R / C_1210_3225Metric	Murata	1 / 1	\$1.880	\$1.88	\$1.88
E30	RC0805FR-0726K1L 26.1k 1% / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E31	RC0805FR-07100RL 100R / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E32	C0805C472J5GACTU 4.7nF 25V COG / C_0805_2012Metric	KEMET	1 / 1	\$0.800	\$0.80	\$0.80
E33	SN74LVC1G17DBVT SN74LVC1G17DBVT / SOT-23-5	Texas Instruments	1 / 1	\$0.900	\$0.90	\$0.90
E34	RC0805FR-0747KL 47k 1% / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E35	RC0805FR-07150KL 150k 1% / R_0805_2012Metric	Yageo	1 / 1	\$0.100	\$0.10	\$0.10
E36	C0805C102J5GACTU 1nF COG / C_0805_2012Metric	KEMET	1 / 1	\$0.170	\$0.17	\$0.17
E37	LM74700QDBVTQ1 LM74700QDBVTQ1 / SOT-23-6	Texas Instruments	1 / 1	\$2.580	\$2.58	\$2.58
E38	AO3404A AO3404A / SOT-23	Alpha and Omega Semiconductor	1 / 1	\$0.500	\$0.50	\$0.50
E39	STM32G431RBT6 Main MCU LQFP64	STMicroelectronics	1 / 1	\$7.080	\$7.08	\$7.08
E40	RC522 / Amazon B07VLDSYRW Three RC522 reader modules	HiLetgo	3 / 3	\$3.330	\$9.99	\$9.99
E41	DRV5023AJELPGMQ1 Unipolar Hall sensor TO92	Texas Instruments	3 / 1	\$0.560	\$1.68	\$1.68
E42	TL1105AF100Q Reset tactile switch	E-Switch	1 / 1	\$0.350	\$0.35	\$0.35

Complete BOM continued

ID	Part number and description	Manufacturer	Use / pack	Unit \$	Use cost	Buy cost
E43	HLMP3301 External validity indicator red 5 mm	Everlight	1 / 1	\$0.250	\$0.25	\$0.25
M01	28BYJ-48 + ULN2003 kit 5 V motors with ULN2003 driver boards	ELEGOO	3 / 5	\$2.798	\$8.39	\$13.99
M02	9098 Diametric magnet 3 x 2.5 mm	Radial Magnets	3 / 1	\$0.400	\$1.20	\$1.20
M03	NTAG215 25 mm white wet inlay	GoToTags / NXP chip	3 / 10	\$0.410	\$1.23	\$4.10
M04	793 Female female 300 mm jumper conductors	Adafruit	58 / 40	\$0.199	\$11.53	\$15.90
M05	USB2 C-C 3 A data cable USB C to C data cable 1 m rated at least 3 A	Supplier to select	1 / 1	\$10.000	\$10.00	\$10.00
M06	M3 mounting set M3 board standoffs and screws four positions	Supplier to select	1 / 1	\$4.000	\$4.00	\$4.00
M07	Mechanical hardware allowance Shaft pins hinges screws and retainers for 3 mechanisms	Supplier to select	1 / 1	\$12.000	\$12.00	\$12.00
M08	Assembly consumables allowance Wire insulation strain relief adhesive and legends	Supplier to select	1 / 1	\$6.000	\$6.00	\$6.00
F01	v0.1.0 mainboard Four-layer 60 x 100 mm mainboard	PCBWay	1 / 10	\$5.593	\$5.59	\$55.93
F02	v0.1.0 Hall probe Two-layer 12 x 18 mm Hall probe boards	PCBWay	3 / 10	\$0.500	\$1.50	\$5.00
D01	NUCLEO-G431KB Nucleo development board	STMicroelectronics	1 / 1	\$20.130	\$20.13	\$20.13

Printing uses an existing school printer: \$14.02 of filament is consumed and \$48.98 buys the selected whole packages. This covers three mechanisms, one enclosure and three tag housings. PCB freight is separate. The development board is equipment. DNP C12–C14, copper test pads and mounting holes have no discrete-part charge.

Appendix B Connectors and MCU pins

Physical left, center and right slots use wire IDs 0, 1 and 2. Schematic motor/NFC/Hall groups 1, 2 and 3 correspond to those IDs in order. The following connector order is physical pad-number order. Continuity-check and label every harness before power; the reader module order differs from the mainboard header, so a straight ribbon is not a valid wiring assumption.

Table 34. Mainboard connector map

Connector	Pin order and destination
J1 SWD	1 3V3 reference; 2 SWDIO; 3 SWCLK; 4 GND; 5 NRST. Custom header; do not assume standard Cortex cable order or debugger power injection.
J3 / J4 / J5 motor	1 IN1; 2 IN2; 3 IN3; 4 IN4; 5 switched 5V_MOTOR; 6 GND. Connect to external ULN2003 board; motor five-wire connector stays on that board.
J6 / J7 / J8 NFC	1 switched 3V3_NFC; 2 GND; 3 SCK; 4 MOSI; 5 raw MISO; 6 CS_N; 7 RST_N; 8 IRQ_N. Typical module printed order: SDA, SCK, MOSI, MISO, IRQ, GND, RST, 3.3V.
J9 / J10 / J11 Hall	1 3V3_LOGIC; 2 GND; 3 HALL_RAW. Remote sensor TO92 pin 1 VCC, 2 GND, 3 OUT. Probe includes local 100 nF bypass.
J12 panel validity	1 VALID_LED_A; 2 GND. Series resistor is on mainboard; verify the external LED polarity.
Test pads	TP1 VBUS_RAW; TP2 GND; TP3 3V3_LOGIC; TP4 GND; TP5 5V_MOTOR; TP6 NRST. Copper features, not purchased discrete parts.

The harness budget includes 18 motor, 24 NFC, 9 Hall, 2 LED and 5 SWD conductors, or 58 female-to-female conductors. The 300 mm jumper product is a prototyping price reference; its 28 AWG conductors and individual contacts require voltage-drop and retention checks. Use a keyed, heavier motor-power pair if measurements require it and update the cost line.

USB and power connections

USB J2 A6/B6 connect D+ to PA12; A7/B7 connect D- to PA11. CC1 connects PA9/DBCC1 and PB6/UCPD_CC1; CC2 connects PA10/DBCC2 and PB4/UCPD_CC2. SBU contacts are unused. VDD pins 16/32/48/64, VBAT pin 1, VDDA pin 29 and VREF+ pin 28 use 3.3 V. Disable VREFBUF with this connection. VSS pins 15/31/47/63 and VSSA pin 27 use common ground.

MCU pins 1 through 32

Physical pin	Function	Net	Endpoints or purpose
1	VBAT	3V3_LOGIC	Common supply/ground; see schematic
2	PC13	NC	No connect
3	PC14	NC	No connect
4	PC15	NC	No connect
5	PF0	NC	No connect
6	PF1	NC	No connect
7	PG10	NRST	C11.1, J1.5, R1.2, SW1.1, TP6.1
8	PC0	M1_IN1	J3.1, R3.1
9	PC1	M1_IN2	J3.2, R4.1
10	PC2	M1_IN3	J3.3, R5.1
11	PC3	M1_IN4	J3.4, R6.1
12	PA0	HALL1_RESERVED	C12.1, R21.2
13	PA1	HALL2_RESERVED	C13.1, R22.2
14	PA2	HALL3_RESERVED	C14.1, R23.2
15	VSS	GND	Common supply/ground; see schematic
16	VDD	3V3_LOGIC	Common supply/ground; see schematic
17	PA3	VALID_LED_RESERVED	R34.1
18	PA4	QUAL_LED_RESERVED	R32.1
19	PA5	SPI1_SCK	J6.3, J7.3, J8.3
20	PA6	SPI1_MISO	U4.3, U4.6, U4.8
21	PA7	SPI1_MOSI	J6.4, J7.4, J8.4
22	PC4	M2_IN1	J4.1, R7.1
23	PC5	M2_IN2	J4.2, R8.1
24	PB0	NFC1_CS_N	J6.6, R15.2, U4.1
25	PB1	NFC2_CS_N	J7.6, R16.2, U4.4
26	PB2	NFC3_CS_N	J8.6, R17.2, U4.10
27	VSSA	GND	Common supply/ground; see schematic
28	VREF+	3V3_LOGIC	Common supply/ground; see schematic
29	VDDA	3V3_LOGIC	Common supply/ground; see schematic
30	PB10	NFC1_RST_N	J6.7, R24.1
31	VSS	GND	Common supply/ground; see schematic
32	VDD	3V3_LOGIC	Common supply/ground; see schematic

Pin names ending RESERVED are retained source identifiers. They do not mean that the current circuit is omitted. Exact schematic references and net connectivity remain authoritative for assembly.

MCU pins 33 through 64

Physical pin	Function	Net	Endpoints or purpose
33	PB11	NFC2_RST_N	J7.7, R25.1
34	PB12	NFC3_RST_N	J8.7, R26.1
35	PB13	NFC1_IRQ_N	J6.8
36	PB14	NFC2_IRQ_N	J7.8
37	PB15	NFC3_IRQ_N	J8.8
38	PC6	M2_IN3	J4.3, R9.1
39	PC7	M2_IN4	J4.4, R10.1
40	PC8	M3_IN1	J5.1, R11.1
41	PC9	M3_IN2	J5.2, R12.1
42	PA8	HEARTBEAT_RESERVED	R33.1
43	PA9	USB_CC1	J2.A5, U10.3
44	PA10	USB_CC2	J2.B5, U10.5
45	PA11	USB_D_N	J2.A7, J2.B7, U9.5
46	PA12	USB_D_P	J2.A6, J2.B6, U9.3
47	VSS	GND	Common supply/ground; see schematic
48	VDD	3V3_LOGIC	Common supply/ground; see schematic
49	PA13	SWDIO	J1.2
50	PA14	SWCLK	J1.3
51	PA15	VBUS_PRESENT	U13.4
52	PC10	M3_IN3	J5.3, R13.1
53	PC11	M3_IN4	J5.4, R14.1
54	PC12	NC	No connect
55	PD2	NC	No connect
56	PB3	NC	No connect
57	PB4	USB_CC2	J2.B5, U10.5
58	PB5	MOTOR_EN_RESERVED	R41.1, U7.3
59	PB6	USB_CC1	J2.A5, U10.3
60	PB7	POWER_FAULT_RESERVED	R40.2, U5.6, U7.4
61	PB8	BOOT0	R2.1
62	PB9	NFC_EN_RESERVED	R43.1, U8.3
63	VSS	GND	Common supply/ground; see schematic
64	VDD	3V3_LOGIC	Common supply/ground; see schematic

Pin names ending RESERVED are retained source identifiers. They do not mean that the current circuit is omitted. Exact schematic references and net connectivity remain authoritative for assembly.

Appendix C Current schematics

The figures below are native KiCad exports of the selected readable mainboard and Hall-probe sources. The mainboard overview is intended for topology review; use figures/mainboard_schematic.pdf at full zoom for small labels. The Hall design is repeated three times. These documents are review copies, not evidence of fabrication or physical acceptance.

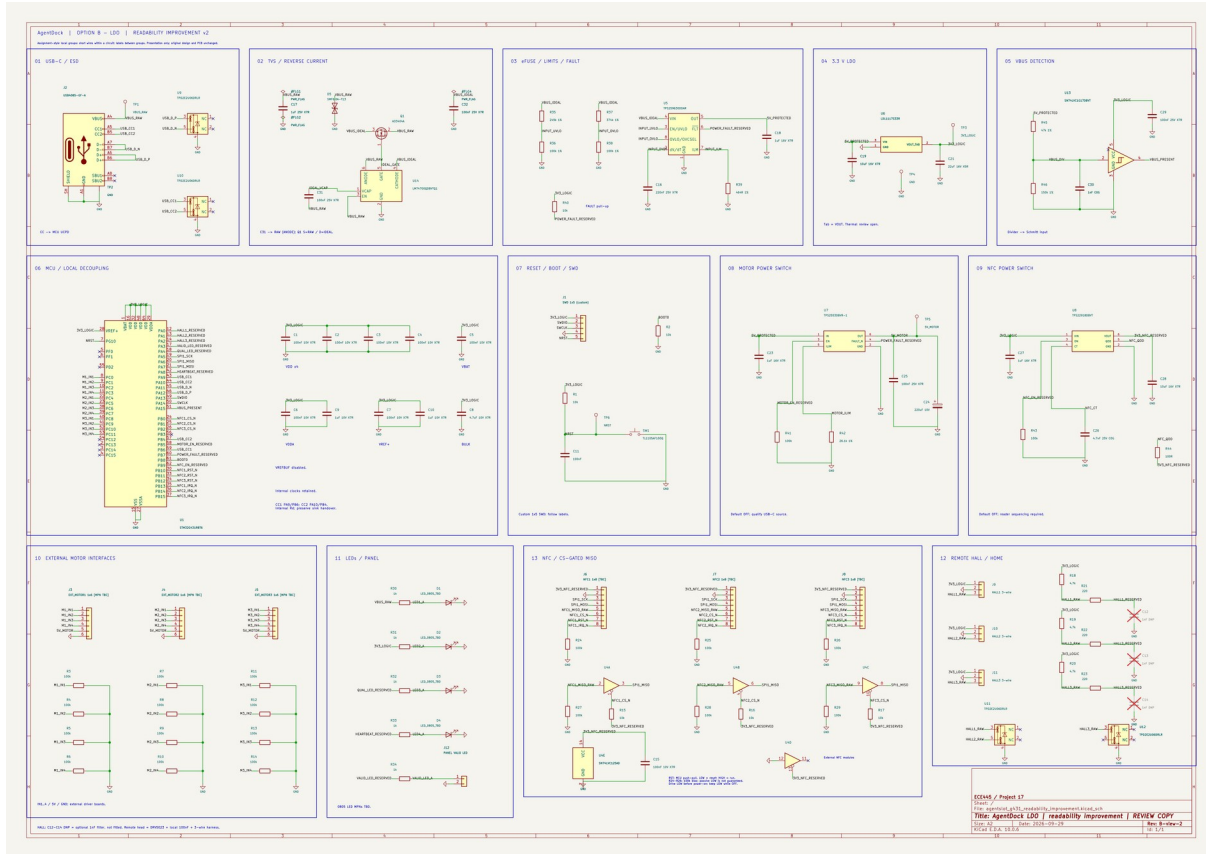


Figure 12. Complete mainboard overview. Full-resolution vector source: figures/mainboard_schematic.pdf.

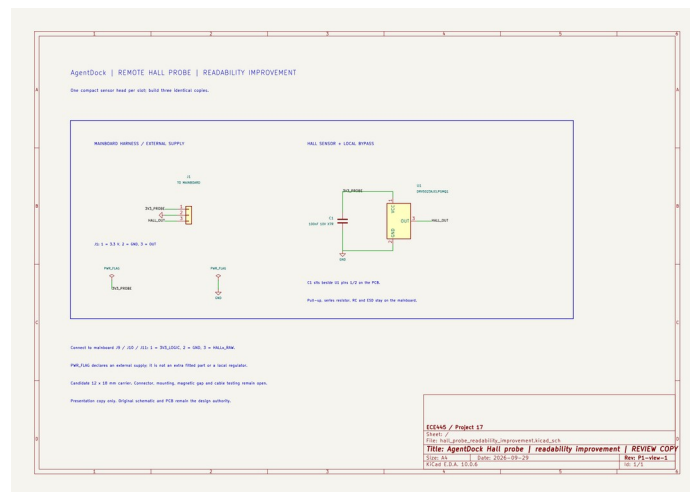


Figure 13. Remote Hall probe. Full-resolution vector source: figures/hall_probe_schematic.pdf.

Power circuit details from the native design

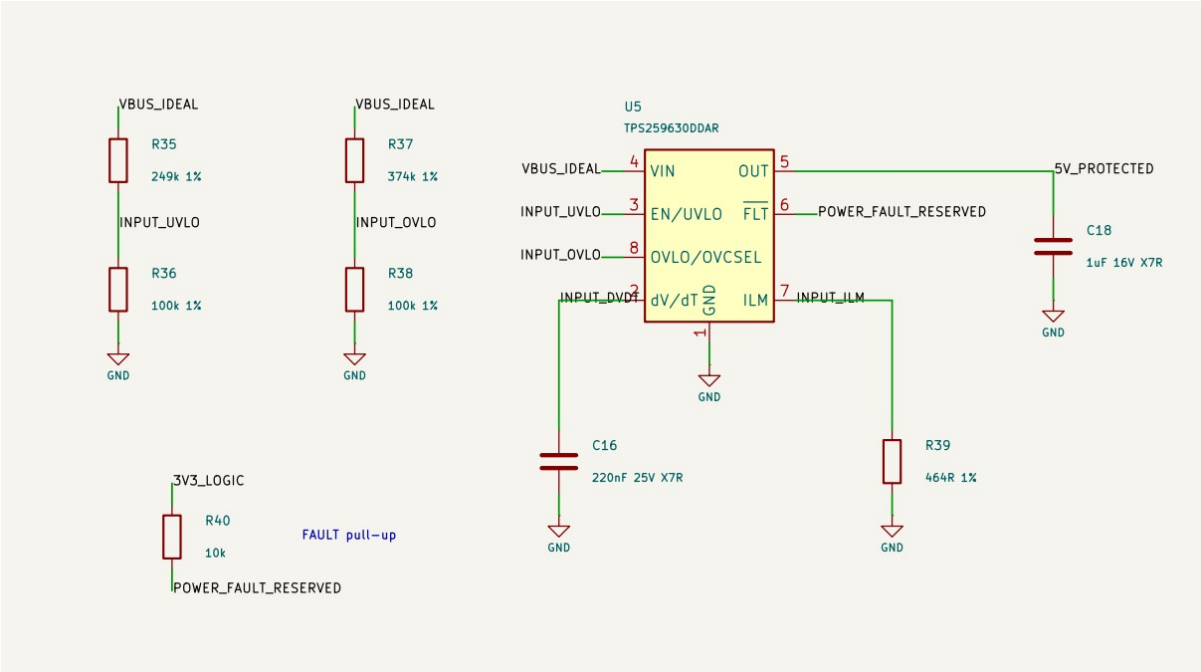


Figure 14. TPS259630 eFuse values and shared fault connection, cropped from the native mainboard export.

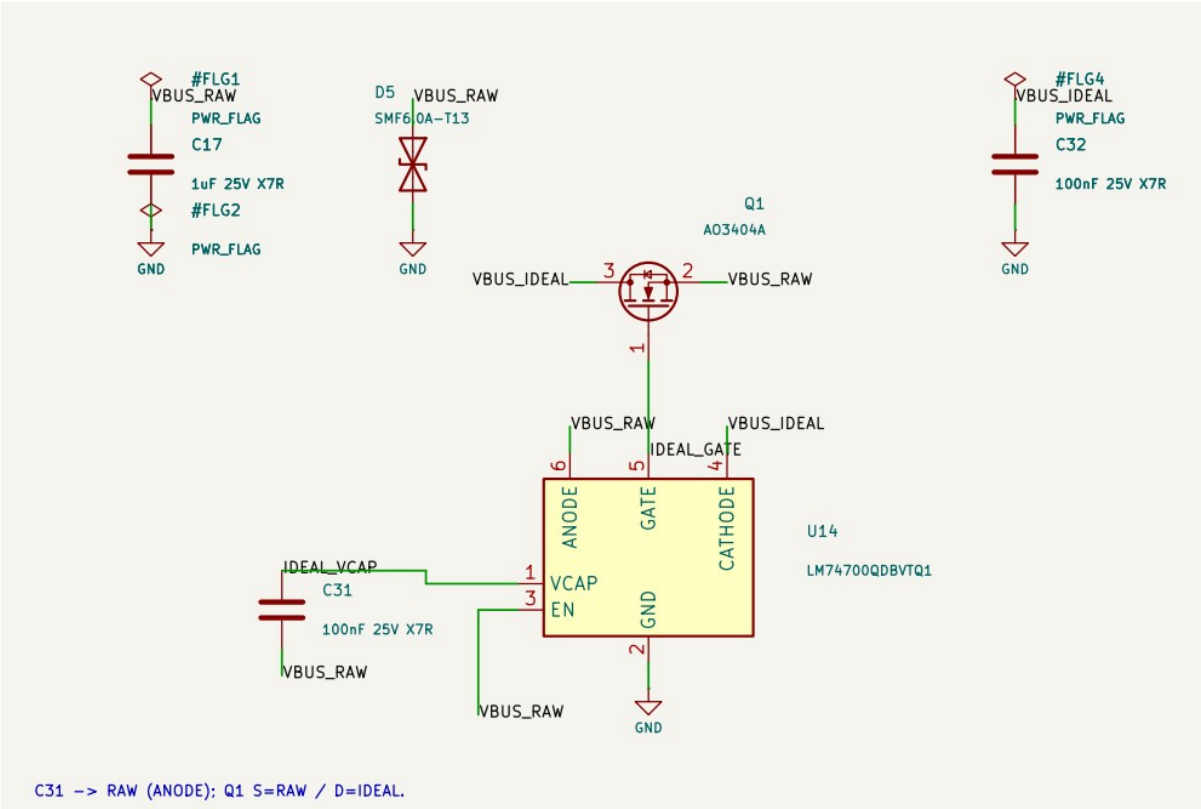


Figure 15. LM74700 and AO3404A reverse-blocking path, cropped from the native mainboard export.

The original net labels and values are preserved. Complete surrounding connections and test points remain in the full schematic PDF. S7 and the tolerance analysis state the current qualification limits.

Reader circuit details

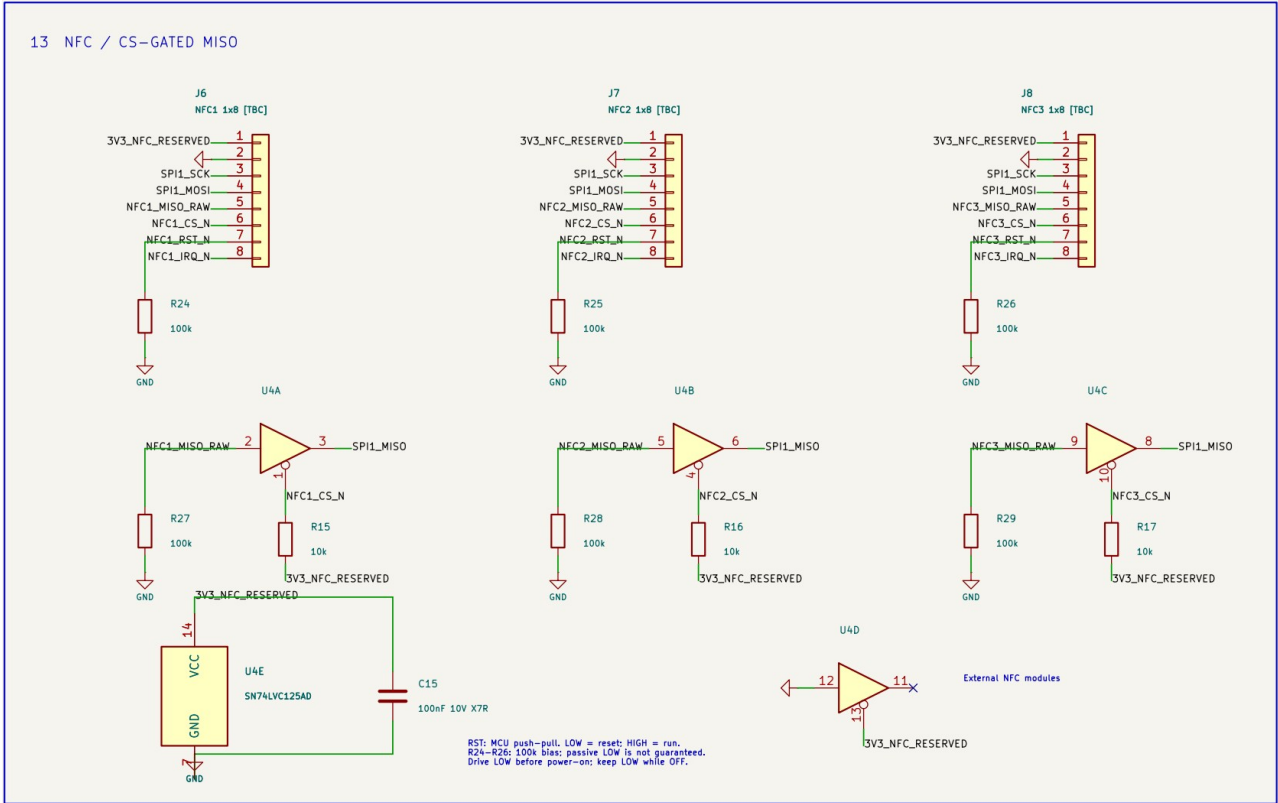


Figure 16. Three reader headers, separate RST pulldowns and CS-controlled MISO isolation. Native schematic detail.

Hall circuit detail

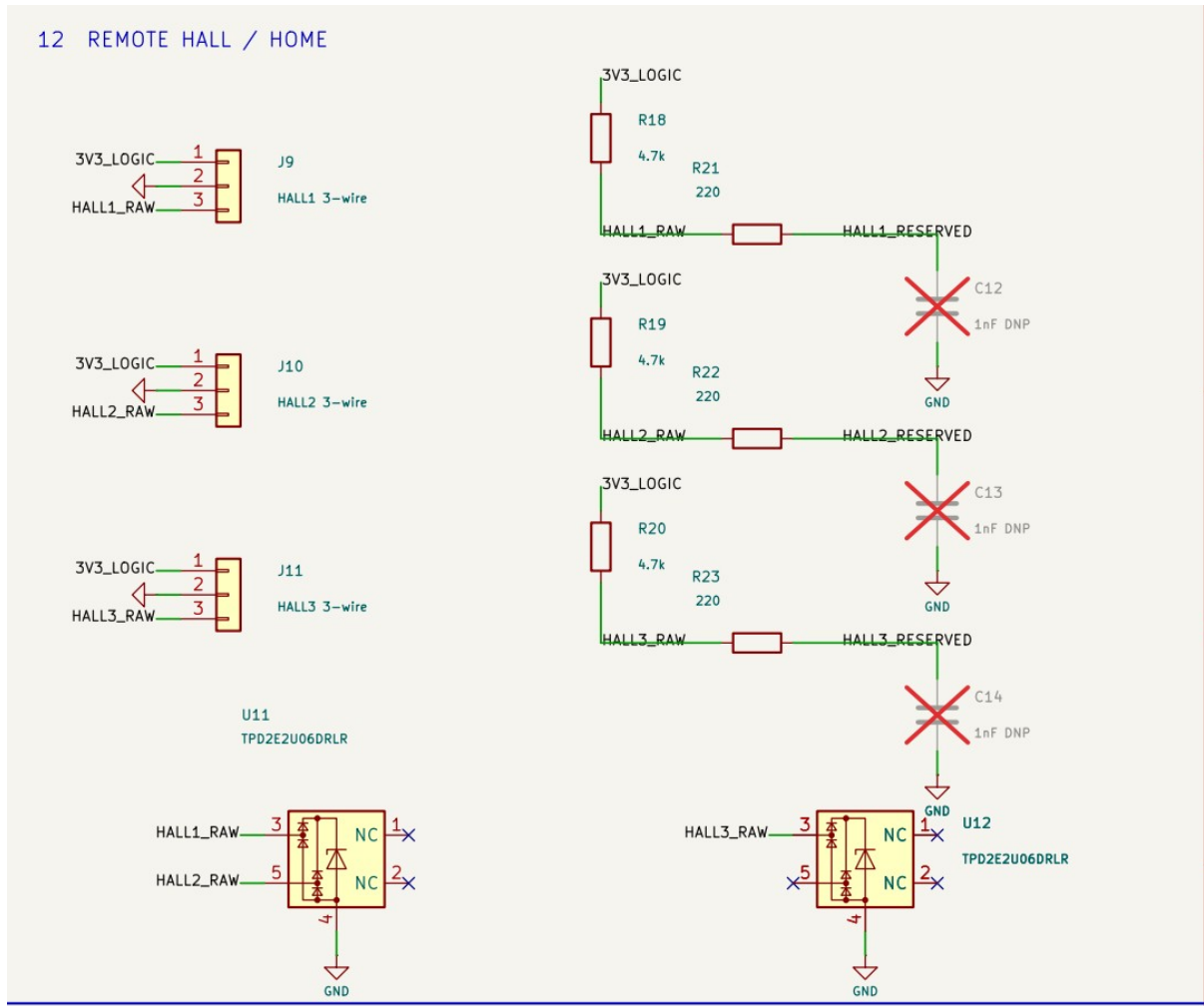


Figure 17. Mainboard Hall pullups, series resistors and DNP filters. Native schematic detail.

Probe construction: DRV5023AJELPGMQ1, one local 100 nF capacitor and one three-pin header per 12 × 18 mm board. Mainboard connector pin order must be followed exactly.

Appendix D Requirement traceability

Table 35. Requirement-to-evidence map

System objective or risk	Subsystem requirements	Acceptance evidence
H1 three-slot binding	S1-R1, S2-R1/R2, S4-R1, S5-R1/R5	600 physical insertion/removal events; zero wrong-slot assignments; old-command injection.
H2 response time	S1-R2/R3, S2-R2, S5-R2/R3, S6-R2/R3, S7-R2/R3	100 transitions per slot covering all ordered state pairs, with three simultaneous schedules and video.
H3 readability	S6-R1/R3; physical area and pitch checks	Each tester and distance passes $\geq 57/60$ under specified illumination/azimuth.
Cross-computer continuity	S2-R3, S3-R1/R2/R3, S4-R2	Ten round trips, authenticated project lookup, verified code/context IDs and exact card readback.
Disconnect and stale data	S1-R3/R4, S5-R1/R5	Heartbeat/source expiry, reconnect reconciliation and rejection of delayed old identities.
NFC write interruption	S3-R3, S4-R2/R3	Twenty interruption trials and 300 complete readback pairs.
Jam and home failure	S5-R4, S6-R2/R4/R5	Bounded home travel/time, safe invalid state, controlled recovery.
Power abnormalities	S7-R1 through R5	Grant, rail, thermal, overload, reverse-current and back-power measurements.

Test record format and acceptance

Every physical trial record must include date, operator, hardware/firmware/host revision, fixture and calibration, ambient conditions, commanded slot and state, measured result, pass/fail and linked raw log/video. Preserve failed trials; rerun a corrected design as a new version rather than deleting failures. The detailed requirement rows are also exported to data/requirements_traceability.csv.

Before final demonstration, the team must close source-current permission, actual LDO load and temperature, loaded motion rate, Hall geometry, adjacent-reader reliability, serial firmware and native-platform observation. The current host and PCB check records remain supporting evidence within their own scope. No physical result has been invented to fill these open items.