

Rider-Adaptive Automatic Bicycle Mirror

ECE 445 Design Document

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Team 53

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Design overview

A button-activated, two-axis bicycle mirror estimates the rider's head position with a multizone time-of-flight (ToF) sensor and re-aims itself with closed-loop motor control. One VL53L5CX-SATEL module facing the rider is the only head-position sensor. A single STM32F103CBT6 on the custom PCB reads its 8×8 depth grid, applies a calibrated head-to-eye offset, computes the required mirror yaw and pitch, drives two geared DC motors through DRV8876 H-bridges and closes each axis loop with an AS5600 magnetic angle sensor. When the mirror reaches its target the motors are switched off and a mechanical holding stage keeps the position.

The hardware is defined by the MirrorPCB v0.2 KiCad schematic, PCB and BOM, submitted for fabrication on September 30, 2026 (schematic excerpts in Appendix D). This document describes that hardware, the firmware and mechanics built around it, the requirements each subsystem must meet and how each will be verified. Requirements are acceptance targets for upcoming tests; no measured results are reported yet.

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The example design document [2] informs the section organization and level of subsystem detail. Schematic figures are taken directly from the v0.2 KiCad schematic; all other diagrams are original project drawings.

1 Introduction

1.1 Problem and solution

A bicycle mirror only shows the intended rear region when it is aimed for the rider's current eye position. Leaning forward, sitting upright, changing seat height or sharing a bicycle moves that position and can push the chosen rear region out of view. Correcting the mirror by hand interrupts riding and is difficult for people with limited reach or dexterity. We address this alignment problem; we do not claim a measured reduction in crashes. Handlebar accessories must also preserve braking, steering and safe mechanical clearances; CPSC bicycle guidance is used as a design reference [3].

Existing solutions do not address this. Bar-end and helmet mirrors are fixed or hand-adjusted, so every posture change needs a manual correction. Automotive memory mirrors restore positions stored for each driver, but they do not measure where the driver's head actually is; a new posture still needs a manual adjustment and a new stored setting. Our device measures the rider's head position at the moment of each request and computes the mirror angle from that measurement, so it adapts to postures it has not seen before.

Our solution is a button-activated mirror with motorized yaw and pitch. A VL53L5CX depth module facing the rider measures a coarse 8×8 depth grid of the head region. The STM32F103CBT6 estimates the head position from several neighboring zones, adds a rider-specific calibrated head-to-eye offset, computes the mirror normal for a fixed rear target and drives two geared DC motors. AS5600 sensors measure the actual mirror axis angles. Compared with the Raspberry Pi and camera arrangement in our proposal [1], the design removes the single-board computer, the RGB camera and the 5 V computer supply. This reduces assemblies and power demand at the cost of localization detail: a depth grid does not see the eyes, so the system relies on rider calibration and rejects uncertain measurements.

1.2 Visual aid

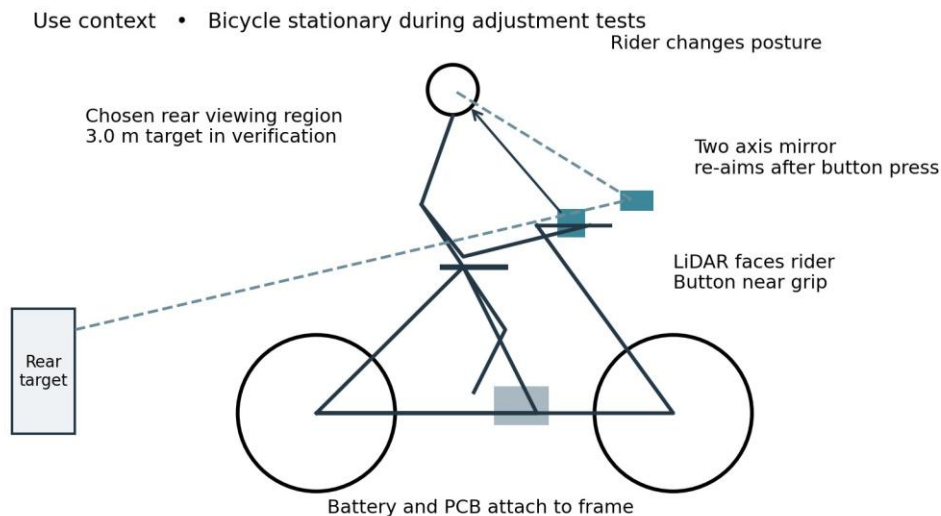


Figure 1. Rider, bicycle, sensor and rear target in use. Dashed lines show the viewing path, not electrical connections.

1.3 High-level requirements

- **HL1:** With the system initialized and a calibrated rider in the validated sensing envelope, each button press shall complete both-axis adjustment within 3.0 s; measured yaw and pitch shall remain within $\pm 1.0^\circ$ of their computed targets for at least 200 ms before the motors are disabled.

- **HL2:** For three calibrated normal rider postures spanning at least 20 cm of forward-to-backward head displacement, a fixed 40 mm diameter verification target 3.0 m behind the mirror shall be fully visible in at least 9 of 10 trials at each posture, observed through a verification camera placed at the measured eye midpoint.
- **HL3:** The battery-powered assembly shall complete 60 min of testing with one adjustment per minute without a controller reset or rail limit violation; afterwards it shall withstand 20 full steering sweeps without mount loosening or contact with brake controls, cables or the rider.
- **HL4:** A stale or invalid sensing result, feedback failure, motor driver fault, travel limit violation or software timeout shall disable both motor outputs within 100 ms of detection, and restart or power loss shall not cause uncommanded motion.

Operating envelope

Initial demonstration conditions are a stationary bicycle, dry indoor lighting, a forward-facing calibrated rider, a sensor-to-face distance of 0.4 to 1.2 m and an eye-to-mirror distance of 0.55 to 0.75 m. Sensor distance and eye-to-mirror distance are separate quantities because the sensor and mirror are mounted at different places on the handlebar; the three test postures must satisfy both envelopes. Angles of incidence at the mirror are limited to 25° for the tolerance calculation. Outdoor, wet, night-time and moving-bicycle performance are outside the demonstrated scope.

The requirements keep the proposal's 3 s adjustment, $\pm 1^\circ$ settling, 3 m target and 60 min runtime [1]. HL4 makes fault behavior an explicit acceptance criterion. The proposal's camera-based eye-detection requirement is replaced by a calibrated head-position accuracy requirement (S2) suited to a depth sensor.

2 Design

2.1 Block diagram and changes since the proposal

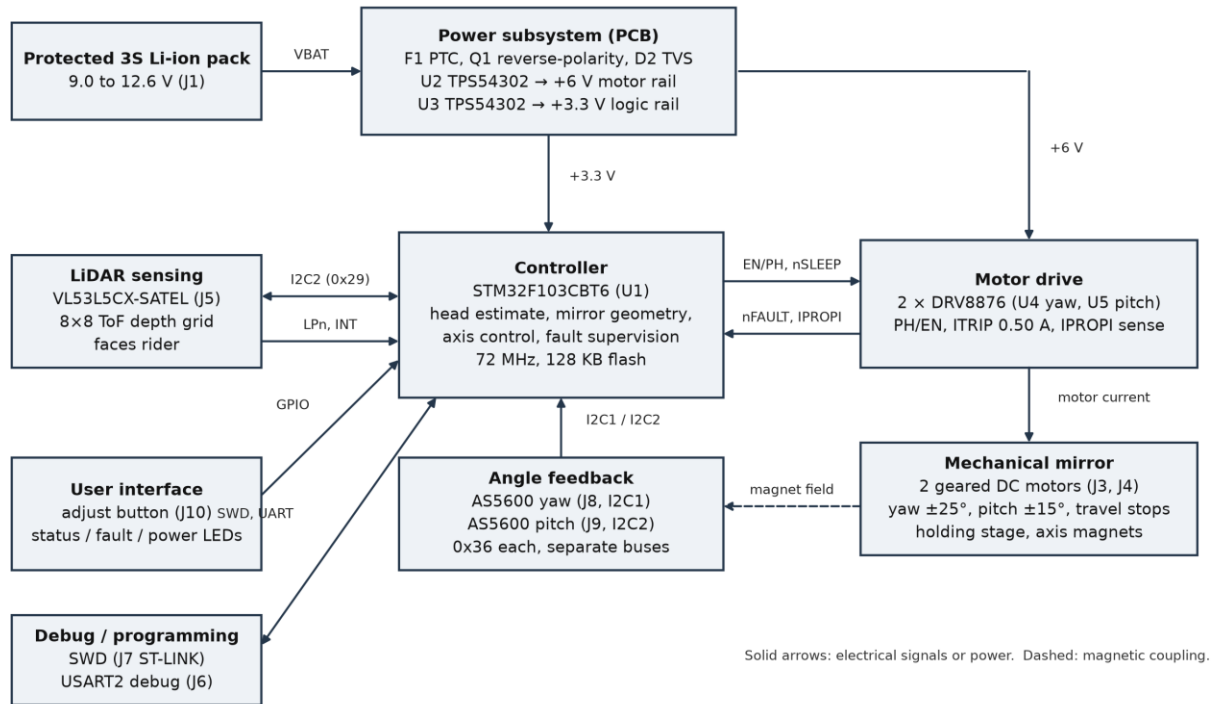


Figure 2. System block diagram. Each block can be verified independently before integration.

The LiDAR block measures the rider’s head region; the controller turns that measurement into a mirror orientation and supervises safety. The motor drive and angle feedback blocks close one position loop per axis, while the mechanical assembly sets the travel limits and holds the mirror without sustained motor current. The power block converts battery energy into a 6 V motor rail and a 3.3 V logic and sensor rail. The user interface provides deliberate activation and fault indication; the debug block is used for programming and bench testing.

Table 1. Changes from the proposal baseline.

Proposal baseline [1]	v0.2 design
Raspberry Pi 5 and RGB camera	Removed. The VL53L5CX depth grid is processed directly on the STM32; there is no camera or Pi connector on the board.
STM32G474RET6 (LQFP-64)	STM32F103CBT6 (LQFP-48): same package and pin-out as the STM32F103C8T6 used in the course soldering and CAD assignment, with 128 KB of flash for the VL53L5CX driver and firmware image.
5 V Pi buck and 3.3 V LDO	Removed. A second TPS54302 (U3) produces +3.3 V directly from the battery; U2 produces +6 V for the motors.
Pi-to-STM32 UART link	Replaced by the VL53L5CX header J5 (I2C2 plus LPn and INT). J6 remains a debug UART.
Two DRV8876 and two AS5600	Kept: U4/U5 in PH/EN mode with a 0.50 A current limit; AS5600 modules on J8 (I2C1) and J9 (I2C2).

2.2 Physical design

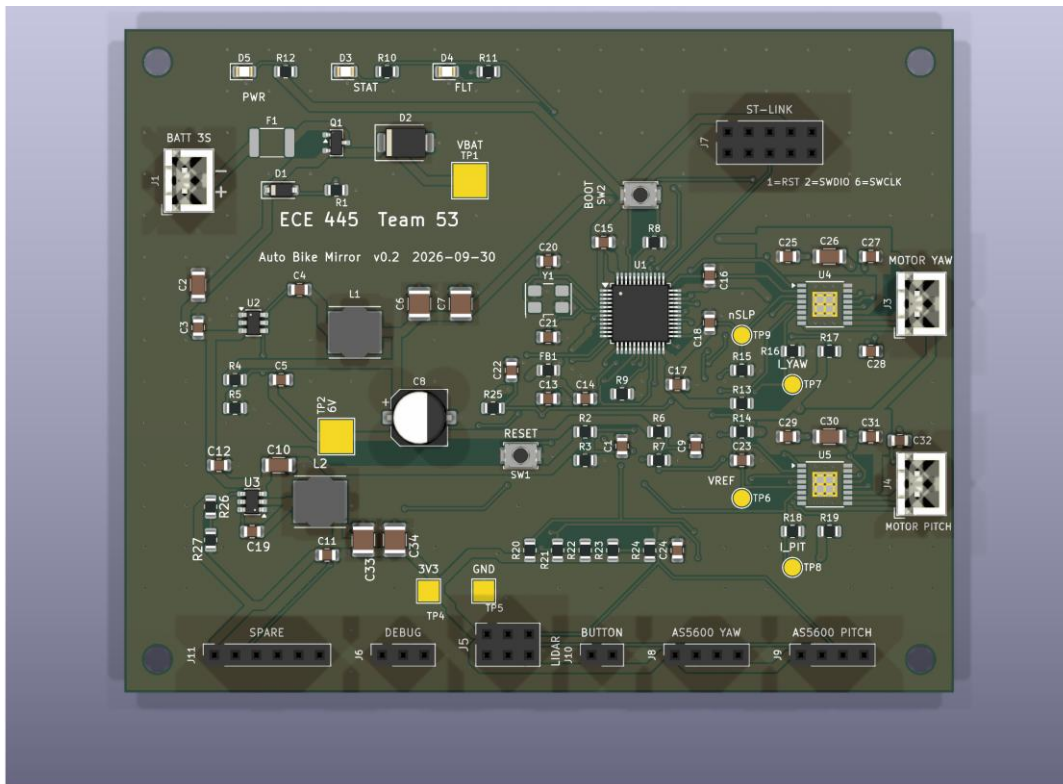
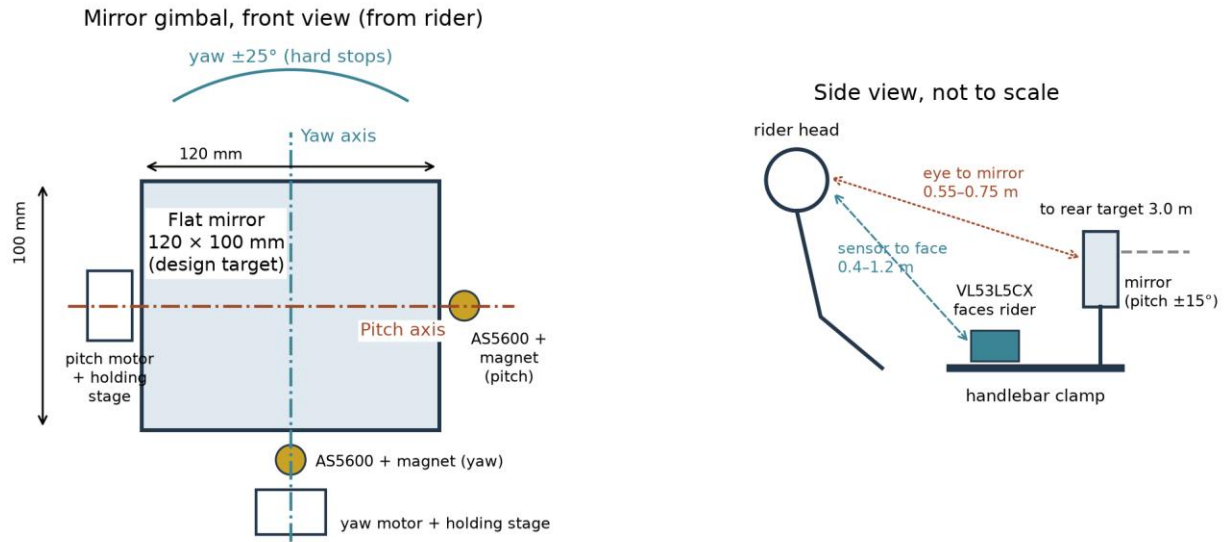


Figure 3. MirrorPCB v0.2, top view rendered from the final KiCad board file. Power input and protection are at the upper left, the two bucks at the left, the MCU in the center, the motor drivers at the right and all off-board sensor and interface headers along the bottom edge.

The PCB is a two-layer FR4 board, 100.0 × 80.0 mm and 1.6 mm thick, with 35 μm (1 oz) copper and ground pours on both layers. Four M3 mounting holes (3.2 mm, H1–H4) sit 4 mm in from each corner. Power traces are at least 1.0 mm wide wherever the pads allow; the DRV8876 exposed pads connect solidly to the ground pour through thermal vias. The final board passes KiCad DRC with no errors, warnings or unconnected items and passes the JLCDFM manufacturability check with no danger-level findings. A 3D-printed enclosure base and lid (105.5 × 85.5 mm footprint) was generated from the board outline and connector positions; it holds the PCB on M3 standoffs and leaves openings for the JST battery and motor connectors and the header row.



Mechanism dimensions are design targets; the gimbal CAD is not finalized.

Figure 4. Mirror mechanism and mounting geometry (design targets).

The planned 120 × 100 mm flat mirror pivots about its center on orthogonal yaw (vertical) and pitch (horizontal) axes. Each axis is driven by a Pololu 100:1 micro metal gearmotor through a secondary 20:1 holding stage, with a diametrically magnetized magnet on the output axis read by an AS5600. Hard stops limit travel to $\pm 25^\circ$ yaw and $\pm 15^\circ$ pitch. The VL53L5CX module mounts near the handlebar center facing the rider; the mirror assembly is offset toward one grip. The handlebar clamp is sized to the measured bar diameter of the test bicycle. Cables have service loops and strain relief, gear meshes are guarded, and the mirror edges are covered. The gimbal CAD is not finalized, so the mechanism dimensions above are design targets; they will be replaced with measured values from the built assembly.

2.3 LiDAR sensing subsystem

This block contributes to HL1 and HL2 by estimating the rider's head position after an intentional button press. The VL53L5CX-SATEL module provides an 8×8 grid of distances over a 45° × 45° field of view (63° diagonal), not an image. At 8×8 resolution the maximum ranging rate is 15 Hz, so the design runs at 15 Hz and collects five fresh frames after each press [4], [5]. The sensor is initialized once at power-up and stays initialized while the device is powered; the 3 s response requirement starts from that ready state.

Electrical interface

J5 carries +3.3 V, LPn, SCL, INT, SDA and ground (Appendix A). SCL/SDA are the I2C2 bus (PB10/PB11) shared with the pitch AS5600 on J9. The VL53L5CX 7-bit address is 0x29 (0x52 in 8-bit notation) and the AS5600 uses 0x36, so the two devices share the bus without a multiplexer [5], [10]. I2C2 runs at 400 kHz, the STM32F103 fast-mode limit. LPn (PA9) is driven high to enable the sensor's I2C interface and INT (PA10, EXTI with internal pull-up) signals a new frame. R22/R23 (5.1 kΩ) pull SCL and SDA to 3.3 V. With an estimated 75 pF bus capacitance the rise time is $t_r \approx 0.8473RC = 324$ ns, slightly above the 300 ns fast-mode limit, so S4 measures it on the assembled cable harness. If the module's own pull-ups are fitted in parallel the effective resistance drops and the rise time improves; if the measured rise time is too long, R22/R23 are changed to 2.2 kΩ after checking each device's sink current.

Firmware configuration

The VL53L5CX ultra-lite driver (ULD) [5] stores the sensor firmware image (86,016 bytes) in the STM32's internal flash and uploads it over I2C during initialization. The ideal transfer time is $86,016 \times 9 / 400 \text{ kHz} \approx 1.94$ s, so start-up takes roughly 2–3 s before the device reports ready. To keep memory use low, the driver is built with only the outputs the algorithm uses: distance, target status and number of detected targets (signal per SPAD is kept for weighting). The other outputs (ambient, SPAD count, sigma, reflectance, motion indicator) are disabled with the ULD's VL53L5CX_DISABLE_* build options, which shrinks the result buffer and the driver's temporary buffer. Frames are processed as they arrive: each frame updates per-zone running sums and valid counts instead of storing five full 8×8 frames.

Head localization and calibration

- Initialize and configure the sensor once at start-up (8×8, 15 Hz), then leave it ranging-ready.
- On a button press, collect five fresh frames and reject zones with invalid target status, no target or a range outside 0.4–1.2 m.
- Map zone order to physical orientation using the ULD convention [5] and restrict processing to a calibrated head region of the grid.
- Separate the upper head cluster from torso returns and compute a weighted centroid over the valid neighboring zones using distance and signal per SPAD.
- Convert the centroid to a 3-D point $p = d \cdot r$ using the calibrated ray r of each zone, transform it into the bicycle frame and add the rider-specific head-to-eye offset: $E = R_{B_s} p + t_{B_s} + o_{eye}$.
- Average the five estimates; reject the batch if its coordinate spread exceeds 30 mm or the acquisition times out, and require a new press.

Zone rays are calibrated by moving a measured target through the field at 0.5, 0.8 and 1.1 m. R_{B_s} and t_{B_s} are the measured sensor mounting rotation and offset, and o_{eye} is measured per rider by comparing the head centroid with the eye midpoint located by the verification fixture. The sensor does not detect the eyes; the eye position is inferred from the head estimate and this calibrated offset. Glasses, hair, helmets, sunlight and head rotation can shift the head cluster, so uncertain estimates are rejected and the mirror does not move.

LiDAR requirements and verification

Table 2. LiDAR sensing requirements and verification.

Requirement	Verification
S1. Produce five fresh valid frames and a viewing-position estimate within 0.8 s of each ready-state button press in at least 9 of 10 trials per calibrated posture.	Equipment: logic analyzer on J10 pin 1 (ADJ_BTN) and J5 pin 4 (LIDAR_INT); timestamped debug log on J6 (USART2). 1. Power the board, let the sensor initialize at 8×8 / 15 Hz and wait for the ready message. 2. Seat the rider in posture 1 and press the button 10 times, at least 5 s apart. 3. For each press, measure the time from the button falling edge to the “estimate ready” log line and check that five distinct frame IDs were used. 4. Repeat steps 2–3 for postures 2 and 3. Pass if: at least 9 of 10 presses per posture finish within 0.8 s using five distinct frames. Record: table of latency per press; minimum, mean and maximum per posture.
S2. Viewing-position estimate error ≤ 20 mm in each direction perpendicular to the eye-to-mirror line and ≤ 30 mm along that line, at all three calibrated postures.	Equipment: surveyed 3-D jig with an eye-midpoint pointer (uncertainty ≤ 5 mm), tape measure, debug log. 1. Measure the mirror pivot M and the sensor mounting position in the bicycle frame. 2. For each posture, place the pointer at the rider’s eye midpoint and record the reference point E_{ref}. 3. Freeze the calibration and run 10 adjustment batches per posture, logging each estimate E_{est}. 4. Compute $E_{est} - E_{ref}$ and project it onto the eye-to-mirror direction e and the two directions perpendicular to it. Pass if: every accepted batch is within 20 mm in both perpendicular directions and 30 mm along e. Record: error table per batch, scatter plot per posture, number of rejected batches.
S3. Reject invalid status, out-of-range data, an ambiguous head cluster, a stale frame (>200 ms) or an acquisition timeout (0.8 s): no motion starts and motor outputs are disabled within 100 ms.	Equipment: fault-injection firmware build; logic analyzer on TP9 (MOTOR_nSLEEP) and on PA1 (J11 pin 2) used as a fault marker. 1. Start an adjustment with the motors connected and the mirror free to move. 2. Inject one fault (invalid status, out-of-range distance, ambiguous cluster, repeated frame ID, I2C bus held low, or no frame for 0.8 s); the firmware raises PA1 at the injection point. 3. Measure the time from the PA1 edge to TP9 going low and check the fault LED. 4. Repeat each fault type 5 times. Pass if: no motion starts, the fault LED lights and TP9 falls within 100 ms in every trial. Record: table of fault type $\times$ trial with the measured response time.
S4. Shared I2C2 rise time ≤ 300 ns at 400 kHz with the LiDAR and pitch encoder attached; zero unhandled communication failures over 100 adjustment cycles.	Equipment: oscilloscope (≥ 100 MHz) with I2C decoding; debug log. 1. Connect the VL53L5CX and pitch AS5600 with their final cables on J5 and J9. 2. Probe J5 pin 3 (SCL) and pin 5 (SDA) against pin 6 (GND). 3. Measure the 30%–70% rise time on 20 edges of each line. 4. Run 100 adjustment cycles while the pitch encoder is read at 50 Hz and count NACKs and timeouts in the log. Pass if: worst-case rise time ≤ 300 ns and zero unhandled failures. Record: scope capture of the worst edge, rise-time table, error count.
S5. Sensor initialization (firmware upload and configuration) completes within 5 s of power-on in 20 of 20 cold boots; a failed initialization latches a fault and never enables the motors.	Equipment: bench supply (10.8 V, 0.5 A limit) into J1, logic analyzer on J5 pin 2 (LPn) and TP9, debug log. 1. Leave the board unpowered for at least 10 s, then switch the supply on. 2. Measure the time from supply rise to the “sensor ready” log line. 3. Repeat steps 1–2 for 20 cold boots. 4. Remove the VL53L5CX module from J5 and power on once more. Pass if: all 20 boots reach ready within 5 s; with the module removed the fault LED lights, TP9 stays low and nothing moves. Record: table of the 20 start-up times; capture of the failure case.

Timing

Five frames at 15 Hz take about $5/15 = 0.333$ s when acquisition starts just after a frame boundary. With the trimmed output set, one frame read is a few hundred bytes; even a 1024-byte transfer takes only $1024 \times 9 / 400 \text{ kHz} \approx 23$ ms plus addressing overhead. Five transfers plus processing therefore fit inside the 0.8 s budget if the sensor read and the pitch-encoder reads on the same bus use bounded, scheduled transactions.

2.4 Controller and geometry subsystem

The STM32F103CBT6 handles sequencing, sensing, geometry, both angle loops and fault handling for HL1, HL2 and HL4. It has a 72 MHz Cortex-M3 core, 128 KB of internal flash and 20 KB of SRAM in an LQFP-48 package [6]. It has no floating-point unit, so the geometry runs in software floating point or fixed point and its time is measured (C1). The firmware is bare-metal with bounded I2C transfers and an independent watchdog.

Pin compatibility with the STM32F103C8T6

The STM32F103x8 and STM32F103xB share one datasheet and an identical LQFP-48 pin-out; they differ only in flash (64 KB vs. 128 KB) [6]. Every pin used on the v0.2 schematic was checked against that pin-out. Supplies, oscillator, reset, boot, SWD, both I2C ports, the TIM1/TIM2 PWM pins, ADC channels 6–9 and all GPIO functions below exist on the same pads of both parts, so the CB is a direct drop-in for the C8 footprint used in the course assignment. The supporting clock, reset and decoupling circuitry is shown in Figure 10 (Appendix D).

Table 3. STM32F103CBT6 pin assignment (v0.2 schematic).

Function	Net	Pin (pad)	Peripheral / note
Supply	+3.3V / +3.3VA / GND	VDD 24, 36, 48; VBAT 1; VDDA 9; VSS 23, 35, 47; VSSA 8	C15–C17 100 nF, C18 10 μ F; VDDA via FB1 with C13/C14
Oscillator	OSC_IN / OSC_OUT	PD0 5 / PD1 6	8 MHz crystal Y1, C20/C21 10 pF
Reset / boot	NRST / BOOT0 / BOOT1	NRST 7 / BOOT0 44 / PB2 20	R25, C22, SW1; R8 and R9 hold boot low
SWD	SWDIO / SWCLK	PA13 34 / PA14 37	J7 (ST-LINK header)
Yaw drive	YAW_EN / YAW_PH	PA0 10 / PA4 14	TIM2_CH1 PWM / GPIO
Pitch drive	PITCH_EN / PITCH_PH	PA8 29 / PA5 15	TIM1_CH1 PWM / GPIO
Driver sleep, faults	MOTOR_nSLEEP / YAW_nFAULT / PITCH_nFAULT	PB12 25 / PB8 45 / PA12 33	shared sleep with R15 pull-down; R17/R19 pull-ups
Current sense	YAW_IPROPI / PITCH_IPROPI	PA6 16 / PA7 17	ADC12_IN6 / IN7
Supply sense	VBAT_SENSE / V6_SENSE	PB0 18 / PB1 19	ADC12_IN8 / IN9
Yaw encoder	YAW_SCL / YAW_SDA	PB6 42 / PB7 43	I2C1
Pitch encoder + LiDAR	PITCH_SCL / PITCH_SDA	PB10 21 / PB11 22	I2C2
LiDAR control	LIDAR_LPN / LIDAR_INT	PA9 30 / PA10 31	GPIO out / EXTI
User interface	ADJ_BTN / LED_STATUS / LED_FAULT	PB13 26 / PB14 27 / PB15 28	GPIO
Debug UART	DBG_TX / DBG_RX	PA2 12 / PA3 13	USART2 on J6
Spare (J11)	SPARE_PA1 / PA15 / PB4 / PB5	11 / 38 / 40 / 41	PA15, PB4 need SWD-only debug mode

Because PA9/PA10 now serve the LiDAR, the ROM USART1 bootloader is not used; the board is programmed and debugged only through SWD on J7.

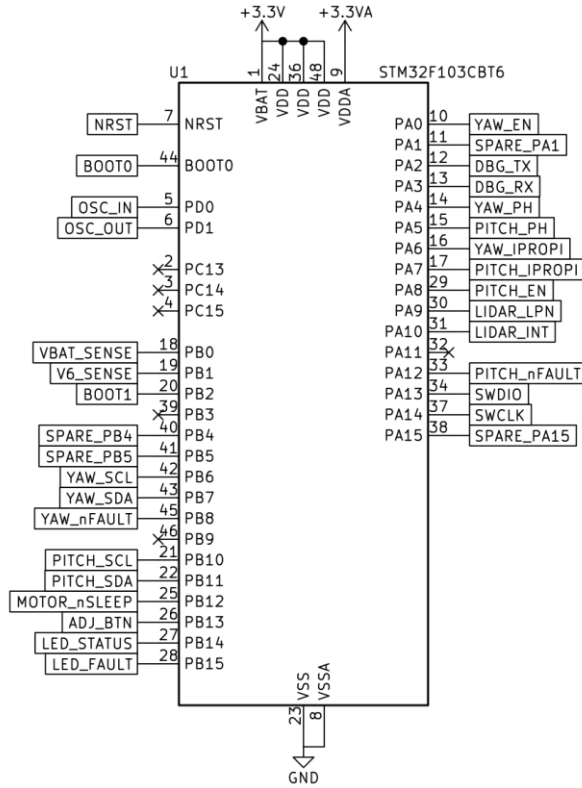


Figure 5. STM32F103CBT6 (U1) pin assignment from the v0.2 KiCad schematic.

Reflection calculation and reference frames

Bicycle coordinates are x rearward, y to the rider's left and z upward. The mirror pivot M , eye point E and target center T are measured in this frame. With the outward unit directions $e = (E - M)/\|E - M\|$ and $r = (T - M)/\|T - M\|$, the flat-mirror normal is

$$n = (e + r) / \|e + r\| \quad (1)$$

The physically reachable sign of n is selected, and the geometry is rejected when $\|e + r\| < 0.1$ or either direction vector is zero. For a mount whose normal is $n = [\cos(\text{pitch})\cos(\text{yaw}), \cos(\text{pitch})\sin(\text{yaw}), \sin(\text{pitch})]$, the commands are $\text{yaw} = \text{atan2}(n_y, n_x)$ and $\text{pitch} = \text{atan2}(n_z, \sqrt{n_x^2 + n_y^2})$. The measured mount rotation, encoder zeros and axis signs are applied before checking the $\pm 25^\circ$ and $\pm 15^\circ$ travel limits. Unreachable targets are rejected rather than clipped, since a clipped command would point the mirror in a misleading direction. If the built hinge order differs from this model, its fitted forward and inverse kinematics replace these equations.

Control and timing

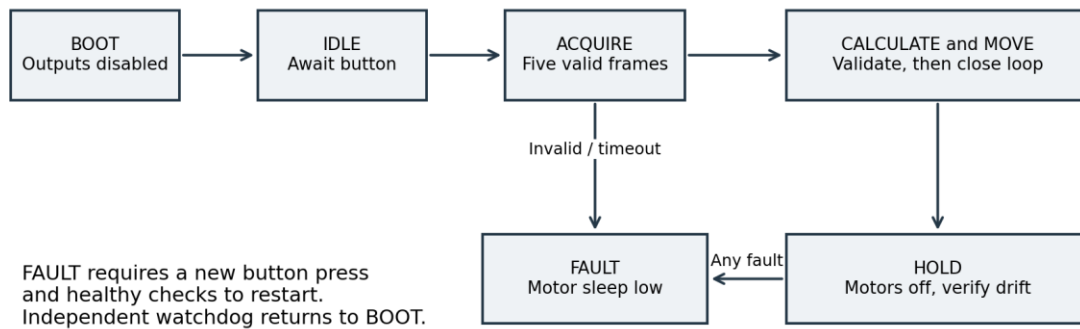


Figure 6. Firmware states. Every invalid state and every watchdog restart leads to disabled motor outputs.

Each axis is regulated at a nominal 100 Hz using the latest valid angle sample (polled at ≥ 50 Hz). The control law starts as proportional duty control on the wrapped angle error with a 0.3° deadband and 80% duty saturation; gain and minimum effective duty come from bench step responses. Integral action is added only if backlash and stiction measurements show it is needed. An axis is settled when both errors stay within 0.5° for 200 ms (M2), inside the $\pm 1.0^\circ$ HL1 limit; MOTOR_nSLEEP is then driven low. A 2.0 s movement timeout stops any move. The response budget is 0.8 s sensing + 0.05 s geometry + 2.0 s movement = 2.85 s, leaving 0.15 s of the 3.0 s HL1 limit.

Controller requirements and verification

Table 4. Controller requirements and verification.

Requirement	Verification
C1. Geometry and target validation complete within 50 ms; computed angles within 0.25° per axis of a double-precision reference.	Equipment: PC reference script (double precision), logic analyzer on PA1 (J11 pin 2), debug UART. 1. Generate 100 reachable eye points plus 5 singular and 5 out-of-travel cases on the PC. 2. Send each case to the firmware geometry routine over the debug UART. 3. Toggle PA1 around the calculation and measure its duration. 4. Compare the returned yaw and pitch with the reference values. Pass if: every reachable case finishes in ≤ 50 ms with $\leq 0.25^\circ$ error and every singular or out-of-travel case is rejected. Record: error histogram, maximum execution time, rejection table.
C2. Both motor outputs disabled ≤ 100 ms after an invalid sensor result, feedback older than 40 ms, nFAULT, a travel violation or a timeout; motors stay off through reset and power-up.	Equipment: 4-channel oscilloscope on TP9, J3 pin 1, J4 pin 1 and the PA1 fault marker. 1. Command a move on both axes. 2. Inject one fault: invalid sensor result, unplugged encoder (stale feedback), nFAULT pulled to GND through 1 k Ω , a target beyond travel, or a 2 s timeout. 3. Measure from the PA1 marker to TP9 low and to zero motor voltage. 4. Press RESET (SW1) during a move, halt the debugger during a move, and power-cycle the board 10 times. Pass if: outputs are disabled within 100 ms for every fault and no output pulse appears during reset or power-up. Record: scope capture per fault and a timing table.

Requirement	Verification
C3. Final firmware image ≤ 120 KB of the 128 KB flash (≥ 8 KB margin) and static SRAM plus peak stack ≤ 16 KB of 20 KB (≥ 4 KB margin); no stack overrun in 100 cycles.	Equipment: release build with linker map file, ST-LINK/V2 and debugger. 1. Build the release firmware including the VL53L5CX ULD and all features. 2. Read flash use (.text + .rodata + .data) and static RAM (.data + .bss) from the map file. 3. Fill the unused stack with a 0xA5 pattern at boot and run 100 adjustment cycles. 4. Read the stack high-water mark with the debugger. Pass if: flash ≤ 120 KB and static RAM plus peak stack ≤ 16 KB. Record: memory table with flash, RAM, stack and remaining margins.

The flash budget for C3 is dominated by the 86,016-byte (84 KB) ULD firmware image, which leaves about 44 KB for the ULD API, configuration tables and application code. The trimmed driver configuration keeps the main ULD RAM structures to a few kilobytes (offset and crosstalk buffers of 488 and 776 bytes plus a temporary buffer of about 1 KB) [5], well within 20 KB. These are expected values; C3 is checked on the compiled release build. A hardware driver fault shuts down its own H-bridge, but the shared MOTOR_nSLEEP line is otherwise MCU-controlled; R15 holds it low during reset and power-up. It is not a safety-rated emergency stop, so the battery disconnect stays within reach during testing.

2.5 Motor drive and angle feedback subsystem

This block contributes to HL1 by reaching the commanded yaw and pitch and to HL2 by holding the optical alignment. Each axis uses a Pololu #2367 100:1 micro metal gearmotor (6 V, 220 rpm no-load, 0.67 A theoretical stall current, 0.94 kg-cm theoretical stall torque [8]) driven by a DRV8876 H-bridge [9]. On both U4 and U5, PMODE is tied to ground to select PH/EN mode and IMODE is tied to ground to select the datasheet's fixed off-time current regulation mode. The EN pins receive 20 kHz PWM (TIM2_CH1 for yaw, TIM1_CH1 for pitch; ARR = 3599 at a 72 MHz timer clock) and the PH pins set direction. TIM1 is an advanced timer, so its main output enable must be set. PWM stays at zero and MOTOR_nSLEEP low until all start-up checks pass. Both nFAULT lines have 10 kΩ pull-ups (R17, R19) and are monitored even when only one axis moves.

Current limit and sensing

A shared reference $DRV_VREF = 3.3 \text{ V} \times 100 \text{ k} / (10 \text{ k} + 100 \text{ k}) = 3.0 \text{ V}$ is set by R13/R14 and filtered by C23. R16 and R18 (6.04 kΩ, 1%) convert each driver's IPROPI current ($A_IPROPI = 1000 \mu\text{A/A}$ [9]) to a voltage read by the ADC:

$$I_TRIP = V_REF / (A_IPROPI \cdot R_IPROPI) = 3.0 \text{ V} / (1000 \mu\text{A/A} \times 6.04 \text{ k}\Omega) \approx 0.50 \text{ A} \quad (2)$$

The 0.50 A limit is below the motor's 0.67 A stall current, and at the limit the IPROPI voltage is $6.04 \text{ V/A} \times 0.5 \text{ A} = 3.02 \text{ V}$, inside the 3.3 V ADC range. Current regulation protects the bridge, but a stalled motor would still sit at the limit, so firmware treats a sustained current near the limit with no angle progress as a stall and disables the axis. With both motors at the limit the 6 V rail carries about 1 A, well within its 2 A acceptance load. Each driver has 10 μF + 100 nF on VM, a 100 nF VCP capacitor and a 22 nF flying capacitor placed at the pins; C8 (100 μF) provides bulk storage on +6 V. The driver schematic is Figure 12 (Appendix D).

Angle sensors and mechanics

The yaw AS5600 connects to I2C1 through J8 and the pitch AS5600 to I2C2 through J9. Both have the fixed address 0x36, so they must stay on separate buses; only the pitch bus is shared with the LiDAR (0x29). R20–R23 (5.1 kΩ) are the bus pull-ups and are left unfitted if the AS5600 modules carry their own. The 12-bit output gives $360^\circ/4096 = 0.088^\circ$ resolution, which is not the same as accuracy [10]. Each magnet sits on the mirror axis after all reduction stages, magnet status is checked at start-up and the mounted encoder is calibrated against a reference protractor.

For a 150 g moving mirror with its center of mass 30 mm from the pitch axis, the gravity torque is $0.15 \times 9.81 \times 0.03 = 0.044 \text{ N}\cdot\text{m}$, and a 2× static margin requires 0.088 N·m. The motor's theoretical stall torque is about 0.092 N·m before the secondary stage; with 20:1 reduction and an assumed 30% stage efficiency this becomes about 0.55 N·m, which is not a continuous rating. The current limit reduces the available torque, so starting torque and friction are measured at 0.50 A and the mirror is counterbalanced if needed. The nominal output speed is $220/20 = 11 \text{ rpm} = 66^\circ/\text{s}$, so a 50° yaw traverse ideally takes 0.76 s; loaded speed and settling must still meet the 2.0 s movement budget. Holding is a tested property: a worm stage is not assumed to be self-locking, and M3 verifies drift with power removed. Physical stops back up the software limits.

Actuation requirements and verification

Table 5. Motor drive and angle feedback requirements and verification.

Requirement	Verification
M1. Each mounted angle channel updates at ≥ 50 Hz and, after calibration, agrees with an independent angle reference within $\pm 0.5^\circ$ across the required travel.	Equipment: digital inclinometer or protractor (uncertainty $\leq 0.2^\circ$), encoder log over J6. 1. Mount the mirror and zero both encoders at the mechanical center. 2. Step yaw from -25° to $+25^\circ$ in 5° steps, approaching each point from below and then from above. 3. At each point record the reference angle and the encoder angle, and the update interval from the log timestamps. 4. Repeat steps 2–3 for pitch from -15° to $+15^\circ$. 5. Store the per-axis calibration table, then repeat steps 2–4 with it applied. Pass if: calibrated error $\leq 0.5^\circ$ at every point and maximum update interval ≤ 20 ms. Record: error-versus-angle plot per axis (raw and calibrated) and the calibration table.
M2. Both axes settle within $\pm 0.5^\circ$ of target (encoder reading) for ≥ 200 ms within 2.0 s of the command across the full reachable travel.	Equipment: angle log at 100 Hz, oscilloscope, inclinometer. 1. Command 10 steps in each direction on each axis, including full-travel moves ($\pm 25^\circ$ yaw, $\pm 15^\circ$ pitch), and 10 combined two-axis moves. 2. Log both angles from the command until the motors stop. 3. Measure the time until the error stays within 0.5° for 200 ms and note the overshoot. 4. Check the final position with the inclinometer. Pass if: every move settles within 2.0 s with no collision and no sustained oscillation. Record: step-response plots and a settling-time / overshoot table.
M3. Unpowered drift $< 1.0^\circ$ on each axis for 60 s with the mirror installed.	Equipment: inclinometer and timer. 1. Move each axis to three positions (negative limit, center, positive limit). 2. Drive MOTOR_nSLEEP low and disconnect motor power. 3. Record the angle at 0, 10, 30 and 60 s. 4. Repeat with a light tap on the mirror frame at 5 s. Pass if: drift $< 1.0^\circ$ at 60 s in every case. Record: drift table per axis and position.
M4. Software limits and hard stops keep travel within $\pm 25^\circ$ yaw and $\pm 15^\circ$ pitch; all 10 out-of-range commands are rejected.	Equipment: debug UART, inclinometer; bicycle fixed and hands clear of the mechanism. 1. Send targets just beyond each limit (yaw $\pm 26^\circ$, pitch $\pm 16^\circ$), 10 commands in total. 2. Confirm each is rejected and TP9 stays low. 3. Set the supply limit to 0.3 A and jog each axis slowly into its hard stop once, under supervision. 4. Read the stop angle with the inclinometer. Pass if: 10 of 10 commands rejected and every hard stop within 1° beyond its software limit. Record: table of commands, responses and stop angles.
M5. Peak motor current ≤ 0.55 A per axis while M2 is met; accessible enclosure surfaces $< 45^\circ\text{C}$ at 25°C ambient.	Equipment: current probe on the J3/J4 motor leads, oscilloscope, thermocouple. 1. Record the motor current during 10 starts and 10 reversals per axis. 2. Run the 60 min duty cycle (one adjustment per minute) at 25°C ambient. 3. Measure the enclosure and motor surface temperature every 10 min. Pass if: peak current ≤ 0.55 A and every surface $< 45^\circ\text{C}$. Record: current waveforms and a temperature log.

Each calibration angle is approached from both directions to separate sensor non-linearity from backlash. Encoder offsets are stored with a version number and checksum and validated at every boot before motion is allowed. Because the sensor measures the mirror axis itself, drivetrain backlash affects the transient response but not the settled feedback reading.

2.6 Power and custom PCB subsystem

This block supports HL1 and HL3 by keeping both rails stable during motor starts and supports HL4 through its reset and sleep behavior. The battery connects to J1 (JST XH). F1 is a resettable 1812 PTC fuse (BOM part Bourns MF-MSMF150/16X-2: 1.5 A hold, 3.0 A trip, 16 V). Q1 (AO3407A P-MOSFET) provides reverse-polarity protection: its gate is pulled to ground by R1 and clamped by the 10 V Zener D1, so it conducts only when the battery is connected the right way. D2 (SMBJ15CA) clamps transients on VBAT. Both regulators run directly from VBAT; there is no 5 V rail. Figures 7–9 in Appendix D show the input protection and both regulators.

The protected commercial 3S Tenenergy 31016 pack from the proposal is kept: 10.8 V nominal, 4.4 Ah, 47.52 Wh [1]. The electronics are designed for 9.0 to 12.6 V and routine discharge stops at 9.6 V, with the pack's per-cell protection setting the absolute limits. Firmware monitors the pack through R2/R3 (100 k/33 k, VBAT_SENSE = VBAT × 33/133, 3.13 V at 12.6 V) and the motor rail through R6/R7 (10 k/10 k, 3.15 V at 6.3 V).

Regulators

U2 and U3 are TPS54302 3 A synchronous bucks switching at 400 kHz with a 0.596 V feedback reference [7]. Their EN pins are left open; the internal pull-up enables both converters whenever VBAT is present.

$$V_{out} = V_{FB} (1 + R_{top} / R_{bottom}) \quad (3)$$

U2 (motor rail) uses R4/R5 = 100 k/11.0 k (1%): $0.596 \times (1 + 100/11.0) = 6.01$ V, with an 82 pF feed-forward capacitor C5 across R4. U3 (logic rail) uses R26/R27 = 49.9 k/11.0 k (1%): $0.596 \times (1 + 49.9/11.0) = 3.30$ V. Both use a 10 µH Bourns SRN6045TA-100M inductor ($I_{sat} \geq 3$ A), 2×22 µF output capacitors and 10 µF + 100 nF input capacitors. Inductor ripple at the worst case 12.6 V input is

$$\Delta I = V_{out} (1 - V_{out} / V_{in}) / (f_{svv} L) \quad (4)$$

which gives $6 \times (1 - 6/12.6) / (400 \text{ kHz} \times 10 \text{ µH}) = 0.79$ A peak-to-peak on the 6 V rail and 0.61 A on the 3.3 V rail. At the 2 A acceptance load the 6 V inductor peak is about 2.4 A, below the inductor rating and the converter's current limit. The logic load (MCU, two AS5600s, VL53L5CX and LEDs) is budgeted at 0.3 A. The analog supply VDDA is fed from +3.3 V through ferrite bead FB1 with C13/C14.

Power requirements and verification

Table 6. Power subsystem requirements and verification.

Requirement	Verification
P1. Motor rail stays within 5.7–6.3 V for 9.0–12.6 V input and 0–2.0 A load, including load steps; the controller does not reset.	Equipment: current-limited bench supply, electronic load, DMM, oscilloscope. 1. Connect the supply to J1 and the electronic load from TP2 (+6 V) to TP5 (GND); motors disconnected. 2. At 9.0, 10.8 and 12.6 V input, set 0, 0.5, 1.0 and 2.0 A; hold each 2.0 A point no longer than 10 s, since at low input voltage the input current approaches F1's 1.5 A hold rating. 3. Read TP2 with the DMM at each point. 4. Step the load from 0.1 to 2.0 A and capture TP2 on the scope while the MCU logs its reset counter. Pass if: every DC and transient reading is within 5.7–6.3 V and no reset occurs. Record: voltage table and transient captures.

Requirement	Verification
P2. Logic rail stays within 3.135–3.465 V at 0–0.3 A and during combined motor starts, with ripple ≤ 100 mV peak-to-peak.	Equipment: oscilloscope (20 MHz bandwidth limit, ground spring), electronic load, DMM. 1. Probe TP4 (+3.3 V) against TP5 (GND). 2. Load the 3.3 V rail through J11 pins 1 and 6 at 0, 0.15 and 0.3 A for 9.0, 10.8 and 12.6 V input. 3. Measure the DC value and peak-to-peak ripple at each point. 4. Start both motors together and capture TP4. Pass if: all readings within 3.135–3.465 V, ripple ≤ 100 mV and no reset. Record: table of DC and ripple values plus the motor-start capture.
P3. The battery prototype runs ≥ 60 min at one adjustment per minute with no resets, no undervoltage shutdown and surface temperature $< 45^\circ\text{C}$ at 25°C ambient.	Equipment: charged pack in a lithium safety bag, DMM or data logger, thermocouple. 1. Charge the pack with the approved charger, then disconnect the charger. 2. Start the test firmware: one automatic adjustment per minute for 60 min. 3. Every minute log VBAT (TP1), +6 V (TP2), +3.3 V (TP4), the adjustment result, the reset count and the surface temperature. Pass if: 60 min completed with no reset, no undervoltage shutdown and every temperature $< 45^\circ\text{C}$. Record: time-series plots of the voltages and temperature.
P4. Reverse-polarity protection, input fuse and sleep pull-down are verified before the battery is connected; both bridge outputs stay disabled through 10 power cycles.	Equipment: current-limited bench supply (12 V, 100 mA limit), DMM, oscilloscope. 1. Check the orientation of F1, Q1 and D2 against the schematic (Appendix D). 2. With no motors connected, apply reversed polarity to J1 and measure TP1. 3. Apply correct polarity and probe TP9, J3 pin 1 and J4 pin 1 through 10 power cycles. Pass if: TP1 stays below 0.5 V under reverse polarity; TP9 stays low and no motor-output pulse appears. Record: readings and scope captures.

Regulator tolerance

The TPS54302 feedback reference is specified as 0.581–0.611 V [7]. With 1% divider resistors the 6 V rail corners are $0.581 \times [1 + 100(0.99)/(11.0 \times 1.01)] = 5.76$ V and $0.611 \times [1 + 100(1.01)/(11.0 \times 0.99)] = 6.28$ V, and the 3.3 V rail corners are 3.16 V and 3.44 V. Both stay inside their requirement windows (5.7–6.3 V and 3.135–3.465 V) under static worst case, but the 6 V rail has only about 20 mV of upper margin left for load-step overshoot. Typical parts sit near 6.01 V and 3.30 V, and P1/P2 measure the real transient behavior.

Energy estimate and PCB current paths

With a conservative $3.3 \text{ V} \times 0.3 \text{ A} = 0.99 \text{ W}$ logic budget, $6 \text{ V} \times 1.0 \text{ A} = 6 \text{ W}$ while moving, 85% converter efficiency and 2 s of movement every 60 s, the average input power is $(0.99 + 6 \times 2/60) / 0.85 \approx 1.40 \text{ W}$. Using 70% of the 47.52 Wh pack gives about 23.8 h, and even continuous 6 W motor loading gives about 4.0 h. These are estimates rather than measured runtime; P3 checks the 60 min requirement directly.

Power nets (VBAT, both switch nodes, +6 V and +3.3 V) are routed at 1.0 mm or wider wherever the pads allow, with +6 V copper pours beside the drivers. A 50 mm, 1.0 mm wide, 35 μm trace has $R = \rho l / (wt) \approx 0.024 \Omega$ ($\rho = 1.68 \times 10^{-8} \Omega \cdot \text{m}$), so 2 A drops 48 mV and dissipates under 0.1 W. Short neck-downs remain where traces enter fine-pitch IC pins. The motor outputs from U4/U5 to J3/J4 are 0.4–0.7 mm wide because they pass between the driver's supply and charge-pump pins, but they carry at most the 0.5 A current limit; IPC-2221 gives about 1.2 A for a 0.4 mm external 1 oz trace at a 10°C rise. Loaded voltage drop and heating are still measured during P1 and P3.

2.7 User interface and debug interfaces

This block supports HL1, because every adjustment starts from a deliberate button press, and HL4, because faults are shown to the rider immediately. J10 connects the handlebar adjustment button between ADJ_BTN (PB13) and ground. R24 (10 k Ω) pulls the input to 3.3 V and C24 (100 nF) forms a 1 ms RC filter; firmware adds a 20 ms debounce, accepts one request per press and requires release before another adjustment. LED_STATUS (PB14) drives the green status LED D3 and LED_FAULT (PB15) the red fault LED D4, each through 330 Ω (about 4 mA); D5 shows that +3.3 V is present. Planned behavior: slow blink while acquiring, fast blink while moving, steady when ready, and a latched fault indication until a healthy new request.

J7 is a 2x5 header matching the 10-pin ST-LINK/V2 programmer pin-out (1 NRST, 2 SWDIO, 6 SWCLK, 3/4 GND, 7/8 3.3 V), so the programmer can power the logic rail with the battery disconnected. J6 carries USART2 TX/RX at 3.3 V for debug logging. J11 brings +3.3 V, ground and four unused GPIOs (PA1, PA15, PB4, PB5) out as spare expansion pins. Figures 11 and 13 (Appendix D) show the user-interface circuits and all connectors.

Table 7. User interface and debug requirements and verification.

Requirement	Verification
U1. Exactly one adjustment request per debounced press; visible status and fault indication in every state.	Equipment: logic analyzer on J10 pin 1 and on the LED_STATUS / LED_FAULT pins, function generator, debug log. 1. Press the button by hand 20 times. 2. Inject 20 bounce bursts (5 pulses within 5 ms) into J10 pin 1 through 1 kΩ. 3. Hold the button for 5 s once. 4. Pull a driver nFAULT line low and watch the fault LED. Pass if: one request per press or burst, one request for the 5 s hold, and the fault LED on within 100 ms. Record: request-count table and LED state table.
U2. The firmware programs and verifies over SWD (J7) in 10 of 10 attempts, and USART2 logging works at 115200 baud.	Equipment: ST-LINK/V2, USB-UART adapter, PC. 1. Disconnect the battery and connect the ST-LINK to J7. 2. Program and verify the release build 10 times. 3. Connect the USB-UART adapter to J6 at 115200 baud and capture a 10 min log. Pass if: 10 of 10 successful program-and-verify cycles and zero framing errors. Record: pass/fail table and a log excerpt.

2.8 Tolerance analysis

Critical interface

The most demanding interface is the depth-based viewing estimate feeding the mirror geometry. An error in the estimated eye position or in the final mirror angle moves the reflected view away from the rear target, so this chain decides whether HL2 passes. We selected this interface as the critical one and will review the budget below with our TA, Zhuoer Zhang, at the design review. The analysis sets the limits that the LiDAR estimate (S2) and the actuation chain (M1, M2) must meet.

Component accuracies

Table 8. Component accuracies used in the tolerance analysis.

Component / parameter	Specified accuracy	Source	Role in the budget
VL53L5CX range, 8×8 at 15 Hz, 0.2–4 m	±5% in the dark; 8% (white) to 11% (grey) at 5 klux; 2.7σ (99.3% of readings)	[4], Table 19	Depth along each zone ray
VL53L5CX field of view	45° × 45° (63° diagonal), 8 zones per axis	[4], Table 2	5.6° zone pitch sets transverse resolution
AS5600 system INL	±1° over 360°, no magnet displacement	[10]	Too large uncalibrated; per-axis calibration required (M1)
AS5600 noise and resolution	0.015° RMS (SF = 00); 0.088° per LSB	[10]	Negligible
Encoder after calibration	≤0.5°	M1	Part of ε _m
Settled control error	≤0.5°	M2	Part of ε _m
Mount and target-frame calibration	0.3° on the reflected ray	Design allowance	Angle term
Mirror aperture	120 × 100 mm	Section 2.2 (design target)	Half-aperture a

The AS5600's uncalibrated ±1° INL alone would use the entire mirror-angle budget, which is why M1 requires a per-axis calibration table over the ±25° and ±15° travel. The total mirror normal error is the worst-case sum of the calibrated encoder error and the settled control error: $\epsilon_m = 0.5^\circ + 0.5^\circ = 1.0^\circ$.

Optical model

Consider one direction perpendicular to the eye-to-mirror line. Let L be the eye-to-mirror distance, $D = 3.0$ m the target distance and a the projected mirror half-aperture. Linearizing a ray reflected from a planar mirror, an eye error ϵ_E shifts the reflection point by $D/(L + D) \cdot \epsilon_E$. A mirror normal error ϵ_m deflects the reflected ray by $2\epsilon_m$ and shifts the reflection point by $LD/(L + D) \cdot \tan(2\epsilon_m)$. The 0.3° allowance is added to that angle, and a target of radius $b = 20$ mm uses $L/(L + D) \cdot b$ of the aperture. The first-order condition is

$$s = [D/(L+D)] \cdot \epsilon_E + [LD/(L+D)] \cdot \tan(2\epsilon_m + 0.3^\circ) + [L/(L+D)] \cdot b \leq a \quad (5)$$

The smaller (vertical) mirror dimension gives a half-height of 50 mm; at incidence up to 25°, $a \geq 50 \cos 25^\circ = 45.3$ mm. With $\epsilon_E \leq 20$ mm (S2) and $\epsilon_m = 1.0^\circ$:

Table 9. Aperture budget from Eq. (5) versus eye-to-mirror distance.

L (m)	Eye term (mm)	Angle term (mm)	Target term (mm)	Total s (mm)	Margin a – s (mm)
0.55	16.9	18.7	3.1	38.7	6.6
0.65	16.4	21.5	3.6	41.5	3.9
0.75	16.0	24.1	4.0	44.1	1.2

L (m)	Eye term (mm)	Angle term (mm)	Target term (mm)	Total s (mm)	Margin a - s (mm)
1.20	14.3	34.4	5.7	54.4	-9.1

Only the eye error perpendicular to the eye-to-mirror line enters Eq. (5): moving the eye along that line leaves the direction e in Eq. (1) unchanged to first order. Because the mirror sits below and to the side of the rider's eyes, this line is inclined to the bicycle axes, so S2 is written perpendicular to and along e (20 mm and 30 mm) rather than in bicycle coordinates, where a fore-aft error would partly project into the perpendicular direction.

Insights from the analysis

- The budget closes across the 0.55–0.75 m eye-to-mirror envelope, with the smallest margin (1.2 mm) at 0.75 m. At 1.2 m it fails by 9.1 mm, so the three test postures, 20 cm apart, are placed inside 0.55–0.75 m.
- The angle term dominates beyond about 0.6 m. If the axes were only required to settle within the $\pm 1.0^\circ$ HL1 limit, ϵ_m would be 1.5° and the budget would fail at every distance (margins of -1.5, -5.5 and -9.3 mm at 0.55, 0.65 and 0.75 m). This is why M2 and the firmware settle band are $\pm 0.5^\circ$ while HL1 keeps $\pm 1.0^\circ$ as the system acceptance limit.
- Reducing ϵ_m from 1.0° to 0.75° through better encoder calibration would raise the margin at 0.75 m from 1.2 mm to 6.5 mm, the most effective improvement available.
- At $L = 0.75$ m the largest eye error that still closes the budget is 21.5 mm, so the 20 mm S2 limit leaves little slack; sensing accuracy is the second limiting factor.

LiDAR resolution and how the estimate reaches 20 mm

With a 45° field over eight zones, each zone spans about 5.6° , or about 74 mm at 0.75 m. Taking a single zone center would leave up to 2.8° (about 37 mm) of transverse uncertainty before any head-to-eye offset error, which would not meet Eq. (5). The design therefore does not rely on raw zone centers:

- A head 150–200 mm wide at 0.5–0.8 m covers several zones, and the weighted centroid of those neighboring zones interpolates between zone centers.
- Each zone's actual ray is calibrated instead of assuming equal 5.6° spacing.
- The $\pm 5\%$ range accuracy is ± 40 mm per zone at 0.8 m (2.7σ , so $\sigma \approx 15$ mm). The random part averages down over about six head zones and five frames (30 samples) to roughly 3 mm if independent; the systematic part is constant for a given rider and distance and is absorbed by the per-rider head-to-eye calibration.
- Batches with a coordinate spread above 30 mm are rejected instead of producing a mirror move.

Ambient light at 5 klux raises the range error to 8–11%, one reason outdoor operation is outside the demonstrated scope. These steps do not mathematically guarantee 20 mm, so S2 measures the achieved accuracy directly and the HL2 rear-target visibility test is the final check. If S2 is not met, the first corrective actions are better zone-ray calibration and head-region selection, tighter actuation error, or narrowing the demonstrated posture envelope while still covering the required 20 cm of head motion.

2.9 Integration verification and bring-up sequence

Table 10. System-level verification of HL1–HL4.

System acceptance	End-to-end procedure
HL1 and HL2 response and visibility	Fix the bicycle and place the measured target 3.0 m behind the mirror. Put the verification camera aperture at the eye midpoint for each of three calibrated postures spanning ≥ 20 cm. Press the button 10 times per posture from varied starting angles; log button time, completion, final independent angles and full target visibility. Pass on latency and angle for accepted adjustments and $\geq 9/10$ visible targets per posture. Record every failure and rejection.
HL3 endurance and clearance	Run the 60 min battery duty cycle (P3) and inspect fasteners before and after. Sweep the handlebar fully left to right 20 times with hands on the grips and brakes operated; record no interference, loosening or cable tension.
HL4 fault response	During commanded motion inject sensing, bus, encoder and driver failures separately. Scope MOTOR_nSLEEP and bridge outputs, then attempt a new request; recovery is allowed only when every validity check is healthy.

Bring-up order: visual inspection and continuity, current-limited rail bring-up (P1, P2, P4), SWD programming (U2), VL53L5CX initialization and bus checks (S5, S4), memory check (C3), sensor and encoder calibration (S2, M1), one-axis then two-axis motion (M2–M5), and finally battery testing (P3). No battery or rider test takes place before the matching protection checks and course safety prerequisites are complete.

3 Cost and schedule

3.1 Parts cost

Part numbers follow the team's v0.2 bill of materials; the itemized BOM with purchase links is in Appendix C. Unit prices for the motors, sensor module and battery come from the proposal's vendor listings [1]; the remaining prices are planning allowances until purchase. Many passives and the 0805 resistors are available from the ECE Electronics Shop at no cost; their allowance is kept as a conservative upper bound. Existing lab instruments are listed at zero incremental cost.

Table 11. Parts cost summary (itemized BOM with purchase links in Appendix C).

Description	Manufacturer / part number	Qty	Unit (\$)	Total (\$)
MCU	ST / STM32F103CBT6	1	8.00	8.00
ToF depth module	ST / VL53L5CX-SATEL	1	21.00	21.00
Buck converters	TI / TPS54302DDCR	2	2.50	5.00
Motor drivers	TI / DRV8876PWPR	2	4.00	8.00
Geared motors	Pololu / #2367 (100:1 MP 6 V)	2	23.95	47.90
Angle sensor modules	ams OSRAM AS5600 breakout with magnet	2	8.00	16.00
Battery	Tenergy / 31016 (3S2P, 4.4 Ah)	1	76.99	76.99
Charger	Compatible 3S Li-ion 12.6 V charger	1	25.00	25.00
Passives, inductors, crystal	R1–R27, C1–C34, L1/L2 (SRN6045TA-100M), FB1, Y1	1	18.00	18.00
Protection and LEDs	F1 (MF-MSMF150/16X-2), Q1 (AO3407A), D1–D5	1	8.00	8.00
Connectors, switches	J1/J3/J4 JST XH, J5–J11 headers, SW1/SW2 SKRKAEE010	1	15.00	15.00
PCB	MirrorPCB v0.2, 2-layer, 100 × 80 mm	1	35.00	35.00
Stencil	v0.2 top stencil	1	15.00	15.00
Mirror	120 × 100 mm acrylic mirror	1	15.00	15.00
Secondary gear stages	20:1 holding stage per axis	2	15.00	30.00
Magnets, clamp, fasteners	Axis magnets, handlebar mount, M3 hardware	1	20.00	20.00
Enclosure and wiring	Printed enclosure, cables, strain relief	1	20.00	20.00
Shipping	Combined allowance	1	20.00	20.00
Parts subtotal				403.89

Labor and services

We use \$50/hour as a planning wage, consistent with the ECE 445 guidance [16], and the specified 2.5 overhead multiplier. Estimated full-project labor is 100 h per partner, covering design, assembly, firmware, testing and reporting.

Table 12. Labor cost.

Team member	Wage	Hours	Calculation	Cost
Bohan Ren	\$50/h	100	$50 \times 2.5 \times 100$	\$12,500
Joshua Rio	\$50/h	100	$50 \times 2.5 \times 100$	\$12,500
Anthony Montalto	\$50/h	100	$50 \times 2.5 \times 100$	\$12,500
Total labor		300		\$37,500

Table 13. Equipment and services.

Equipment or service	Quantity / hours	Basis	Cost (\$)
DMM, oscilloscope, logic analyzer, bench supply	Shared lab access	No incremental charge	0
Electronic load and thermocouple	Shared lab access	No incremental charge	0
ST-LINK/V2 programmer	Lab checkout	No incremental charge	0
Machine shop fabrication / consultation	2 h (estimate)	Estimated at \$50/h; ECE Machine Shop quote requested	100
Verification camera and angle fixture	Team / borrowed	No incremental charge	0
Battery safety bag and insulated tray	1 set	Purchase allowance	20

Direct cost: parts \$403.89 + shop \$100.00 + safety equipment \$20.00 = \$523.89. A 15% contingency (\$78.58) covers substitutions and one board repair, giving a budgeted direct cost of \$602.47. The grand total including labor is **\$38,102.47**. The shop line is an estimate and will be replaced by the ECE Machine Shop quote once the gimbal drawings are submitted. Removing the Raspberry Pi, camera and 5 V regulator from the proposal eliminates their cost and power; the upgrade from the STM32F103C8T6 to the CBT6 adds about \$2.

3.2 Schedule

The plan starts from the September 30 PCB submission and runs through late November. Dates are internal milestones aligned with the course calendar; task ownership can be adjusted by agreement.

Table 14. Weekly schedule and division of labor.

Week of	Work and completion gate	Bohan Ren	Joshua Rio	Anthony Montalto
Sep 28	Freeze v0.2 architecture; PCB DRC/DFM review and Gerber submission.	Sensing approach and ULD study	PCB review and fabrication files	Mechanism envelope
Oct 5	Order remaining parts; VL53L5CX ULD integration on a dev setup; firmware/linker memory check (C3).	ULD integration and memory map	Rail and connector checks; purchasing	Measure clamp and axis geometry
Oct 12	Receive boards; assemble power and MCU; pass rail tests before motors; LiDAR initialization on the PCB (S4, S5).	LiDAR initialization and bus test	Solder and rework; P1/P2, SWD	Build mirror support and gear stages
Oct 19	LiDAR and encoder calibration; sensing accuracy testing (S2).	Head centroid and eye-offset calibration	I2C scheduling and fault state machine	Encoder mounting and angle reference
Oct 26	One-axis control, then two-axis movement; pass M1/M2.	Geometry reference validation	PWM, current limit, debug traces	Drive tuning, backlash, holding
Nov 2	Integrated stationary-bicycle target tests; pass HL1/HL2 across three postures.	Posture and accuracy testing	Fault injection and timing tests	Mount clearances and target fixture
Nov 9	Battery endurance and thermal tests; fix measured failures.	Data analysis and sensing refinements	P3 runtime and safety records	Hold drift and steering sweeps
Nov 16	Final regression, repair margin, demo rehearsal.	Compile sensing results	Freeze firmware and PCB documentation	Freeze mechanics, inspect fasteners
Nov 23	Final report, presentation and demo materials.	Sensing discussion and plots	Electrical results and report integration	Mechanical results and demonstration

Each owner keeps notebook evidence and a second partner reviews the associated test. Parts ordering, LiDAR initialization and sensing accuracy are the critical path. If the S2 accuracy gate fails on October 19, the corrective actions in Section 2.8 start immediately, leaving about two weeks before the integrated tests. The week of November 16 is a repair margin rather than new feature work.

4 Societal impact, standards, ethics and safety

4.1 Societal impact

Automatic alignment can reduce repeated manual mirror adjustment and may help shared-bicycle users or riders with limited reach. It supports convenience and potentially steadier rearward awareness, but a successful bench test does not establish a public-health benefit or a crash reduction. Cycling needs vary between cultures and regions: cost, repair access, weather and local bicycle rules all affect adoption, so the prototype focuses on measurable alignment and clear limits.

The electronics, moving mechanism and rechargeable battery add cost and maintenance compared with a fixed mirror. Removing the Pi and camera reduces the number of assemblies and the expected energy use, while rider calibration can disadvantage people whose head shape, posture, glasses or helmet produce poor depth returns. We will test volunteers with varied postures and report failures. The mirror can still be aligned by hand when powered off, and use never depends on facial identification or network access. Environmental burden includes battery production, PCB fabrication and eventual electronic waste; we use replaceable modules, document connectors for repair, avoid continuous motor holding and recycle batteries and electronics through approved channels.

4.2 Engineering standards and guidance

Table 15. Applicable standards and guidance.

Standard or guidance	Application and evidence
16 CFR Part 1512 and CPSC guidance [3]	Check added hardware against relevant mechanical, braking and handlebar guidance; record clearances, mounting and steering tests. The prototype is not declared compliant as a complete bicycle.
IEC 60825-1 as referenced by the sensor manufacturer [4]	Use the VL53L5CX only in its specified optical configuration; keep the emitter optics and the supplier's Class 1 laser classification. No focusing optics or emitter modifications.
I2C bus and device electrical specifications [5], [6], [10]	Match 3.3 V I/O, addresses, bus speed, rise time and pull-up loading.
IEEE and ACM Codes of Ethics [11], [12]	Prioritize safety, privacy, honest claims and competence; report limitations and seek review of uncertain design interfaces.
ECE 445 ethics, safety and battery guidance [13]–[15]	Complete required training; use supervised work, written battery procedures and the required TA and power-TA approval for protection and charging circuits.

No water-ingress rating, road-vibration qualification, battery certification or legal product compliance is claimed.

4.3 Ethical concerns and changes since the proposal

IEEE and ACM ethics apply directly to honest communication about rear visibility, avoiding harm and respecting privacy [11], [12]. The finished device has no camera: the VL53L5CX returns an 8×8 grid of distances that is processed on the STM32 and not stored, so it cannot record an identifiable image. Only calibration offsets and test logs are kept. The verification camera used for HL2 is test equipment, not part of the product; we obtain consent from test participants, avoid capturing bystanders and keep recordings only as long as needed for the report. Vendor firmware (the VL53L5CX ULD), libraries and source documents are attributed according to course rules [13], and calculated feasibility is never presented as a measured result.

The depth-only design introduces one new concern: the estimate can misplace the viewing point. This is handled by the S2 calibration gate and by rejecting uncertain measurements so that the mirror stays still and

the fault LED lights. Riders must continue normal rearward checks; the device does not detect vehicles, warn of collisions or guarantee a clear rear view.

4.4 Electrical and mechanical hazards

A 3S lithium-ion pack can deliver damaging short-circuit current despite its modest voltage. Hazards include reversed connectors, damaged insulation, overcharge, over-discharge, overheating, stalled motors and solder bridges. The board has a resettable input fuse, reverse-polarity protection and a TVS clamp; we also use a protected commercial pack, an approved charger, keyed JST connectors, insulated terminals and strain relief. Bench tests start from a current-limited supply, and the input protection, current limits and buck polarity are checked before battery use.

Moving gears create pinch points, mirror edges can cut and a loose handlebar mount can affect steering or braking. Gears are guarded, mirror edges covered, physical travel stops added and the assembly tethered where appropriate. Fingers stay outside the mechanism while powered, the sensor and battery are mounted clear of the brakes and grips, and a power disconnect stays within reach. All rider and target tests are done with the bicycle fixed and the wheels blocked; any later moving test would need a separate risk review, a controlled area and protective equipment.

4.5 Battery and lab safety work instruction

All team members complete the course's mandatory lab safety training and follow the two-person rule in the lab [14]. Before lithium battery work we complete the additional fire-safety training and obtain the required review of protection and charging circuits by our TA and a power-focused TA. Charge and discharge testing uses lithium safety bags and written procedures as required by the course battery document [15].

- **Before use:** inspect the pack for swelling, dents, leaks, odor, damaged leads or heat; verify connector polarity, charger compatibility and protection limits; place the pack in the safety bag on an insulated, non-flammable surface. Remove conductive jewelry and keep the disconnect within reach.
- **Charging:** use only the approved 3S charger and the manufacturer's limits; never charge through the mirror PCB or leave charging unattended.
- **Discharging:** log pack voltage and temperature; stop at the 9.6 V cutoff, a protection trip, unusual heating, swelling, odor or noise. Never bypass protection or short the pack to test a fuse; use a limited bench supply for electrical fault injection.
- **After testing:** switch off and disconnect the pack, insulate exposed terminals, inspect leads and store it in a non-conductive container. Recycle damaged packs through the approved campus process.
- **Emergency:** stop work, move away and alert lab staff; disconnect only if safe; follow posted emergency guidance and call emergency services for smoke or fire.

5 References

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- Requirement and verification tables follow [17] and [19]; the error budget follows [18].

Appendix A Connector and test point map

Pin assignments are taken from the v0.2 schematic netlist (Appendix D). Identify the pin-1 marker on the board before making any cable and check continuity and polarity with a DMM.

Table 16. Connector pin map.

Connector	Pins
J1 battery (JST XH)	1 VBAT_IN; 2 GND
J3 yaw motor (JST XH)	1 YAW_OUT1; 2 YAW_OUT2
J4 pitch motor (JST XH)	1 PITCH_OUT1; 2 PITCH_OUT2
J5 VL53L5CX (2×3)	1 +3.3V; 2 LIDAR_LPN; 3 PITCH_SCL; 4 LIDAR_INT; 5 PITCH_SDA; 6 GND
J6 debug UART	1 DBG_TX (PA2); 2 DBG_RX (PA3); 3 GND
J7 ST-LINK (2×5)	1 NRST; 2 SWDIO; 3 GND; 4 GND; 5 NC; 6 SWCLK; 7 +3.3V; 8 +3.3V; 9 NC; 10 NC
J8 AS5600 yaw	1 +3.3V; 2 YAW_SCL; 3 YAW_SDA; 4 GND
J9 AS5600 pitch	1 +3.3V; 2 PITCH_SCL; 3 PITCH_SDA; 4 GND
J10 adjust button	1 ADJ_BTN; 2 GND
J11 spare I/O	1 +3.3V; 2 PA1; 3 PA15; 4 PB4; 5 PB5; 6 GND

Table 17. Test points.

Test point	Net	Use
TP1	VBAT	Battery rail after protection
TP2	+6V	Motor supply
TP4	+3.3V	Logic supply
TP5	GND	Ground reference
TP6	DRV_VREF	Current-limit reference (3.0 V)
TP7	YAW_IPROPI	Yaw current feedback (6.04 V/A)
TP8	PITCH_IPROPI	Pitch current feedback (6.04 V/A)
TP9	MOTOR_nSLEEP	Shared motor-driver sleep/enable

J7 follows the 10-pin ST-LINK/V2 header pin-out; check the specific programmer or adapter against this table before connecting. The silkscreen also marks 1=RST, 2=SWDIO and 6=SWCLK.

Appendix B Assembly checklist

Table 18. Assembly checklist.

Item	Confirmation before final assembly
Parts and BOM	Every fitted part matches the v0.2 BOM order code, package and orientation; polarized parts (C8, D1–D5, Q1) and IC pin 1 checked.
Power stage	U2/U3 output voltages, F1 and Q1 orientation and the TVS checked on a current-limited supply before any motor or sensor is connected (P1, P2, P4).
MCU and clock	STM32F103CBT6 fitted; 8 MHz oscillator starts; reset and boot straps correct; SWD connects (U2).
Firmware memory	Linker map within the C3 flash and SRAM limits with the ULD firmware image included.
LiDAR	VL53L5CX-SATEL module at 3.3 V, J5 cable pin-out, effective pull-ups and sensor orientation confirmed; initialization passes S5.
Motor drivers	DRV8876 exposed pads soldered (hot air or oven); VREF = 3.0 V at TP6; current limit checked at reduced load before full travel.
Sensing accuracy	S2 passed with frozen calibration and an independent eye reference.
Mechanical geometry	Mirror size, pivot location, incidence angle, gear ratio, moving mass, clamp size and stops measured; M3 and clearance tests passed.
Battery and approvals	Pack and charger part numbers, protection limits, fuse coordination, course training and TA/power-TA review completed before battery tests.
Budget and schedule	Allowances replaced with receipts; course milestone dates confirmed.

Appendix C Bill of materials

Itemized from the v0.2 KiCad schematic. Digi-Key and Amazon links are search links for the listed part number or specification; parts marked ECE Electronics Shop are stocked there at no cost.

Table 19. PCB bill of materials (per board).

Reference	Qty	Description	Manufacturer / part number	Purchase link
U1	1	MCU, Cortex-M3, 128 KB flash, LQFP-48	ST STM32F103CBT6	https://www.digikey.com/en/products/result?keywords=STM32F103CBT6
U2, U3	2	Buck converter, 4.5–28 V in, 3 A, SOT-23-6	TI TPS54302DDCR	https://www.digikey.com/en/products/result?keywords=TPS54302DDCR
U4, U5	2	H-bridge driver, PH/EN, 3.5 A peak, HTSSOP-16	TI DRV8876PWPR	https://www.digikey.com/en/products/result?keywords=DRV8876PWPR
Q1	1	P-MOSFET –30 V, –4.3 A (reverse polarity), SOT-23	AOS AO3407A	https://www.digikey.com/en/products/result?keywords=AO3407A
D1	1	Zener 10 V, 500 mW, SOD-123	Diodes BZT52C10-7-F	https://www.digikey.com/en/products/result?keywords=BZT52C10-7-F
D2	1	TVS 15 V bidirectional, 600 W, SMB	Littelfuse SMBJ15CA	https://www.digikey.com/en/products/result?keywords=SMBJ15CA
F1	1	PTC fuse 1.5 A hold / 3 A trip, 16 V, 1812	Bourns MF-MSMF150/16X-2	https://www.digikey.com/en/products/result?keywords=MF-MSMF150%2F16X-2
L1, L2	2	Inductor 10 μ H, $I_{sat} \geq 3$ A, 6×6 mm	Bourns SRN6045TA-100M	https://www.digikey.com/en/products/result?keywords=SRN6045TA-100M
FB1	1	Ferrite bead 600 Ω @ 100 MHz, 0805	Murata BLM21PG601SN1D	https://www.digikey.com/en/products/result?keywords=BLM21PG601SN1D
Y1	1	Crystal 8.000 MHz, CL 10 pF, 5.0×3.2 mm	Abrakon ABM3B-8.000MHZ-10-1-U-T	https://www.digikey.com/en/products/result?keywords=ABM3B-8.000MHZ-10-1-U-T
SW1, SW2	2	Tactile switch SPST-NO (RESET, BOOT)	Alps SKRKAEE010	https://www.digikey.com/en/products/result?keywords=SKRKAEE010
D3, D5	2	LED green, 0805	Lite-On LTST-C171GKT	https://www.digikey.com/en/products/result?keywords=LTST-C171GKT
D4	1	LED red, 0805	Lite-On LTST-C171KRKT	https://www.digikey.com/en/products/result?keywords=LTST-C171KRKT
C1, C3, C4, C9, C12, C15–C17, C19, C22–C25, C27, C29, C31	16	Capacitor 100 nF, 50 V X7R, 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
C28, C32	2	Capacitor 22 nF, 50 V X7R, 0805 (driver CFLY)	Generic	https://www.digikey.com/en/products/result?keywords=22nF+50V+X7R+0805
C14	1	Capacitor 10 nF, 50 V X7R, 0805	Generic	https://www.digikey.com/en/products/result?keywords=10nF+50V+X7R+0805
C20, C21	2	Capacitor 10 pF, 50 V C0G, 0805	Generic	https://www.digikey.com/en/products/result?keywords=10pF+50V+C0G+0805
C5	1	Capacitor 82 pF, 50 V C0G, 0805	Generic	https://www.digikey.com/en/products/result?keywords=82pF+50V+C0G+0805
C11, C13	2	Capacitor 1 μ F, 25 V X7R, 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
C18	1	Capacitor 10 μ F, 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
C2, C10, C26, C30	4	Capacitor 10 μ F, 25 V X7R, 1206	Generic	https://www.digikey.com/en/products/result?keywords=10uF+25V+X7R+1206
C6, C7, C33, C34	4	Capacitor 22 μ F, 25 V X7R, 1210	Generic	https://www.digikey.com/en/products/result?keywords=22uF+25V+X7R+1210

Reference	Qty	Description	Manufacturer / part number	Purchase link
C8	1	Electrolytic 100 μ F, 16 V, 6.3 $\times$ 7.7 mm SMD	Generic	https://www.digikey.com/en/products/result?keywords=100uF+16V+electrolytic+6.3x7.7
R1, R6–R9, R13, R15, R17, R19, R24	10	Resistor 10 k Ω 1%, 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
R2, R4, R14	3	Resistor 100 k Ω 1%, 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
R3	1	Resistor 33 k Ω , 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
R5, R27	2	Resistor 11.0 k Ω 1%, 0805	Generic	https://www.digikey.com/en/products/result?keywords=11.0k+1%25+0805+resistor
R26	1	Resistor 49.9 k Ω 1%, 0805	Generic	https://www.digikey.com/en/products/result?keywords=49.9k+1%25+0805+resistor
R16, R18	2	Resistor 6.04 k Ω 1%, 0805	Generic	https://www.digikey.com/en/products/result?keywords=6.04k+1%25+0805+resistor
R20–R23	4	Resistor 5.1 k Ω , 0805 (I2C pull-ups)	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
R10–R12	3	Resistor 330 Ω , 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
R25	1	Resistor 1 k Ω , 0805	Generic	ECE Electronics Shop (free): https://ece.illinois.edu/about/eshop
J1, J3, J4	3	JST XH 2-pin header, vertical	JST B2B-XH-A(LF)(SN)	https://www.digikey.com/en/products/result?keywords=B2B-XH-A%28LF%29%28SN%29
J5	1	Female header 2 $\times$ 3, 2.54 mm	Generic	https://www.digikey.com/en/products/result?keywords=female+header+2x3+2.54mm
J6	1	Female header 1 $\times$ 3, 2.54 mm	Generic	https://www.digikey.com/en/products/result?keywords=female+header+1x3+2.54mm
J7	1	Female header 2 $\times$ 5, 2.54 mm	Generic	https://www.digikey.com/en/products/result?keywords=female+header+2x5+2.54mm
J8, J9	2	Female header 1 $\times$ 4, 2.54 mm	Generic	https://www.digikey.com/en/products/result?keywords=female+header+1x4+2.54mm
J10	1	Female header 1 $\times$ 2, 2.54 mm	Generic	https://www.digikey.com/en/products/result?keywords=female+header+1x2+2.54mm
J11	1	Female header 1 $\times$ 6, 2.54 mm	Generic	https://www.digikey.com/en/products/result?keywords=female+header+1x6+2.54mm
TP1–TP9, H1–H4	–	Test pads and M3 mounting holes (PCB copper only)	–	Part of the PCB

Table 20. Off-board modules, mechanical parts and wiring.

Item	Qty	Description	Manufacturer / part number	Purchase link
ToF module	1	VL53L5CX breakout, 8 $\times$ 8 zones, 3.3 V	ST VL53L5CX-SATEL	https://www.st.com/en/evaluation-tools/vl53l5cx-satel.html
Motors	2	Gearmotor 100:1 micro metal MP, 6 V	Pololu #2367	https://www.pololu.com/product/2367

Item	Qty	Description	Manufacturer / part number	Purchase link
Angle sensors	2	AS5600 magnetic encoder module with diametric magnet	Generic AS5600 breakout	https://www.amazon.com/s?k=AS5600+magnetic+encoder+module
Battery	1	Li-ion 3S2P 10.8 V 4400 mAh with PCB protection	Tenergy 31016	https://power.tenergy.com/at-tenergy-li-ion-18650-10-8v-4400mah-rechargeable-battery-pack-w-pcb-3s2p-47-52wh-5-7a-rate/
Charger	1	3S Li-ion smart charger, 12.6 V	Tenergy (compatible model)	https://www.amazon.com/s?k=Tenergy+12.6V+Li-ion+smart+charger
Connector housings	6	JST XH 2-pin housing	JST XHP-2	https://www.digikey.com/en/products/result?keywords=XHP-2
Crimp terminals	20	JST XH crimp terminal	JST SXH-001T-P0.6	https://www.digikey.com/en/products/result?keywords=SXH-001T-P0.6
Button	1	Momentary push button for handlebar	Generic	https://www.amazon.com/s?k=handlebar+momentary+push+button+waterproof
Mirror	1	Acrylic mirror sheet, cut to 120 × 100 mm	Generic	https://www.amazon.com/s?k=acrylic+mirror+sheet
Gear stages	2	20:1 worm gear set (secondary holding stage)	Generic	https://www.amazon.com/s?k=worm+gear+set+20%3A1+small
Hardware	1	M3 screws, nuts and standoffs	Generic	https://www.amazon.com/s?k=M3+standoff+screw+nut+kit
Wire	1	20–22 AWG hook-up wire, red/black	Generic	https://www.digikey.com/en/products/result?keywords=22+AWG+hook-up+wire
PCB	1	MirrorPCB v0.2, 2-layer, 100 × 80 mm	Course PCB order (TA)	https://jlcpcb.com
Programmer	1	ST-LINK/V2 (lab checkout)	ST ST-LINK/V2	Lab checkout

Appendix D Schematic excerpts

The following pages reproduce the main circuit blocks of the v0.2 KiCad schematic in landscape so that reference designators, values and net names stay readable. The MCU pin assignment is shown in Figure 5.

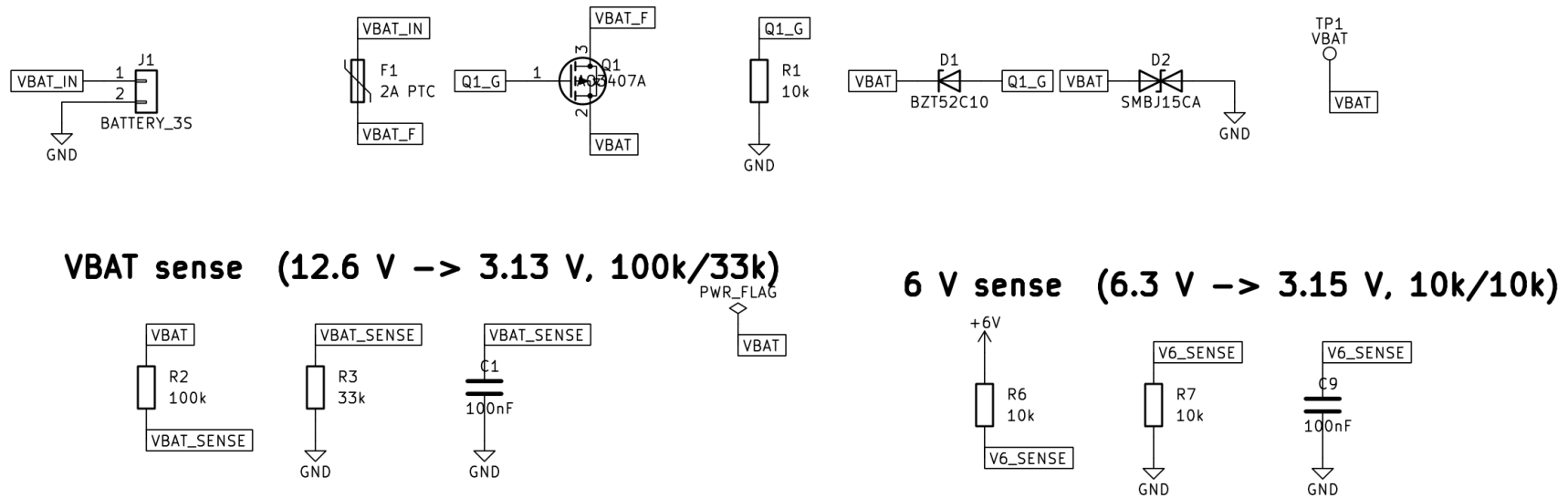
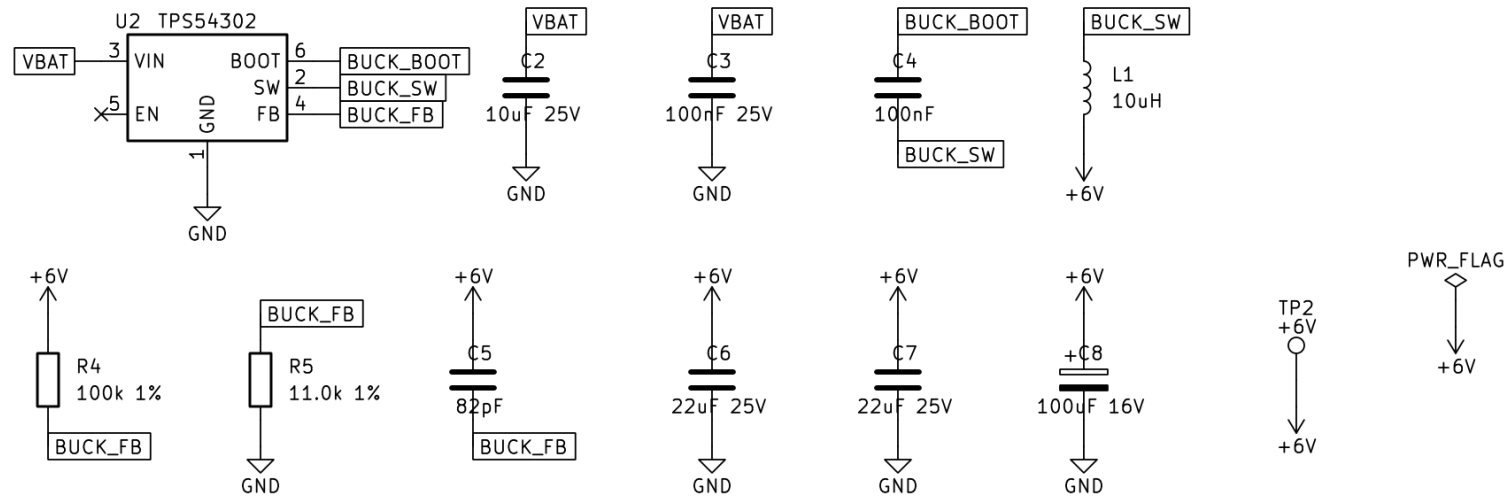


Figure 7. Battery input and protection (J1, F1, Q1, D1, D2) with the VBAT and +6 V sense dividers.

2. 6 V MOTOR RAIL (TPS54302, VFB = 0.596 V, 400 kHz)



$V_{out} = 0.596 \times (1 + 100k/11.0k) = 6.01 \text{ V}$. EN left open = always on. L1: 10 uH, $I_{sat} \geq 3 \text{ A}$ (Bourns SRN6045TA-100M).

Figure 8. 6 V motor-rail buck converter U2 (TPS54302, R4/R5 = 100 k/11.0 k, C5 feed-forward).

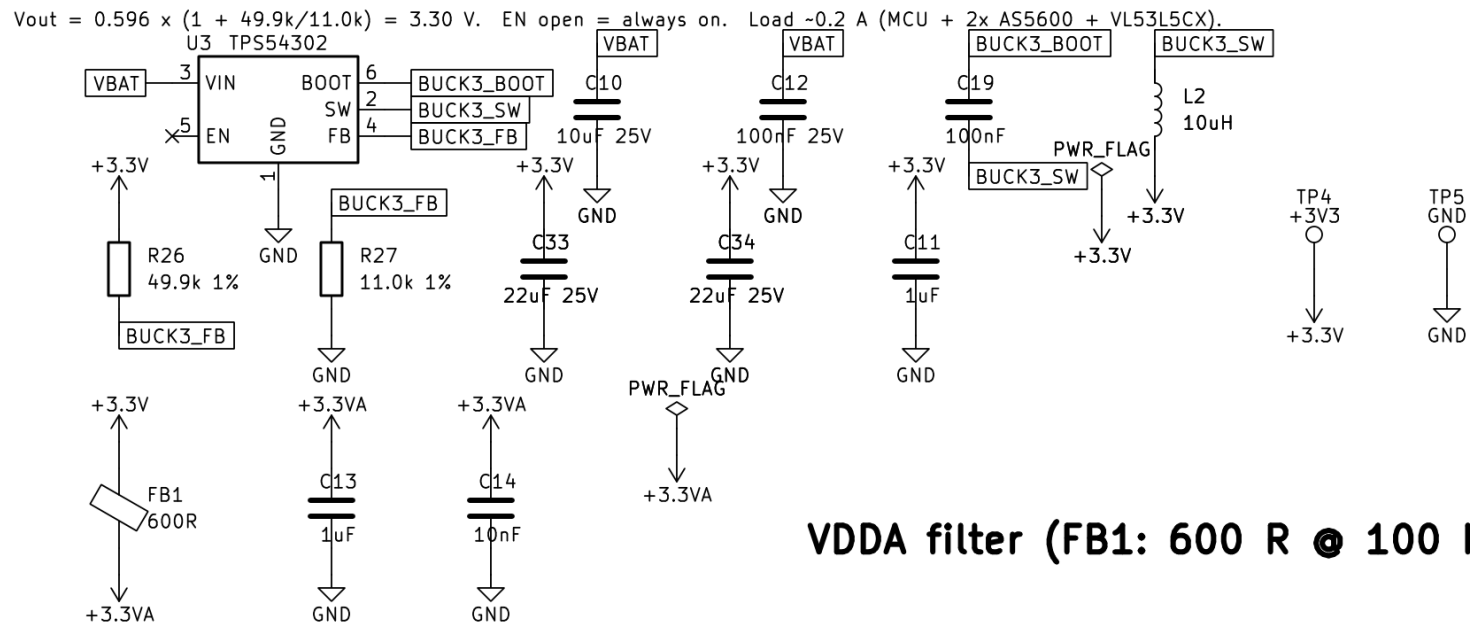
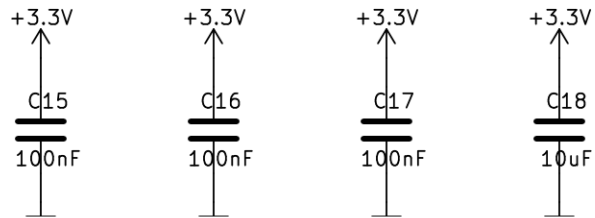
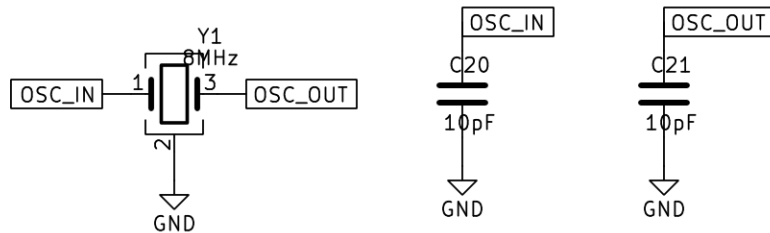


Figure 9. 3.3 V logic-rail buck converter U3 (TPS54302, R26/R27 = 49.9 k/11.0 k) and the VDDA filter FB1/C13/C14.

Decoupling (one 100nF at each VDD pin)



8 MHz crystal (5032, same as CAD assignment)



Reset / Boot

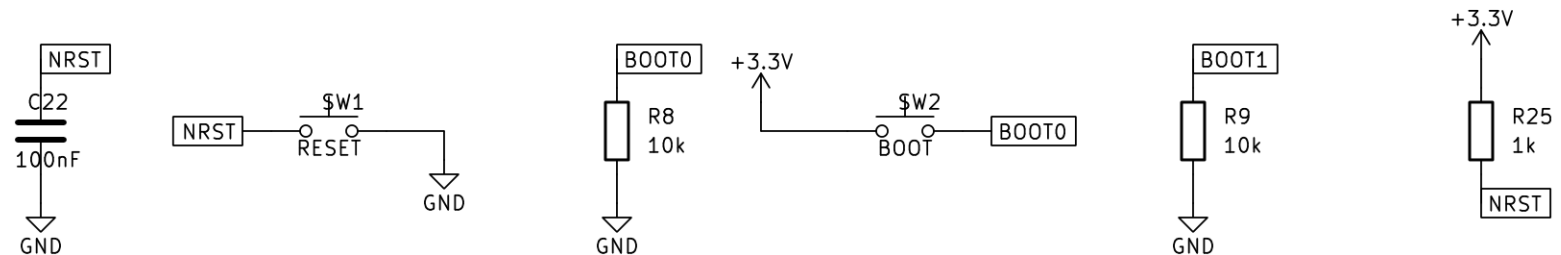


Figure 10. MCU support: VDD decoupling, 8 MHz crystal Y1 and the reset/boot network.

LEDs

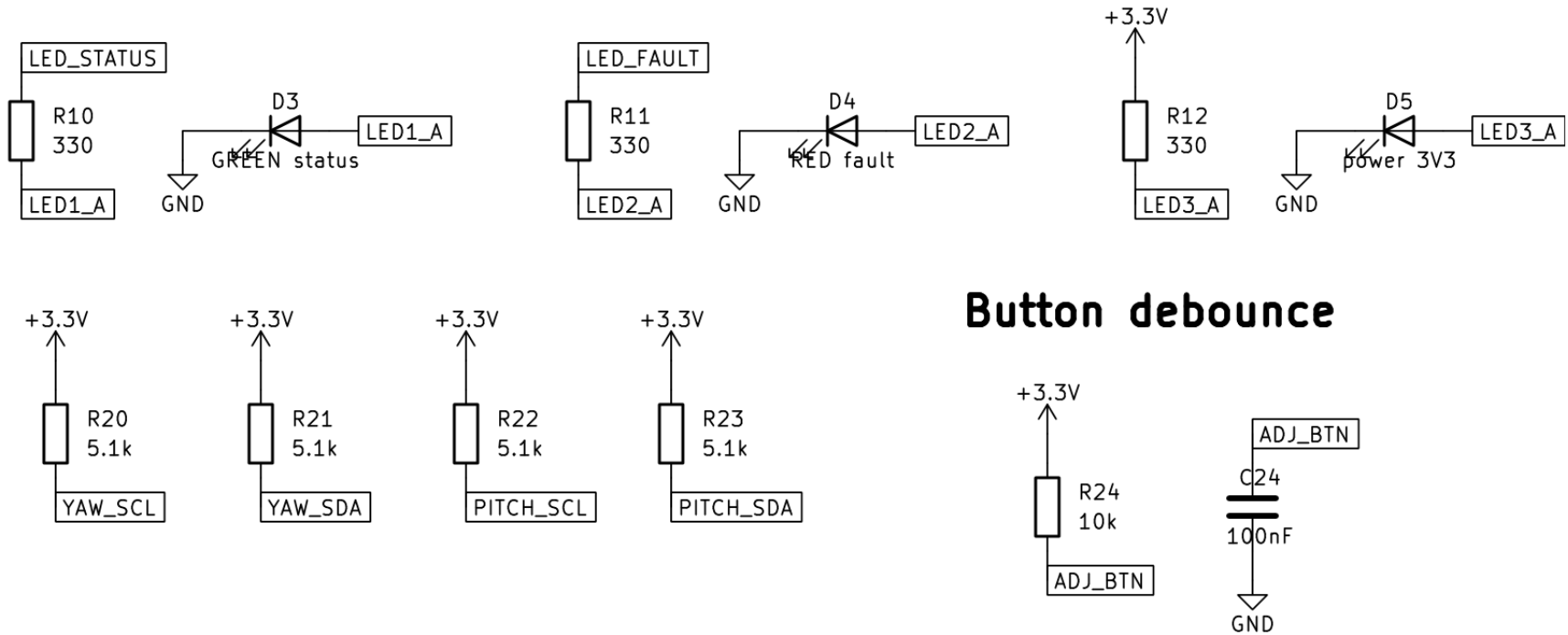
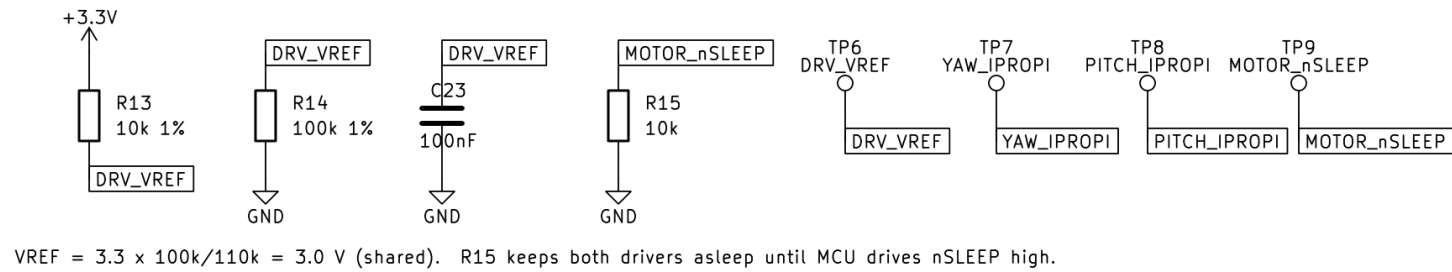


Figure 11. Status, fault and power LEDs; I2C pull-ups R20–R23; adjustment-button filter R24/C24.



YAW axis

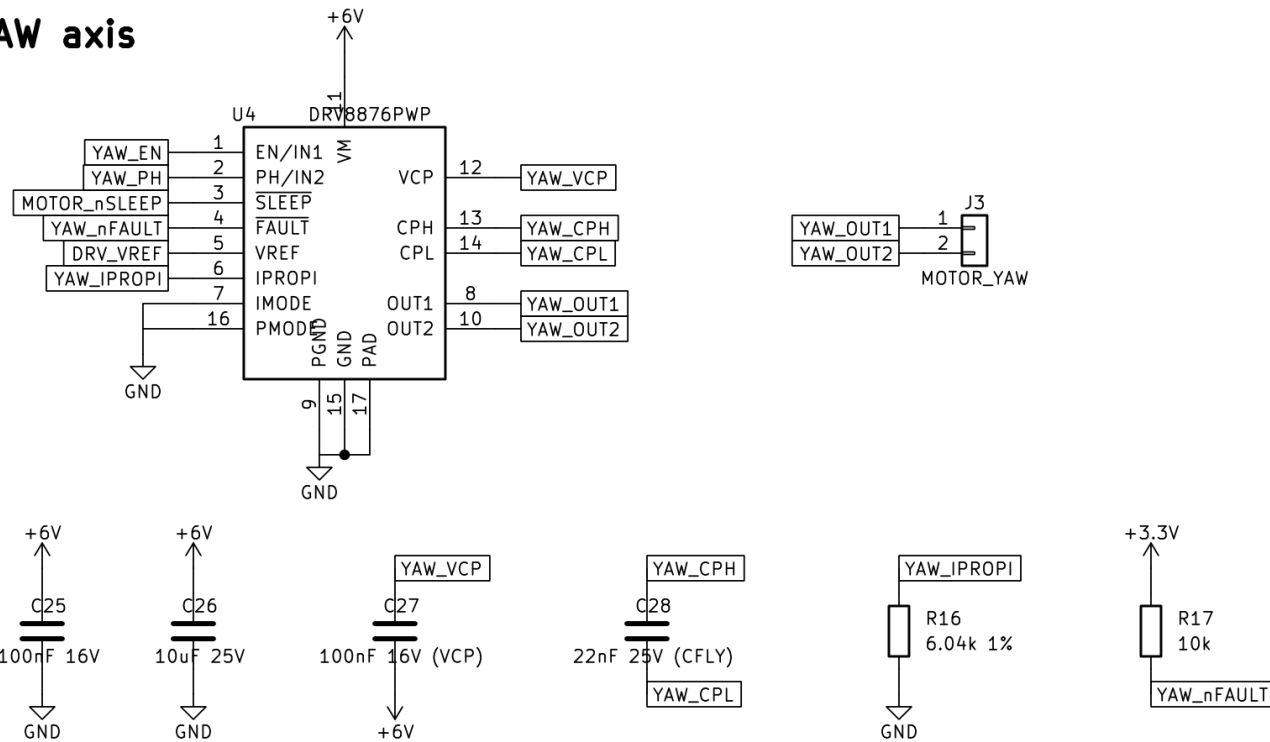


Figure 12. Yaw motor driver U4 (DRV8876, PH/EN mode) and the shared VREF and sleep network. The pitch driver U5 is identical (C29–C32, R18, R19, J4).

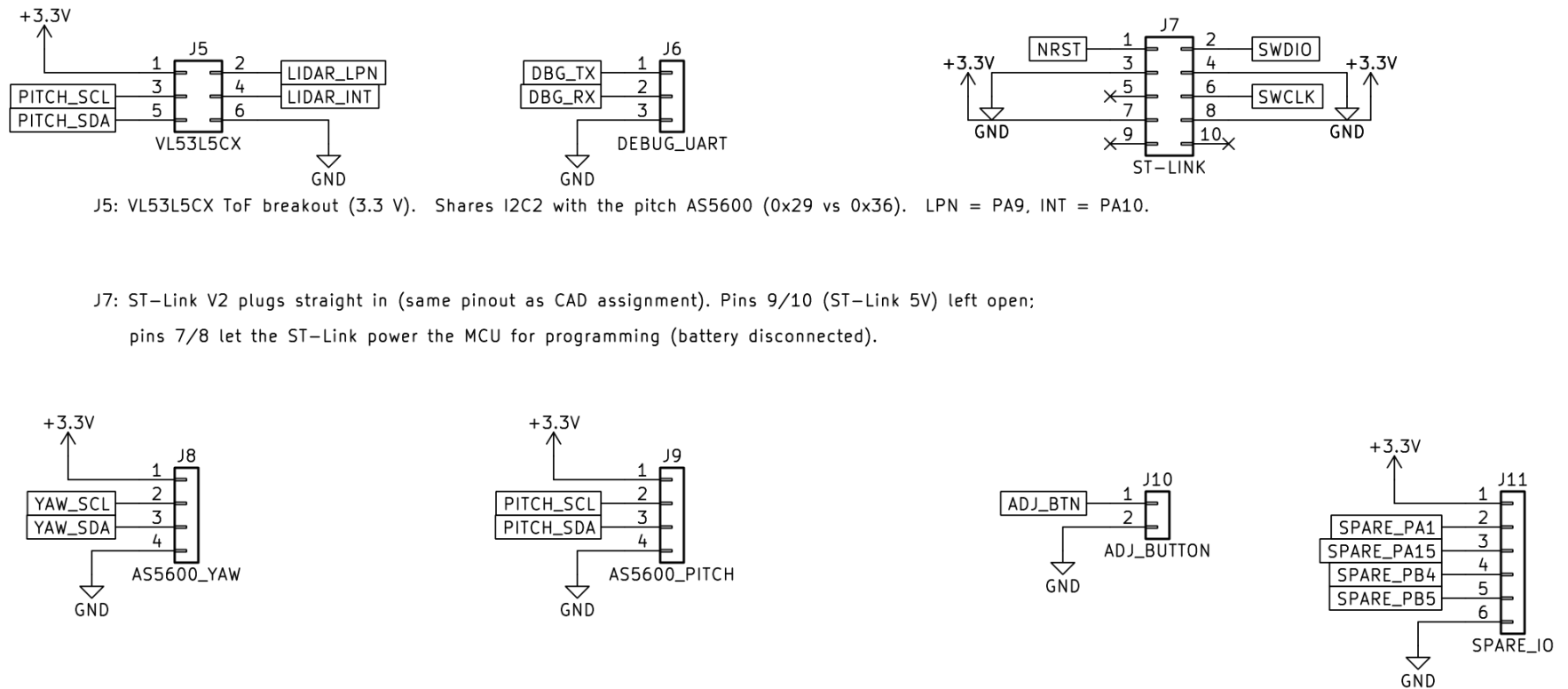


Figure 13. Off-board connectors: VL53L5CX (J5), debug UART (J6), ST-LINK SWD (J7), AS5600 yaw/pitch (J8, J9), adjustment button (J10) and spare I/O (J11).