

Consumer-Friendly Spatial Anti-Jamming for WiFi Security Cameras

By
Alexander Bessonov
Everest Bencher
Michael Przybyl

Initial Report for ECE 445, Senior Design, Spring 2026 TA: Pusong Li
September 18th 2026 Project #33

Contents

1. Introduction	3
1.1 Problem	3
1.2 Solution	3
1.3 Visual Aid	4
1.4 High Level Requirements	4
2. Design	5
2.1 Block Diagram	5
2.2 Subsystem Overview and Requirements	5
2.2.1 Receive RF Chain Subsystem	5
2.2.1.1 Overview	5
2.2.1.2 Requirements	6
2.2.1.3 Components	7
2.2.2 Power Detect Subsystem	7
2.2.3.1 Overview	7
2.2.3.2 Requirements	7
2.2.3.3 Components	8
2.2.3 Control Subsystem	8
2.2.4.1 Overview	8
2.2.4.2 Requirements	9
2.2.4.3 Components	10
2.2.5 Power Subsystem	10
2.3 Constraints and Tolerance Analysis	12
2.3.1 Systems Budgeting	12
2.3.2 Criterion For Success	13
2.3.3 Limitations	13
2.3.3.1 Friendly Signals	13
2.3.3.2 Wide-Band Jammers	14
2.3.3.3 Sympathetic Nulls	14
3. Cost and Schedule	14
3.1 Cost Analysis	14
3.1.1 Labor	14
3.1.2 Parts	14
3.1.3 Total Cost	16
3.2 Schedule	16
4. Ethics, Safety and Societal Impact	17
5. Citations	18

1. Introduction

1.1 Problem

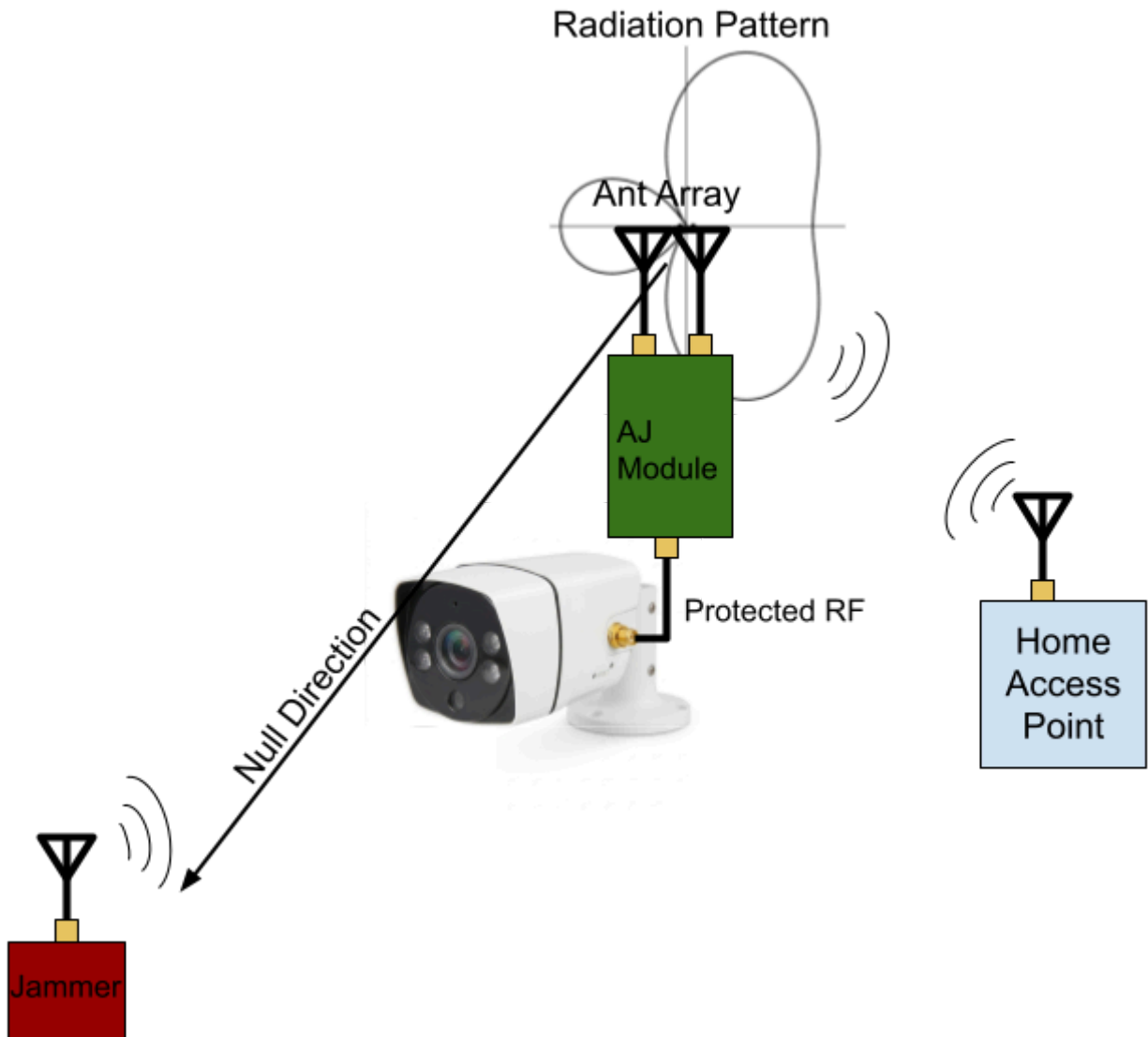
Today there are still numerous wireless systems still susceptible to malicious attacks from cheap RF jammers. Recent news articles report how burglars are using WiFi jammers to disable home security cameras before breaking and entering. These jammers are broad-band noise jammers that demand more than just digital filtering to mitigate, but spatial nulling at the antenna array. Conventional spatial anti-jamming (AJ) systems rely on high-speed digitizers and heavy signal processing to calculate adaptive weights. Having a digitization stage then forces the use of automatic-gain-control (AGC) to prevent ADC saturation. All said, this approach is impractical for size/cost/power constrained systems. Meanwhile, alternative countermeasures like spread-spectrum or frequency hopping technologies demand broad spectral allocations and have low bandwidth (non-ideal for video transmission). This motivates the development of a consumer-friendly solution for spatial AJ.

1.2 Solution

We propose a spatial AJ add-on module that would replace the rubber duck antenna on a typical 2.4 GHz WiFi security camera. The module features two SMA inputs for a receive antenna array (one of which doubles as a transmit antenna) and one SMA port connecting directly to the camera's RF interface. The choice of a two element antenna array limits the scope of the project by reducing hardware and processing complexity.

The module would be able to null one adversary jammer and provide the end device with protected RF. Instead of digitizing the incoming RF, the module taps total signal power. The presence of a jammer would show up as a high power reading. An MCU monitors this power level and performs a gradient descent algorithm to tune the phase of one RF channel in order to minimize the jammer's effect. As a result, a deep spatial null is steered toward the jammer's direction.

1.3 Visual Aid

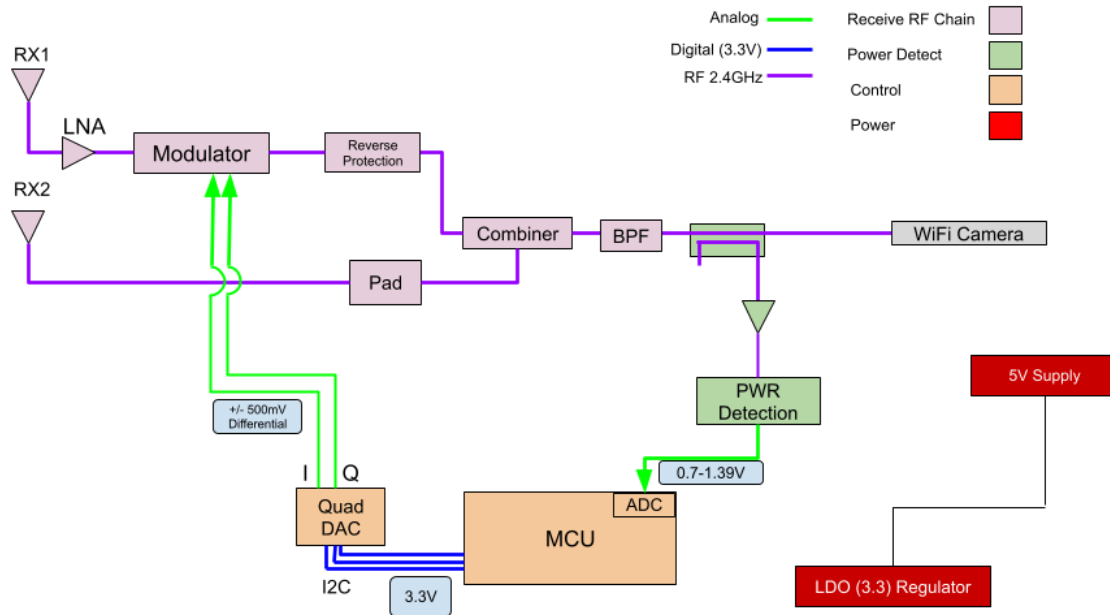


1.4 High Level Requirements

- At a high level, the module should help mitigate an external jammer from overwhelming a WiFi receiver by placing a spatial null of the radiation pattern in the direction of the jammer. The module should converge on a minimum of a 20 dB null depth.
- The AJ module should not significantly degrade the friendly WiFi signal. Total system gain should be no lower than -6 dB and noise figure no greater than 10 dB. The AJ algorithm must not incidentally null the access point's WiFi signal.
- The AJ module must maintain full bidirectional Wi-Fi communication capabilities. To support this, the module must be able to pass through up to +20 dBm signals from the WiFi device without causing damage to the RF circuitry.

2. Design

2.1 Block Diagram



2.2 Subsystem Overview and Requirements

2.2.1 Receive RF Chain Subsystem

2.2.1.1 Overview

This subsystem serves as the front-end for the received WiFi and jammer signals. It begins with two SMA inputs for two antennas. Channel 1 routes through a RF vector modulator, which applies continuous phase adjustments based on control signals from the MCU. Channel 2 routes through a fixed attenuation pad to match the inherent insertion loss of the modulator, ensuring equal power levels between the channels. These two channels are summed into one through a RF combiner which produces the destructive interference in the direction of the jammer. The combined signal is then fed through a 2.4 GHz WiFi

bandpass filter and passed to the power detect subsystem. This ensures that out-of-band signals or jammers don't unintentionally influence the AJ loop.

2.2.1.2 Requirements

This subsystem contributes to the high level requirements by performing the phase change and channel addition that causes destructive interference of the jammer.

- The inputs should interface with the antennas using SMA connectors. Both the inputs and outputs should present 50 ohm impedances
- The LNA must be <2 dB noise figure and >15 dB of gain in order to maintain system gain and noise figure according to the first high level requirement
- The modulator must have a dynamic input power range from -60 dBm to +0 dBm to properly receive weak WiFi signals while not becoming saturated by a higher power jammer
- There must be >30 dB of out-of-band rejection from the BPF such that out-of-band signals don't influence the AJ loop during power detection
- A PIN diode protection circuit must be implemented on channel 1 that limits power to <+15 dBm

Requirements	Verification
Impedance Matching & Return Loss: Both RF inputs and the combined output port must present a characteristic impedance of $50\Omega \pm 5\Omega$ with a return loss < 10 dB.	Equipment: Vector network analyzer Procedure: Measure the S parameters of the entire RF path and take the S11 to calculate the return loss for a 50 ohm reference.
Dynamic Range: Both RF inputs must be able to pass through power within a dynamic range of -60 dBm to +0 dBm without distortion.	Equipment: Vector network analyzer, signal generator, spectrum analyzer Procedure: (1) Measure the S parameters of the entire RF path over power levels from -60 dBm to +0 dBm with a 10 dB increment. Examine the S21 and ensure the response is consistent. (2) Inject a 2.45 GHz tone at -60 dBm into the module input and measure the output tone using a spectrum analyzer. Ensure there are no spurs resulting from component nonlinearity. Repeat with increasing input power on the signal generator using a 10 dB increment until +0 dBm.
Reverse Protection: Channel 1 must be reverse protected to protect the active circuitry from outgoing TX signals from the WiFi device. PIN diodes must be installed to limit power to ~+13 dBm and a ~12 dB attenuation pad shall attenuate the power to +1 dB which is below the maximum power on the modulator output.	Equipment: Multimeter Procedure: (1) Use the resistance setting on the multimeter to ensure the attenuation of the pad is approximately 12 dB. (2) In the diode on condition, test the diode resistance and estimate the dynamic forward voltage. Use this to calculate the power for a 50 ohm load.

2.2.1.3 Components

- LNA: TSS-53LNB+
- RF Modulator: AD8341
- Combiner: PD2425J5050S2HF
- Bandpass Filter: 2450BP08A0100001T

2.2.2 Power Detect Subsystem

2.2.3.1 Overview

This subsystem taps RF energy from received waves to supply feedback for the spatial nulling algorithm. A forward -20 dB directional coupler taps a fraction of the combined receive signal and routes it to a logarithmic power detector, which converts RF power into a linear DC voltage for the MCU to read. An amplifier is put in place to maintain the power within the power detector's dynamic range.

2.2.3.2 Requirements

This subsystem contributes to the high level requirements by providing the continuous power monitoring to the control subsystem in order to perform the nulling algorithm

- The RF inputs and outputs must present 50 ohm impedances. The power detector analog output must be within the MCU ADC's full-scale voltage of 0 to 3.3V.
- The power detector must function over a dynamic range from -60 dBm to +0 dBm

Requirements	Verification
1. Power measurement: At the selected WiFi test frequency, the subsystem shall measure RF power from -60 to 0 dBm at its main RF input, with calibrated measurement error within ± 1 dB under CW excitation.	Equipment: Calibrated RF signal generator, calibrated attenuators, 50 Ω termination, DMM, and computer for recording readings. Procedure: (1) Account for cable and attenuator losses to establish power at the subsystem input. (2) Connect the generator to the main RF input and terminate the main RF output in 50 Ω. (3) Apply the subsystem's calibration procedure. (4) Sweep input power from -60 to 0 dBm in 5 dB steps using independent validation readings. (5) Record detector voltage and convert it to estimated RF input power using the calibration. Confirm each estimate is within ± 1 dB of the applied power. Results: Present a table of applied power, output voltage, estimated power, and error, plus a calibration/error plot.
2. MCU interface: With the MCU connected, the	Equipment: Oscilloscope, DMM, RF signal

detector output shall remain between 0 and 3.3 V throughout the specified RF input range, including startup and input-power changes. The output shall also remain within the MCU ADC's configured usable measurement range during normal operation.	generator, and connected MCU board. Procedure: (1) Probe the detector output at the MCU ADC input relative to board ground. (2) Sweep the RF input over the specified range. (3) Capture supply startup and changes between minimum and maximum input power. (4) Confirm no excursion outside 0–3.3 V and no ADC clipping during normal measurements. Results: Record minimum and maximum voltages and ADC codes; include oscilloscope captures of startup and power changes.
3. Response time: Following a 10 dB step in RF input power within the supported range, the calibrated detector reading shall settle within ± 1 dB of the final applied power within 10 ms.	Equipment: RF generator capable of triggered power steps, oscilloscope, and computer. Procedure: (1) Apply upward and downward 10 dB steps near the low, middle, and high portions of the supported range. (2) Trigger the oscilloscope from the generator's step signal and capture the detector output. (3) Use the calibration curve to determine when the output enters and remains within the specified error band. Results: Present representative response traces and a table of settling times.

2.2.3.3 Components

- Directional Coupler: DC2337J5020AHF
- Gain Block: TQP369184
- Log Power Detector: AD8319ACPZ-R7

2.2.3 Control Subsystem

2.2.4.1 Overview

This subsystem executes the anti-jamming algorithm and drives the analog control voltages. An ESP32-S3 MCU samples the logarithmic power detector voltage and executes a gradient descent search. The algorithm tunes the IQ control voltages on the modulator which adjusts the phase of one channel and observes the power change to see if it was favorable in improving jammer nulling. Through multiple iterations, the null will eventually settle on the exact jammer direction. A quad DAC is needed for the MCU to produce the control voltages. To achieve better than 1 degree of resolution, a >10bit DAC is needed. The MCU's internal ADCs will be used to read the power detector output.

Added programming and thresholding would ensure the algorithm tries not to null the friendly WiFi signal. It will also ensure outgoing TX packets do not disturb the control loop. Finally, a toggle switch will act as the user interface to toggle AJ or pass-through modes.

2.2.4.2 Requirements

This subsystem contributes to the high level requirements by executing the nulling algorithm and producing the control voltages to the receive RF chain subsystem.

- The DAC output voltage must support a range between at least 0 to 1 V
- The DAC must be >10 bits to maintain better than 1 degree of phase resolution of the modulator

Requirements	Verification
1. Analog control outputs: Each DAC channel used to drive the vector modulator shall support commanded voltages from 0 to 1 V, with measured output within ± 10 mV of the commanded value under the connected modulator load.	Equipment: DMM, regulated board supply, and computer running test firmware. Procedure: Power the control subsystem with the modulator connected. Command each DAC channel to 0, 0.25, 0.50, 0.75, and 1.00 V. Measure each output relative to board ground. Calculate measured-minus-commanded voltage and confirm its magnitude does not exceed 10mV. Results: Record commanded voltage, measured voltage, and error for every channel in a table.
2. Phase control: At the selected WiFi operating frequency, the control subsystem shall generate settings covering a complete 360° phase cycle, with no gap greater than 1° between adjacent achievable phase settings.	Equipment: Vector network analyzer with phase measurement, RF cables, and computer running a phase-sweep test. Procedure: (1) Calibrate the analyzer at the modulator's RF input and output reference planes. (2) Connect the modulator and apply the intended operating power. (3) Sweep the firmware's complete phase-control sequence while maintaining the intended modulation magnitude. (4) Record and unwrap measured phase, then calculate adjacent phase increments, including the wraparound interval. Results: Plot measured phase against commanded phase and report the largest gap. Record frequency and RF input power.
3. Automatic adaptation: Under a fixed, jammer-only test condition where a reference sweep demonstrates at least 20 dB suppression, the controller shall reach a detector-reported	Equipment: RF signal generator, splitter, attenuators, phase-adjustable RF paths, spectrum analyzer or RF power meter, and computer for logging.

power within 1 dB of the reference minimum within 5 seconds, starting from each of four initial phase settings: 0°, 90°, 180°, and 270°.	Procedure: (1) Apply two coherent jammer signals to the module's receive inputs at fixed levels and relative phase. (2) Sweep the available control settings to establish the reference minimum; verify suppression independently with the RF instrument. (3) Reset to each specified initial phase and enable adaptation. (4) Log elapsed time, detector readings, and DAC settings. (5) Confirm the controller reaches the stated power interval within 5 seconds for every start. Results: Plot measured power versus time and tabulate convergence time and final power error for each trial.
4. User mode control: Following a stable mode-switch input, the controller shall enter the requested AJ or pass-through control state within 100 ms. In pass-through mode, adaptive DAC updates shall stop and the designated pass-through settings shall be applied.	Equipment: Oscilloscope or logic analyzer, computer, and firmware status output. Procedure: (1) Monitor the mode-switch input, DAC communication lines, and a firmware mode-status signal. (2) Toggle between modes ten times. (3) Measure the interval between the stable switch input and completion of the requested state change. (4) Confirm adaptation stops in pass-through mode and resumes in AJ mode. Results: Record response times and observed state behavior in a pass/fail table.

2.2.4.3 Components

- MCU: ESP32-S3
- Quad 12-Bit DAC: MCP4728

2.2.5 Power Subsystem

2.2.5.1 Overview

The power subsystem powers the anti-jamming module from one 9V 2A DC adapter. It converts the output of a regulated 9 V DC wall adapter into the 5V and 3.3V supplies required by the anti-jamming module. An LM1086-5.0 low-dropout regulator (LDO) converts the 9V output to 5V to supply the RF vector modulator and associated analog circuitry. A second LDO, the TLV1117-33, converts the 5V rail to 3.3V for the ESP32-S3.

This architecture avoids introducing an onboard switching converter, reducing a potential source of switching interference near the sensitive RF and power-detection circuits. The LDOs provide additional

rejection of supply ripple from the wall adapter, while local bypass capacitors and bulk capacitance help reduce supply disturbances.

The PCB uses a continuous ground plane, with component placement and current-return paths arranged to limit coupling from the MCU and other digital circuitry into the RF and detector circuits. Input and output capacitors will meet each regulator's stability requirements, and regulator thermal performance will be verified at maximum load.

2.2.5.2 Requirements

This subsystem contributes to the first high level requirement by supplying stable power to the RF vector modulator, power detector, and control circuitry needed for adaptive jammer cancellation. It supports the second high-level requirement by reducing supply ripple and disturbances that could degrade receive-chain performance. The regulated 5 V and 3.3 V rails allow these subsystems to operate within their specified supply-voltage ranges.

- Distribute power from 9V, 2A adapter to the board.
- The 5V regulator shall maintain an output between 4.75V and 5.25V while supplying a combined load of up to 1.5A, including the current drawn by the downstream 3.3V regulator.
- The 3.3V regulator shall maintain an output between 3.135V and 3.465V while supplying up to 800mA to the ESP32-S3.

Requirements	Verification
1. With the regulated 9 V, 2 A adapter connected, the 5 V regulator shall maintain an output between 4.75 V and 5.25 V for combined output loads up to 1.5 A, including current drawn by the downstream 3.3 V regulator.	Equipment: 9 V adapter, two adjustable electronic loads, DMM, and current meter. Procedure: (1) Connect the adapter to the DC input jack. Connect one electronic load between 5 V and ground and the other between 3.3 V and ground. (2) Measure the 5 V regulator's total output current before the rail branches. (3) Test the combinations of direct 5 V loads of 0, 250, and 650 mA and 3.3 V loads of 0, 400, and 800 mA. (4) With the 3.3 V load at 800 mA, adjust the direct 5 V load until the measured total 5 V regulator output current reaches 1.5 A. (5) Measure the 5 V rail at every condition and confirm it remains within limits. Results: Record both load settings, total regulator output current, and measured voltage in a table.
2. The 3.3 V regulator shall maintain an output between 3.135 V and 3.465 V while supplying a total load from 0 to 800 mA to the ESP32-S3 and other 3.3 V circuitry.	Equipment: Use the same setup as Requirement 1. Procedure: (1) Measure the voltage between the 3.3 V regulator output and ground at each load combination listed above. (2) Include the condition with an 800 mA load on the 3.3 V rail and a combined 5 V regulator output current of 1.5 A. (3) Confirm the 3.3 V output remains within limits at every condition. Results: Add the measured 3.3 V voltage to the load-test table and

	mark each result as pass or fail.
3. Both regulators shall sustain simultaneous maximum loading without thermal shutdown or exceeding their datasheet-recommended operating junction temperatures, while maintaining the output-voltage limits above.	Equipment: The load-test setup above, thermocouples or a suitable temperature probe, and the selected regulator packages' thermal data. Procedure: (1) Set the 3.3 V load to 800 mA and adjust the direct 5 V load until the total 5 V regulator output current is 1.5 A. (2) Record ambient temperature, regulator temperatures, and both rail voltages once per minute. (3) Continue until regulator temperatures change by less than 1°C over five minutes; stop if temperatures approach the applicable limits. (4) Estimate junction temperatures using the measured temperatures and appropriate datasheet thermal parameters. Confirm that both regulators remain within their operating limits and both rails remain in regulation. Results: Present temperature-versus-time plots, maximum estimated junction temperatures, and the minimum and maximum rail voltages.

2.2.5.3 Components:

- LDO (5V): LM1086-5.0
- LDO (3.3V): TLV1117-33
- Regulated 9V, 2A DC wall adapter
- DC input connector, regulator input/output capacitors, and local bypass capacitors

2.3 Constraints and Tolerance Analysis

2.3.1 Systems Budgeting

System performance is constrained by phase control resolution and channel gain imbalance. A 12 bit 3.3V DAC used between 0 to 1 V yields a 0.3 degree phase resolution. And with an arbitrary worst case 0.5 dB of channel gain difference, a theoretical null depth of 25 dB is possible. Accounting for real-world effects, we will target a 20 dB null depth which corresponds to a 99% reduction in jammer power.

Implemented performance depends on the WiFi camera receiver's J/S tolerance. Assuming the camera can operate at <10 dB J/S, and the module provides a 20 dB null depth, the max tolerable J/S at the module input is +30 dB. This can be used to compute the theoretical performance against a far-field jammer. If the WiFi signal is hitting the antenna at -50 dBm, this means the system protects against up to

a -20 dBm jammer. This translates to a 1 W jammer positioned 10 feet away, which matches most real-world scenarios.

RF Chain Link Budget Using Selected Parts:

	Gain	NF	Gain Cascade	NF Cascade
LNA	21	1.4	21	1.4
Modulator	-8.6	14.9	12.4	2.089548623
Atten Pad	-12	10	0.4	3.295621718
Pin Diode	-0.4	0.4	0	3.470951357
Combiner	2.5	0	2.5	3.470951357
BPF	-2	2	0.5	4.070008997
Connector/Trace Estimate	-2	2	System Gain: -1.5	System Noise Figure: 4.877029021

2.3.2 Criterion For Success

At a high level, the module should mitigate an external jammer from overwhelming the camera's WiFi receiver by placing a spatial null of the radiation pattern in the direction of the jammer. In doing so, the system prevents saturation of the camera's LNA and maintains a signal/jammer ratio required for video streaming during the presence of external jamming. This performance shall be quantified by the measured null depth and the measured improvement in packet loss between jammed and unjammed conditions.

In the event one or more subsystems fail to work either by design or due to logistics, a reduced scope plan will be put in place. The same construction would be made out of an eval board of the modulator (AD8341-EVALZ), a discrete combiner, and coax cables which feed into a spectrum analyzer. Benchtop voltage power supplies would control the modulator. An external PC running MATLAB will interface with the equipment via GPIB, reading power levels and executing the gradient descent loop to demonstrate jammer suppression on the spectrum analyzer display.

2.3.3 Limitations

2.3.3.1 Friendly Signals

Total power is direction and content agnostic. A nearby AP, a neighbor's overlapping-channel WiFi, Bluetooth, or even a burst of the camera's own uplink traffic could out-power the jammer momentarily and get nulled instead. Evidently, configuring our anti-jammer to be just a blind power minimizer could easily null the camera's own AP if it's briefly the strongest thing in the room. We do intend on having additional programming and thresholding to identify and separate malicious signals, but it still runs a continuous risk of misidentifying good signals, thus destructively affecting our camera feed.

2.3.3.2 Wide-Band Jammers

Because the modulator applies a fixed phase shift to all frequencies rather than a true time delay, null depth degrades across the WiFi channel bandwidth meaning poorer performance toward the band edges. As a result, the AJ module would exhibit a reduced null depth against wide-band jammers.

2.3.3.3 Sympathetic Nulls

Sympathetic nulls are unintentional nulls created in the array pattern that can accidentally attenuate desired signals from the AP. To mitigate this risk, we suggest utilization of directional patch antennas. This configuration provides physical isolation against forward-facing jammers while significantly narrowing the angular sector where a sympathetic null could intersect the AP. However, spatial overlap risks remain depending on jammer geometry, necessitating further EM simulation to fully characterize these edge cases.

3. Cost and Schedule

3.1 Cost Analysis

3.1.1 Labor

Taking the average annual salary of a UIUC Electrical Engineer graduate starting salary during 2024-2025, (\$87,429), we estimate an hourly salary of \$42/hour.

≈ 350–420 hours, or roughly 115–140 hrs/person

3.1.2 Parts

Part	Part #	Manufacturer	Description	Quantity	Cost
Capacitors	/	/	/	32	\$3.20
Resistors	/	/	/	25	\$2.50
Inductors	/	/	/	7	\$0.70
PIN Diodes	NSVDP301M X2WT5G	onsemi	RF Power Divider 2.4 GHz ~ 2.5 GHz 0805 (2012 Metric), 6 PC Pad	2	\$0.62
2.4 GHz Power Divider	PD2425J5050 S2HF	TTM Technologies, Inc.	RF Power Divider 2.4 GHz ~ 2.5 GHz 0805 (2012 Metric), 6 PC Pad	1	\$0.91
RF Gain Block	TQP369184	Qorvo	RF Amplifier IC CATV, SATV 0Hz ~ 6GHz SOT-363	1	\$2.76

Logarithmic Detector	AD8319ACPZ-R7	Analog Devices Inc.	RF Detector IC RADAR, 802.11/WiFi, 8.2.16/WiMax, Wireless LAN 1MHz ~ 10GHz -60dBm ~ -2dBm ±1dB 8-VFDFN Exposed Pad, CSP	1	\$6.70
SMA Edge Connectors	CON-SMA-E DGE-S	RF Solutions	SMA Connector Jack, Female Socket 50 Ohms Board Edge, End Launch Solder	3	\$8.25
Micro-USB Connector	1050170001	Molex	CONN RCPT USB2.0 MICRO B SMD R/A	1	\$1.00
4-Pin Header	Conn_01x04_Pin	/	/	1	\$0.10
DC Barrel Jack	PJ-002A	Same Sky (Formerly CUI Devices)	Power Barrel Connector Jack 2.00mm ID (0.079"), 5.50mm OD (0.217") Through Hole, Right Angle	1	\$0.58
PTS645 Tactile Push Switches	SW_Push	/	/	2	\$0.20
Vector Modulator	AD8341ACPZ-REEL7	Analog Devices Inc.	RF Modulator IC 1.5GHz ~ 2.4GHz 24-VFQFN Exposed Pad, CSP	1	\$26.23
LNA	TSS-53LNB+	Mini-Circuits	RF Amplifier IC General Purpose 500MHz ~ 5GHz 12-MCLP (3x3)	1	\$4.59
2.4 GHz Balun Transformer	2450BL15B00 50001E	Johanson Technology Inc.	RF Balun 2.4GHz ~ 2.5GHz 50 / 50Ohm 0805 (2012 Metric)	1	\$0.40
2.4 GHz Bandpass Filter	2450BP08A01 00001T	Johanson Technology Inc.	2.45GHz Frequency Band Pass RF Filter (Radio Frequency) 100MHz Bandwidth 1dB 5-SMD, No Lead	1	\$1.12
Directional Coupler	DC2337J5020 AHF	TTM Technologies, Inc.	RF Directional Coupler General Purpose 2.3GHz ~ 3.7GHz 21.3dB 2W 0805 (2012 Metric)	1	\$1.32
3.3V LDO Regulator	TLV1117-33	Texas Instruments	Linear Voltage Regulator IC Positive Fixed 1 Output	1	\$0.46

			800mA SOT-223-4		
Quad 12-Bit I2C DAC	MCP4728	Microchip Technology	12 Bit Digital to Analog Converter 4 10-MSOP	1	\$2.50
5.0V LDO Regulator	LM1086-5.0	Texas Instruments	1.5-A, 29-V, linear voltage regulator KTT 3 -40 to 125	1	\$3.55
MCU Module	ESP32-S3-WR OOM-1	Espressif Systems	Bluetooth, WiFi 802.11b/g/n, Bluetooth v5.0 Transceiver Module 2.4GHz PCB Trace Surface Mount	1	\$5.21
ESD Protection Diode IC	USBL6-2SC 6	STMicroelectronics	17V Clamp 5A (8/20 μ s) Ipp Tvs Diode Surface Mount SOT-23-6	1	\$0.54

Total parts sum = \$73.44

3.1.3 Total Cost

3.2 Schedule

All planned tasks will be attempted together and completed based on the schedule and availability of each member. But each member will be present and work on every task.

Week	Dates	Course Deadlines	Planned Tasks
6	Mon 10/12 – Fri 10/16	Breadboard Demo (Mon-Wed); Teamwork Eval 1 due Thu; 3rd PCBway round due Fri; last day for machine shop revisions Fri	Demonstrate closed-loop nulling on the bench with measurable jammer suppression.
7	Mon 10/19 – Fri 10/23	No calendar deadlines this week.	Assemble and debug delivered PCBs. Refine control-loop step size, stopping criteria, and detector measurements. Verify power-rail stability and regulator temperatures.
8	Mon 10/26 – Fri 10/30	4th JLCPCB round due Fri, 4:45p	Transfer the validated bench design to the custom PCB. Test RF protection circuitry and submit any necessary PCB revisions before the deadline.
9	Mon 11/2 – Fri 11/6	Progress Demo (Mon-Wed); Individual progress reports due Thu	Demonstrate repeatable cancellation on the custom PCB, targeting at least 20 dB under defined test conditions. Record

			results across multiple phase offsets or jammer geometries.
10	Mon 11/9 – Fri 11/13	Team Contract assessment due	Integrate the module with the WiFi camera. Verify bidirectional communication and compare streaming performance with cancellation enabled and disabled.
11	Mon 11/16 – Fri 11/20	Mock demo (Mon-Thu); Mock Presentation (Thu/Fri)	Rehearse the complete demonstration. Complete subsystem verification, document remaining issues, and correct hardware and firmware problems.
12	Mon 11/23 – Fri 11/27	Fall Break	Reserve contingency time for remaining troubleshooting and report preparation, subject to team and laboratory availability.
13	Mon 11/30 – Fri 12/4	Final Demo (Mon-Wed); Final Presentation (Thu/Fri)	Freeze features, complete final checks, and demonstrate measured performance. Present results and clearly identify any unmet requirements.
14	Mon 12/7 – Thu 12/10	Judging Mon; Pitched Reviews Tue; Final paper due Wed 12/9; Lab checkout + notebook due Thu	Submit the final report, complete laboratory notebooks, return borrowed equipment, and finish lab checkout.

4. Ethics, Safety and Societal Impact

To ensure FCC compliance during testing, verification will take place on a cabled benchtop setup using RF signal generators. A signal generator will generate a CW jammer tone at the camera's WiFi channel frequency. This signal will pass through an RF splitter into two coax paths with calibrated phase (length) offsets. The WiFi signal is then embedded into each of these channels using standard 2.4 GHz antennas and combiners. Finally, each channel is fed into the module's inputs.

Initially, this composite signal will be injected into the camera without the AJ module in order to characterize the jammer/signal ratio where video streaming fails. Once established, the module will be installed. Success is demonstrating a ~20 dB improvement in jammer power tolerance while maintaining a continuous video stream. With measured null-depth, the theoretical over-the-air performance could be calculated with FSPL equations.

In terms of the societal impact, the problem statement for our project leans on increasing public-safety by making it more difficult for burglars to disable cameras before break-ins. Even though this is a valid motivation for developing our device, it raises an obligation under IEEE's honesty/realism canon and

ACM's "comprehensive and thorough evaluation, including possible risks" principle: don't let the framing imply more protection than the device delivers.

Concretely, our prototype nulls one jammer, in a known/bounded geometry, up to a specific dynamic range, with a single spatial degree of freedom. A real attacker could use multiple jammers, move during the attack, or use power levels outside your tested range. If this project is ever pitched as a consumer safety product (even hypothetically in your report's future-work section), it's worth explicitly flagging that a "jammer-resistant" claim could give homeowners false confidence and cause them to skip other precautions (monitored alarms, etc.), which could possibly even leave them in a less protected state.

5. Citations

1. Analog Devices. *AD8319: 1 MHz to 10 GHz, 40 dB Logarithmic Detector/Controller*. Data sheet, 2019.
2. Analog Devices. *AD8341: 50 MHz to 2.8 GHz Vector Modulator*. Data sheet, 2016.
3. Analog Devices. *AN-1040: Topics in RF Power Measurement*. Application note, 2009.
4. Balanis, Constantine A. *Antenna Theory: Analysis and Design*. 4th ed., John Wiley & Sons, 2016.
5. IEEE. *IEEE Standard for Information Technology—Part 11: Wireless LAN MAC and PHY Specifications*. IEEE Std 802.11-2020, IEEE, 2021.
6. Murata Manufacturing. *SAFEA2G45MA0F0A: 2.4 GHz SAW Filter*. Data sheet, 2020.
7. Skyworks Solutions. *CLA4605-000: Silicon Limiter Diodes*. Data sheet, 2015.
8. Widrow, Bernard, et al. "Adaptive Antenna Systems." *Proceedings of the IEEE*, vol. 55, no. 12, Dec. 1967, pp. 2143–2159.