

ECE 445 Design Document—RF

Front-End Team Plan

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ECE 445 - Senior Design
Fall 2026

TA: Shiyuan Duan

September 2026

Team Number: 5

Team roster and ownership

Xinyang Liu — RF architecture and excitation

Teammate 2 — receiver and measurement chain

Tian Tu — verification and report integration

Teammate 1 — RF architecture and excitation

Own the problem/solution context and the system-in-use visual aid (show how the instrument connects to the device under test; keep this distinct from the internal block diagram). Draft 3–4 complete, objective high-level requirements with quantitative targets where supported. Produce the modular block diagram and explain the RF source/clock and Port 1 bridge design, their role in S11, design choices, quantitative interfaces, and evidence. Confirm whether the 26 MHz TCXO and Si5351A configuration are current design choices; document verified frequencies, levels, and interfaces.

Deliver to the team: editable diagram(s), section text with citations, verified source/datasheet references, and open questions about the selected project scope.

Teammate 2 — receiver and measurement chain

Own the reference and reflection receiver plus codec/input interface descriptions. Trace the signal path for incident/reference and reflected signals, explain how the outputs support S11 measurement, and define interfaces between the bridge, receiver stages, and acquisition/codec. Provide schematics or annotated figures, quantitative design requirements, design justifications, component values/part numbers, and supporting calculations or simulation results. Identify the most feasibility-critical subsystem/interface and draft a tolerance analysis grounded in actual values.

Deliver to the team: subsystem sections, interface table or clearly stated interfaces, figures/simulation/calculation evidence, candidate BOM entries with source links, and a reproducible verification procedure with pass criteria.

Teammate 3 — verification, cost, safety, and integration

Own the consolidated Requirements and Verifications table and ensure each test has setup, equipment or reference, procedure, measured quantity, tolerance, and pass/fail criterion. Coordinate with Teammates 1 and 2 to make subsystem requirements specific to student-designed blocks rather than merely copying off-the-shelf datasheet specifications. Build the parts/labor cost analysis and the week-by-week schedule with one task and a named member each week. Draft applicable societal impact, engineering standards, ethics, and electrical/lab safety considerations and mitigation procedures. Assemble IEEE-style citations and references, check figure/table captions and equations, export the final PDF, upload it to PACE, and submit the required website URL.

Deliver to the team: consolidated R&V table, cost/BOM with manufacturer, part number, quantity, cost and purchase link, labor estimate, schedule, impact/ethics/safety section, final PDF, and submission confirmation.

1. Introduction

a. Problem and Solution

An RF device does not always absorb all the energy incident on its input. An impedance mismatch reflects part of that energy, and the response can change with frequency. At Port 1, the complex reflection coefficient is $S_{11} = b_1/a_1$, where a_1 is the incident-wave reference and b_1 is the reflected-wave response. A frequency sweep of this ratio can characterize a device under test (DUT). Our design uses the Port 1 S_{11} path of a NanoVNA-derived RF front-end PCB. A programmable RF source drives a resistive bridge connected to the DUT at X1. Separate reference and reflection receivers translate the sampled RF signals to an

intermediate frequency (IF), and a dual-channel codec digitizes them. An external MCU will configure the source and codec, acquire paired samples, apply calibration, and calculate S11. The Rev A1 PCB also retains an X2 transmission branch, but the requirements in this section focus on X1. The PCB and Gerbers are engineering-review artifacts; calibrated accuracy has not yet been demonstrated.

b. Visual Aid

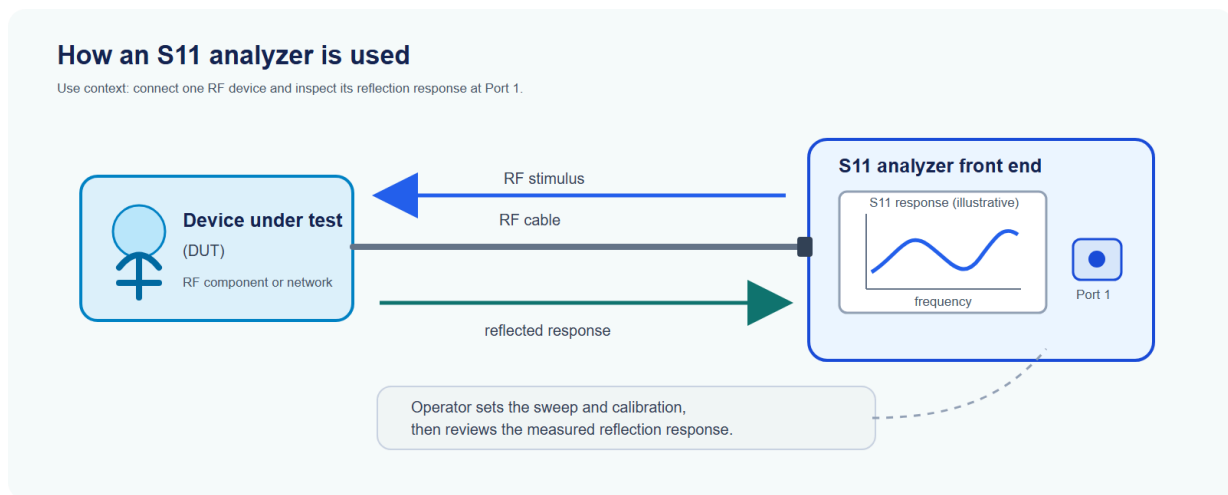


Figure 1. Intended S11 use context. The operator connects the DUT to X1, sets a sweep and calibration through an external MCU and host, and views the calculated reflection response. The RF front-end PCB supplies the stimulus and samples the returned signal. The MCU, host, and DUT are external to this board

c. High-Level Requirements

HLR-1 — Frequency sweep. The proposed operating band is 12.54–14.58 MHz, centered on 13.56 MHz. With X1 terminated in 50 Ω , the system shall generate 101 commanded frequency points in order, including both endpoints, with measured RF frequency within ± 1 kHz of the command and output level between

–30 and 0 dBm at every point. A calibrated spectrum analyzer and a 50 Ω termination will verify this requirement.

HLR-2 — Paired acquisition. At each of the 101 commanded points, after at least 20 ms of settling, the system shall acquire at least 1024 valid reference/reflection sample pairs at a proposed codec rate of 48 ksample/s and fixed gain. Across ten consecutive sweeps, no point or channel pair may be missing or invalid. MCU logs of frame counts, channel identities, and timestamps will verify this requirement.

HLR-3 — Calibrated S11. After open/short/load calibration at the X1 reference plane, the system shall report complex S11 at all 101 points from 12.54 to 14.58 MHz. On an independent verification load whose reference-VNA measurement has $|S_{11}| \geq 0.2$, the absolute difference in linear S11 magnitude shall be ≤ 0.10 and the phase difference shall be $\leq 15^\circ$ at every point. A calibrated reference VNA, using the same cables, frequency grid, and reference plane, will verify this requirement.

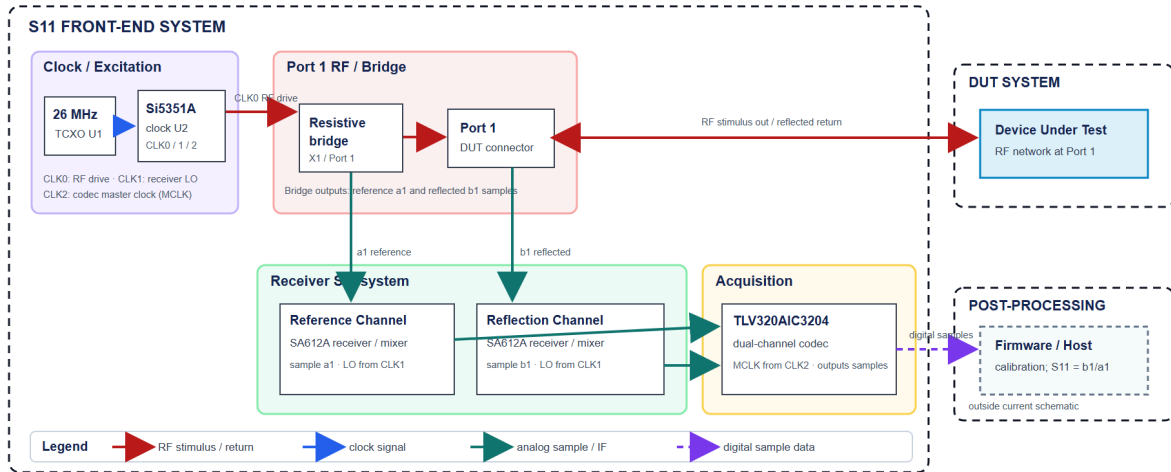
These are proposed design acceptance targets. They have not been demonstrated on assembled hardware.

2. Design

a. Block Diagram

S11 Reflection Front-End Block Diagram

Grouped by subsystem; the dashed boundary marks hardware represented in the current S11 schematic.



S11-only scope intentionally omits X2 and the transmission receiver. Verify component values, electrical levels, and calibration performance before claiming final specifications.

Figure 2. Rev A1 RF front-end architecture. U1 provides the 26 MHz reference for clock generator U3. U3 CLK1 drives the Port 1 bridge, CLK0 provides the receiver local oscillator, and CLK2 supplies the codec master clock. The bridge and X1 provide reference and reflected samples for U7 and U8. The PCB also includes X2 and U9 for transmission measurements. Codec U4 digitizes a selected pair of receiver channels and sends samples through J2 to an external MCU. The MCU configures U3 and U4 over I2C and receives samples over I2S. The S11 requirements above cover the X1 reference/reflection path.

U1 is a nominal 26 MHz voltage-controlled temperature-compensated oscillator that supplies the reference for Si5351A clock generator U3. Under the intended firmware configuration, U3 CLK1 supplies RF excitation to the Port 1 bridge, CLK0 supplies the receiver local oscillator, and CLK2 supplies an 8 MHz master clock to codec U4 [2], [4]. The bridge applies the stimulus to X1 and forms separate reference and reflection signals. U7 and U8 mix those signals with the

common local oscillator before codec acquisition. The programmed frequencies set the IF according to $f_{IF} = |f_{RF} - f_{LO}|$ [1].

b. Circuit Design and Component Selection

The Rev A1 PCB retains the Port 1 resistive bridge with nominal arm values including 49.9 Ω , 82 Ω , and 390 Ω . R25 is retained as an unpopulated option. The revised schematic repairs disconnected balancing-arm and reference-sample paths in the earlier recreation. U3 is a 10-MSOP Si5351A-B-GT. The PCB also provides local clock decoupling, an oscillator tuning bias, and a 3.3 V supply. The current four-pad oscillator candidate for U1 is end-of-life, so an available replacement with a verified pinout and footprint must be selected before fabrication. Bridge match and local-oscillator amplitude have not yet been established by measurement.

c. Interfaces and Supporting Calculations

For the proposed single-point receiver test, $f_{RF} = 13.560$ MHz and $f_{LO} = 13.565$ MHz, giving an expected IF of 5 kHz. This is a test configuration, not a claim that every sweep point has been verified. The external MCU programs U3 and U4 through 3.3 V I2C signals on J2; U4 returns digitized samples over I2S. The source output level, bridge impedance, reference/reflection isolation, local-oscillator amplitude, IF level, and calibration error must be calculated or measured with the final components.

d. Reference Receiver

Function and Signal Path

The reference receiver measures a sample of the RF signal sent toward the DUT. This gives the system a reference for comparing the amplitude and phase of the reflected signal and calculating calibrated S11. A mixer combines this sample with the local oscillator (LO) to produce a lower-frequency signal that the codec can digitize [1]:

$$\underline{IF\ frequency = |RF\ frequency - LO\ frequency|}$$

The reference sample enters the mixer through a 100 nF coupling capacitor, while the other RF input is connected to AC ground through another 100 nF capacitor. The LO also enters through a 100 nF coupling capacitor. Both mixer outputs pass through low-pass filters, each consisting of a 15 k Ω series resistor and a 1 nF capacitor to ground. Two additional 100 nF capacitors block the DC bias before the signals reach the codec's IN2_L and IN2_R inputs [3]. Section 2.g describes how these inputs are configured for acquisition.

Circuit Design and Component Selection

The mixer uses the shared LO so both receivers translate their signals to the same IF. The 100 nF input capacitors pass the RF and LO signals while preserving the mixer's internal DC bias [1].

The 15 k Ω resistors and 1 nF capacitors form low-pass filters to reduce unwanted mixing products. Both output branches use the same nominal values to limit differences in their frequency responses. The 100 nF output capacitors separate

the mixer and codec DC bias levels. Filter bandwidth and codec loading are evaluated in the “Interfaces and Supporting Calculations” subsection below.

Interfaces and Supporting Calculations

Interface	Connection and design details
RF input	REF_TAP connects to mixer pin 1 through 100 nF; pin 2 is AC-grounded through 100 nF.
LO input	Mixer pin 6 receives the shared LO through 100 nF. The recommended input level is 200–300 mV peak-to-peak [1].
Codec input	Both filtered outputs are AC-coupled through 100 nF to IN2_L and IN2_R. Signal levels must remain within the codec’s configured input range [3].

For each 15 kΩ / 1 nF filter, the ideal cutoff frequency is:

$$\textit{Cutoff frequency} = 1 / (2\pi RC) \approx 10.6 \textit{ kHz}$$

Including the mixer’s approximately 1.5 kΩ output resistance [1] gives about 9.6 kHz, assuming negligible codec loading. These are calculated estimates. The selected codec input impedance and coupling capacitors also affect the response, so the final IF and signal levels must be checked with the codec configuration used for acquisition.

Reference receiver and IF filter

Named global nets connect across pages. X = intentionally unconnected pin.

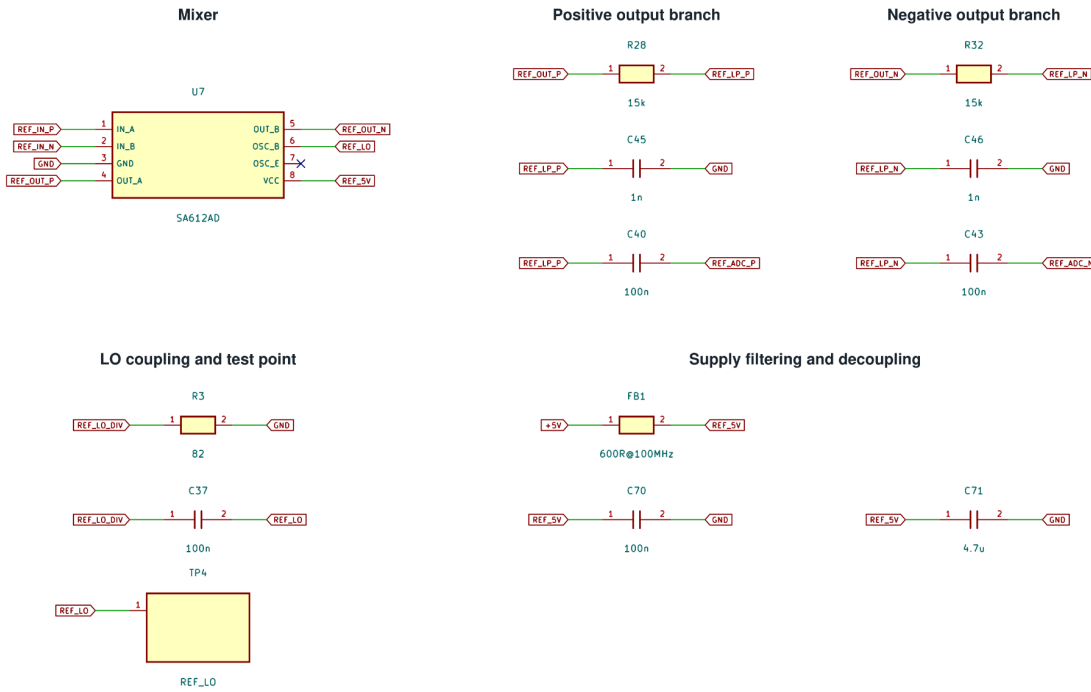


Figure 3. Reference receiver circuit.

e. Reflection Receiver

Function and Signal Path

The reflection receiver measures the bridge signal associated with reflections from the DUT. Its mixer uses the same LO as the reference receiver to produce the same IF [1]. Comparing the two acquired signals provides the amplitude and phase information needed for calibrated S11.

Both bridge outputs enter the mixer through 100 nF coupling capacitors. The mixer outputs then pass through matching 15 k Ω / 1 nF low-pass filters and 100 nF output coupling capacitors. The filtered signals connect to the codec's IN3

inputs [3]. In the current schematic, REFL_ADC_N connects to IN3_L, while REFL_ADC_P connects to IN3_R. This polarity must be accounted for when configuring the codec and calculating phase.

Circuit Design and Component Selection

Both bridge nodes are AC-coupled to the mixer’s differential inputs, preserving the bridge voltage difference without changing the mixer’s internal bias [1]. The output filters use the same nominal values as the reference channel to limit differences in amplitude and phase response. The mixer’s nominal 5 V supply is filtered through a ferrite bead and decoupled with 100 nF and 4.7 μ F capacitors to reduce supply noise. Verification must check both strong reflections for clipping and weak reflections against the receiver noise floor.

Interfaces and Supporting Calculations

Interface	Connection and design details
Bridge input	REFL_TAP_P and REFL_TAP_N connect to mixer pins 1 and 2 through separate 100 nF capacitors.
LO input	Pin 6 receives the shared LO through 100 nF; the recommended level is 200–300 mV peak-to-peak [1].
Codec input	REFL_ADC_N connects to IN3_L (pin 20); REFL_ADC_P connects to IN3_R (pin 21) [3].

The output filters have the same estimated cutoff as the reference channel: 10.6 kHz ideally, or approximately 9.6 kHz when mixer output resistance is included and codec loading is neglected. For a first-order low-pass filter:

$$\text{Phase shift} = -\arctan(\text{IF frequency} / \text{cutoff frequency})$$

Differences in component values can therefore produce unequal phase shifts between the two receivers. Section 2.i evaluates this mismatch; the complete response also depends on codec loading and coupling capacitors.

Reflection receiver and IF filter

Named global nets connect across pages. X = intentionally unconnected pin.

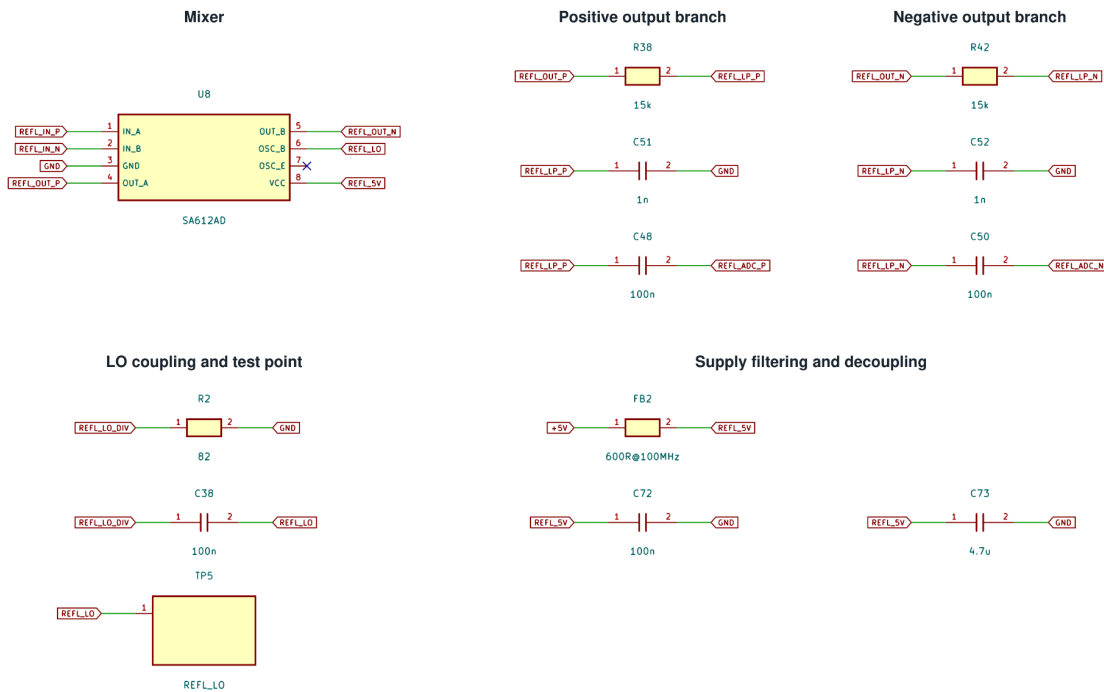


Figure 4. Reflection receiver circuit.

f. Codec and Acquisition Interface

Input Connections and Channel Selection

The codec will be configured to acquire the reference and reflection signals as two differential channels. Its programmable input routing allows the following assignments [4]:

ADC channel	Positive input	Negative input
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Left: reference	IN2_L — REF_ADC_P	IN2_R — REF_ADC_N
Right: reflection	IN3_R — REFL_ADC_P	IN3_L — REFL_ADC_N

Both ADCs use the same sampling clock, providing paired samples for amplitude and phase comparison. Unused input routes will be disabled. This configuration preserves the P-minus-N polarity of both receivers; IN3_L and IN3_R together form the right ADC's differential input [4].

Sampling and Clock Configuration

Parameter	Proposed setting
Codec master clock (MCLK)	8 MHz from the clock generator
Sampling rate	48 ksample/s per channel
Data format	I2S, 16-bit samples, two channels
Clock roles	Codec supplies BCLK/WCLK; MCU receives as slave
Frame length	32 bit clocks, giving BCLK = 1.536 MHz

The codec's PLL and clock dividers must be programmed to obtain 48 ksample/s from the 8 MHz input [4]. The resulting Nyquist frequency is 24 kHz, but the receiver filters further limit the usable IF bandwidth. Both channels will use fixed gain during calibration and measurement, with automatic gain control disabled. Clock rates and frame timing will be verified before RF measurements.

MCU Interface

An external MCU connects through J2 using 3.3 V logic. It configures the codec over I2C at the 7-bit address 0x18 [4]. Both I2C lines have 2.2 k Ω pull-up resistors to 3.3 V.

J2 pin	Signal	Function
3 / 5	SCL / SDA	Codec register control
7 / 9	BCLK / WCLK	Codec-generated clocks received by MCU
11	DOUT	Stereo sample data from codec to MCU
14	RESET_N	Active-low codec reset
1, 4, 6, 8, 10, 12	GND	Shared ground

The MCU will receive the I2S stream through DMA and separate each frame into reference and reflection samples. Samples collected during frequency changes will be discarded until the signal settles. J2 pin 13 connects to codec DIN and is not required for acquisition-only operation.

Codec and acquisition interface

Named global nets connect across pages. X = intentionally unconnected pin.

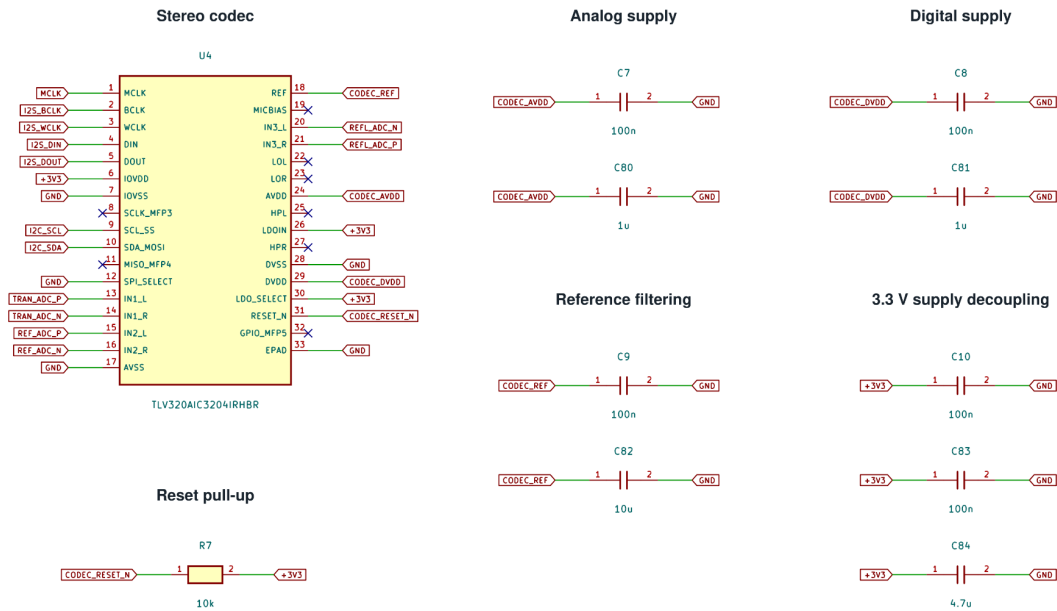


Figure 5. Codec and acquisition interface circuit.

g. Requirements and Verifications

The following requirements are proposed acceptance targets. Receiver tests use RF = 13.560 MHz, LO = 13.565 MHz, and fixed codec gain with automatic gain control disabled.

For receiver testing, disconnect the bridge and use an RF generator, splitter, and balun to drive the reference input single-ended and the reflection input differentially. Set each receiver input to 10 mV RMS, measured across its RF input terminals.

Subsystem	Requirement	Verification
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Receivers (signal quality)	Both channels shall produce a 5.00 kHz ± 50 Hz IF, with a fitted-tone-to-residual ratio of at least 30 dB.	Record 4,800 paired samples at 48 ksample/s. Fit a sinusoid to each channel and calculate its frequency and $20 \log_{10}(\text{tone RMS} / \text{residual RMS})$. Pass if both channels meet both limits.
Receivers (repeatability)	With unchanged inputs, the reflection/reference amplitude ratio and phase difference shall vary by no more than 0.2 dB and 2° , respectively, over ten captures.	Collect ten 4,800-pair records using the same setup. Calculate the complex reflection/reference ratio for each record. Pass if the maximum-minus-minimum amplitude and unwrapped phase stay within the limits.
Codec clocks	WCLK shall be 48 kHz $\pm 0.1\%$, and BCLK shall be 1.536 MHz $\pm 0.1\%$, with 32 bit clocks per stereo frame.	Measure BCLK and WCLK with a logic analyzer or oscilloscope. Decode the I2S stream and confirm two 16-bit samples per frame. Pass if clock rates and frame timing meet the stated requirements.
Codec / MCU	The MCU shall identify both channels correctly and receive data continuously for ten seconds without reported overruns.	Apply a tone to one receiver at a time and confirm its assigned channel. Compare a short logic-analyzer capture of codec DOUT with the corresponding MCU samples. Run acquisition for ten seconds and check DMA and I2S error flags. Pass if channel assignments and decoded values agree and no overruns occur.

These tests verify receiver operation, repeatability, and acquisition at one RF frequency. Calibrated S11 accuracy across the operating band requires separate system-level testing.

h. Tolerance Analysis

The receiver output filters affect the amplitude and phase used to calculate S11. This analysis uses the nominal 15 kΩ / 1 nF values and assumes ±1% resistor and ±5% capacitor tolerances. These tolerances must be confirmed when ordering parts. For each filter:

$$\text{Cutoff frequency} = 1 / (2\pi RC)$$

$$\text{Phase shift} = -\arctan(\text{IF frequency} / \text{cutoff frequency})$$

At the proposed 5 kHz IF, the calculated results are:

Condition	Cutoff frequency	Gain	Phase shift
Nominal values	10.61 kHz	−0.87 dB	−25.23°
Minimum R and C	11.28 kHz	−0.78 dB	−23.90°
Maximum R and C	10.00 kHz	−0.97 dB	−26.55°

If the two receivers have opposite tolerance extremes, their filters can differ by approximately 0.19 dB and 2.65°. Equal nominal component values therefore do not guarantee equal channel responses.

These differences represent fixed channel offsets, while Section 2.h tests capture-to-capture repeatability. Calibration must account for stable offsets using the same IF and gain settings as measurement.

This simplified calculation excludes mixer output resistance, codec loading, and coupling capacitors. The complete response must also be measured with the selected codec configuration before confirming measurement accuracy.

3. Cost and Schedule

Design BOM and costing basis

This estimate covers one assembled RF front-end prototype plus purchased spares. Component quantities follow the Rev A1 design package [13]. Capacitor footprints and the replacement 26 MHz oscillator are assumed compatible with the final PCB for this budget, as specified for the planning scenario; this assumption is not a completed footprint or electrical verification. The board has 106 footprints, including four mounting holes, six test pads and the unpopulated R25, so footprint count is not purchased-part count.

Component / manufacturer or source	Design quantity and identification	Cost treatment
Clock generator, Skyworks	U3, Si5351A-B-GT; 1	Historical purchase below
Stereo codec, Texas Instruments	U4, TLV320AIC3204IRHBR; 1	Historical purchase below
Mixer, NXP	U7/U8/U9, SA612AD; 3	Historical five-piece pack below
Oscillator, FTS replacement candidate	U1; 7Q-26.000MBS-T, 26 MHz; 1	Historical purchase plus substitution reserve
Regulator, Texas Instruments	U10, TLV75533PDBVR; 1	\$4 allowance for two including spare

SMA connectors	X1/X2; 2; Amphenol 132289 design footprint	Historical generic connector pack; assumed final-board fit
Capacitors	30×100 nF, 6×1 nF, 3×1 μ F (0603); 6×4.7 μ F, 2×10 μ F (0805)	Kits plus supplementary passive allowance; final vendor MPNs unselected
Resistors, 0603	$4 \times 82 \Omega$; 3×1 k Ω ; 2×10 k Ω ; 1 each of 150 Ω , 470 Ω , 56 Ω , 27 Ω , 100 Ω , 22 Ω , 12 k Ω , 33 Ω ; $5 \times 49.9 \Omega$; 6×15 k Ω ; 2 each of 390 Ω , 39 Ω , 2.2 k Ω ; R25 DNP	Kits plus supplement; final vendor MPNs unselected
Ferrite beads	$3 \times 600 \Omega$ at 100 MHz	\$6 for six including spares; final MPN unselected
Headers	J1 power, J2 2×8 control, one each	\$10 lot with mating connections; final MPNs unselected
PCB, controller and fixtures	One 90×65 mm, 1.6 mm, four-layer assembled board; external controller and bench fixtures	Allowances detailed below

Historical purchase prices — September 30, 2026

The following prices and package quantities come from the supplied purchasing summary. Prices and stock have not been rechecked. The baseline includes two packs of each of the first four products (original order plus proposed spare purchase), and one pack of each remaining product. Reported original-order submission is not a receipt or delivery record.

Product / purchase link	Quantity per pack	Budgeted packs	Price per pack	Extended cost

Si5351A-B-GTR	1	2	\$4.00	\$8.00
SA612A / SA612AD	5	2	\$9.34	\$18.68
TLV320AIC3204IRHBR	1	2	\$3.99	\$7.98
SMA board-edge connectors	10 per listing	2	\$7.79	\$15.58
7Q-26.000MBS-T	1	1	\$0.86	\$0.86
0603 1% resistor assortment	170 values × 50	1	\$29.99	\$29.99
0805 capacitor assortment	92 values × 25	1	\$39.99	\$39.99
0603 49.9 Ω 1% resistors	100	1	\$0.46	\$0.46
0805 100 nF, 50 V, X7R capacitors	100	1	\$6.38	\$6.38
Total merchandise	Includes surplus inventory			\$127.92

The original four-item order is \$25.12; all proposed pending purchases total \$102.80. Separate reported shipping charges total 26.60(15 + \$10.60 + \$1). The 49.9 Ω pack price and power rating need supplier confirmation before purchase; the report retains the supplied historical amount as an estimate. Exact passive ordering codes, component ratings and substitutes must be

reconciled to the assembly BOM. Package purchases exceed one board's installed quantity and are not a production unit cost.

Labor and Total Cost

This planning estimate assumes one assembled functional RF front end and a spare set of the principal ICs, using the original-plus-pending merchandise scenario above. Purchasing minimum PCB quantities may provide additional bare boards; assembling a second complete unit is outside this baseline. The September 30 merchandise prices are historical user-supplied estimates.

Additional lines below are engineering budget allowances, not supplier quotations or purchase commitments. They are incremental to the \$127.92 merchandise scenario and must not be added twice.

Labor

Use a student-project salary assumption of \$25/hour and the course overhead factor of 2.5 [5], giving \$62.50 per person-hour. Estimate 60 hours per member for the complete project, including design/report preparation, assembly or software integration, testing, debugging and final documentation. This is an equal-effort planning allowance, approximately 6 hours/week for the ten-week plan, not an actual time record.

Member	Planning allocation of 60 hours	Loaded labor cost
Xinyang Liu	20 h architecture/PCB; 10 h review/documentation; 10 h procurement/assembly; 15 h integration/debug; 5 h final demonstration/report	$\$25 \times 2.5 \times 60 = \$3,750$

Yanheng Zhuang	20 h receiver/codec design; 10 h analysis/documentation; 10 h acquisition integration; 15 h testing/debug; 5 h final demonstration/report	$\$25 \times 2.5 \times 60 = \$3,750$
Tian Tu	15 h verification planning/report integration; 10 h costing/schedule/documentation; 15 h calibration/test execution; 15 h analysis/regression; 5 h final demonstration/report	$\$25 \times 2.5 \times 60 = \$3,750$
Total	180 person-hours	\$11,250

Parts, Services and Equipment Budget

The design BOM and historical purchase table above identify known components and purchase links. The allowances below complete a project-level budget without asserting unverified supplier prices. Exact passive MPNs and approved substitutes still need to be reconciled to the BOM before ordering.

Cost item	Quantity / basis	Budget
Listed merchandise including main-IC/connector spare packs	Original \$25.12 plus pending \$102.80; includes kits and proposed oscillator	\$127.92
Reported separate shipping	Three charges, counted once: \$15 + \$10.60 + \$1	\$26.60
U10 regulator	TI TLV75533PDBVR, 2 pieces including one spare; assumed \$2 each	\$4.00
Ferrite beads	6 pieces for 3 installed positions plus spares; assumed \$1 each; exact MPN pending	\$6.00

Power/control headers and mating connectors	One project lot for J1/J2 and mating connections; MPNs pending	\$10.00
Correct-footprint passive parts	One supplementary lot for missing values/0603 capacitors and tolerance requirements; incremental to the candidate kits	\$25.00
Approved oscillator replacement reserve	One incremental allowance if the \$0.86 candidate cannot be used; unused reserve is removed later	\$10.00
Four-layer PCB fabrication	One small prototype order, one revision; 90 × 65 mm nominal board; vendor/quantity to be quoted	\$60.00
Assembly consumables and mechanical protection	One lot: solder/flux, standoffs and simple insulating support	\$15.00
External controller	One development-board allowance; final controller selection pending	\$30.00
Coax cables and adapters	One project lot for bench connections	\$25.00
Calibration and verification fixtures	One project lot of connector standards/loads; characterize using the borrowed reference VNA	\$30.00
Other shipping reserve	Incremental shipments beyond the three known fees	\$20.00
Tax reserve	Budget allowance, not a calculated tax rate or tax determination	\$30.00
Laboratory instruments and shop services	Assume existing lab access to VNA, spectrum analyzer, scope/logic analyzer, RF generator, supply and soldering equipment: \$0 incremental rental; no paid shop work, 0 shop hours	\$0.00

Base non-labor budget	Sum of the above	\$419.52
Contingency	15% of \$419.52, rounded to cents; price changes, rework and minor omissions	\$62.93
Planned non-labor total	Base plus contingency	\$482.45

The laboratory-equipment line assumes borrowed access; it does not assert that reservations have been made. If paid instrument access, a complete second assembled unit, professional assembly or a substantial PCB redesign is required, revise this budget. Kit purchase costs include inventory and spares and therefore are not a per-board production cost. The contingency is a reserve rather than an expense already incurred.

Grand Total

Estimated project economic cost = \$11,250 labor + \$419.52 base non-labor = \$11,669.52.

Including the \$62.93 contingency gives a planned grand total of \$11,732.45. The corresponding non-labor procurement planning envelope is approximately \$500; this is a planning figure, not confirmation of course funding or authorization to purchase. No actual wage payment is implied by the course labor estimate.

Schedule

The following schedule is the report's proposed work allocation as of October 2, 2026. Xinyang Liu leads RF source/bridge and board work; Yanheng Zhuang is assigned receiver and acquisition work for planning; Tian Tu leads verification, costing and report integration. These

are proposed assignments; completion will be recorded during implementation. Each week has a lead and a deliverable. Fabrication delays and official course dates may require adjustment.

Week beginning	Proposed lead	Task and completion evidence
Sep 28	Tian Tu	Integrate the Design Document contribution. Resolve TBDs with module owners; produce a checked team PDF and record the actual submission receipt.
Oct 5	Xinyang Liu	Close source/bridge design questions after review. Deliver revised schematic, clock/interface table and justified quantitative targets.
Oct 12	Yanheng Zhuang	Validate receiver and acquisition interfaces. Deliver calculations or bench traces showing supported levels, bias and IF range.
Oct 19	Xinyang Liu	Complete board bring-up when fabrication and delivery allow. Record inspection, supply checks and source/bridge unit-test results.
Oct 26	Yanheng Zhuang	Integrate paired acquisition with the receiver. Deliver raw paired data and a SYS-2 completeness report.
Nov 2	Tian Tu	Coordinate calibrated comparison tests once the power, source, receiver and acquisition checks are ready. Archive reference and prototype data and a SYS-3 report.
Nov 9	Yanheng Zhuang	Investigate failed requirements and implement agreed fixes. Deliver revision notes and rerun affected tests.
Nov 16	Tian Tu	Run repeatability and full regression with module owners. Deliver repeatability results and a traceable evidence index.

Nov 23	Xinyang Liu	Hold a recovery/documentation buffer; confirm holiday and lab availability. Close remaining issues or document justified scope limits.
Nov 30	Tian Tu	Prepare the final demonstration and report package to the verified course dates. Reconcile costs, results, citations and submission records.

Each named lead coordinates that row; all members still supply and defend their own engineering contributions. Source and receiver unit checks may proceed in parallel after interfaces are agreed. Acquisition precedes calibration, and calibration precedes system accuracy and repeatability claims. PCB delivery delays require replanning rather than marking dependent tasks complete.

4. Societal Impact, Engineering Standards, Ethics, and Safety

Societal impact

The proposed RF front end could make reflection measurements more accessible for student experimentation and help users inspect impedance mismatch. Its educational benefit depends on documented calibration, reproducible procedures and an honest statement of operating limits.

The estimated non-labor budget of \$482.45 depends on access to shared laboratory instruments; purchasing those instruments would substantially increase the cost.

Incorrect measurements could lead users to select unsuitable components or draw false conclusions about a DUT. The report should state the validated band, uncertainty, input restrictions and test conditions. Documentation should identify connectors and units clearly so users with different levels of RF experience can reproduce a measurement. For users from different linguistic and educational backgrounds, labeled ports, SI units, diagrams and a

consistent step-by-step calibration procedure can reduce ambiguity. Global availability and regional shipping costs may limit access; documenting compatible substitutions can improve reproducibility without assuming identical availability everywhere.

Environmental considerations include avoiding unnecessary board revisions through schematic review and unit tests, reusing suitable laboratory fixtures, and routing scrap boards and components through approved electronics-waste channels. Any sustainability benefit remains qualitative unless it is measured.

Proposed laboratory procedures

Risk	Mitigation and required record
Electrical faults and heating	Inspect assembly and check for shorts with power off. Verify rail ratings and current-limit settings before energizing. Begin with a current-limited supply; stop on abnormal current, odor or heating. Record rail readings, supply settings and observed current and temperature; follow SYS-0.
Instrument and DUT damage	Confirm connector type, input ratings, DC bias and signal power before connecting. Use appropriately rated attenuation or DC blocking where needed. Disconnect power for rewiring; verify the grounding arrangement before attaching grounded probes.
RF coupling and interference	Use suitable coaxial interconnects, terminations and shielding where required. Keep stimulus within the approved conducted-test levels. Do not attach an antenna or external transmitter as part of this draft procedure.
Soldering and mechanical work	Use the laboratory extraction system and approved eye protection for the task. Store hot tools in their stands, secure the board and remove loose wire clippings. Follow posted equipment-specific procedures.

ESD and component damage	Use the laboratory ESD work surface and appropriate handling practices. Keep sensitive parts in protective packaging and confirm the safe bench grounding arrangement.
Lab access and scope changes	Course rules require safety training and at least two people present in the lab [8]. Added batteries, high voltage or human connections require the applicable additional procedures before work begins.

The board uses a +5 V input and an onboard +3.3 V regulator. J2 carries the board-generated 3.3 V rail; avoid connecting a second regulator to it. Before first power-up, select a current limit from the assembled load and startup requirements, and locate the laboratory emergency shutoff. SYS-0 defines the proposed rail-voltage check.

Engineering Standards

IEC 61010-1 addresses safety of electrical equipment for measurement, control and laboratory use [11]. IEC 61326-1 addresses electromagnetic compatibility for such equipment [12]. Their published scopes make them relevant candidates for this measurement instrument. The team should assess applicability to the final supply, enclosure, ports and use environment with the TA. The public scope summaries alone do not support clause-level conformity claims; applicable editions and requirements need review. No certification, compliance test or regulatory approval is claimed here.

Component datasheets [1]–[3] constrain interfaces and operating conditions, but meeting an IC specification does not demonstrate the assembled front end’s safety or measurement accuracy. The team must document the actual clock, bias and acquisition settings and verify them at the intended interfaces.

Ethics

The course ethics guidance calls for project-specific ethical analysis [9]. IEEE Code of Ethics item 1 prioritizes public safety, health and welfare; item 2 calls for understanding technological implications; item 5 calls for honest criticism, error correction, realistic claims and attribution [15]. For this instrument, the principal concern is misleading confidence in measurement results. In applying the IEEE Code of Ethics principles discussed by the course, the team should report uncertainty and limitations, preserve failed tests, and distinguish simulations, proposed targets and measurements. A borrowed schematic, reference implementation or diagram must be credited, and the report should identify the team's own changes and verification work.

Open, short and load responses used during calibration do not by themselves demonstrate independent accuracy. Separate verification devices and reference measurements should be used where possible [10]. The report should disclose unavailable equipment or incomplete checks rather than replacing them with unsupported performance claims. Contributor names should reflect actual work, and all members should review the final account of their contributions.

5. System-Level Requirements and Verification

The following procedures consolidate HLR-1 through HLR-3 and supplement the receiver and codec tests in Section 2. These are proposed acceptance tests, not measured results. The targets below follow the current team document; they supersede the unresolved numerical placeholders in the earlier Part 3 working draft.

ID / target	Setup and procedure	Acceptance and evidence
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SYS-1: HLR-1 frequency sweep	Connect X1 to a calibrated spectrum analyzer with a 50 Ω input and any required attenuation. Record cable/attenuator corrections. Command all 101 points from 12.54 to 14.58 MHz, including endpoints (20.4 kHz spacing). Allow at least the proposed 20 ms settling interval and measure frequency and corrected power at every point.	All 101 points occur in order; frequency error is within ± 1 kHz and power is -30 to 0 dBm at every point. Save command/readback logs, analyzer settings and corrected measurements. Check analyzer uncertainty before using these limits.
SYS-2: HLR-2 paired acquisition	Configure 8 MHz MCLK, proposed 48 ksample/s stereo I2S and fixed gain with AGC disabled. Verify clocks and channel identity using the Section 2 procedures. Run ten consecutive 101-point sweeps. After at least 20 ms settling at each point, retain at least 1024 valid reference/reflection pairs.	Across all 1,010 point records, no point or required pair is missing or invalid. Save raw data, point indices, frame counts, timestamps, channel identity and DMA/I2S error flags. Confirm the 48 ksample/s setting against measured clocks.
SYS-3: HLR-3 calibrated S11	Calibrate the prototype and reference VNA at equivalent X1 connector planes using open/short/load standards. Measure an independent verification load not used to fit prototype calibration, with reference S11 magnitude ≥ 0.2 at every required point. Use the same 101-point grid, equivalent cables/reference planes and compatible stimulus settings.	At every point, the absolute difference of linear S11 magnitudes is ≤ 0.10 and the absolute wrapped phase difference is $\leq 15^\circ$. Save complex traces, calibration identifiers, settings and reference uncertainty. A calibration-standard fit alone is not independent accuracy evidence [10].
SYS-0: supply-voltage prerequisite	Inspect assembly and check for shorts with power off. Use a current-limited bench supply at J1 pin 1 (+5 V) and pin 2 (GND). With the three clock outputs and paired acquisition enabled, set and verify TP1 at 4.75, 5.00 and 5.25 V relative to TP3. Measure TP2 at each setting. Power the external controller separately without back-feeding J2.	Proposed voltage acceptance: TP2 remains 3.201–3.399 V (3.3 V $\pm 3\%$) at all three input settings. Save supply settings, TP1/TP2 readings and operating configuration. Also record input current, rail ripple and regulator case temperature as diagnostic measurements; this test does not establish separate current, ripple or thermal compliance.

At 48 ksample/s, 1024 pairs require approximately 21.33 ms. Adding 20 ms settling gives a theoretical minimum of about 4.17 s for 101 points, excluding programming, transfer, processing

and additional settling. This is a timing calculation, not a demonstrated sweep-time requirement. The implemented sweep may take longer.

For SYS-3, compute magnitude error as $||S_{11}^{\text{prototype}}| - |S_{11}^{\text{reference}}||$. Wrap phase differences to -180° through $+180^\circ$ before taking the absolute value. HLR-3 specifies a verification-load magnitude floor of 0.2; phase near a matched load is not a substitute for this test. Record uncertainty and resolve any result too close to a limit to distinguish reliably from instrument error.

Each test record should contain operator/date, board and firmware revisions, instrument model and calibration status, setup, configuration, raw-data location, calculation, applicable limit and PASS/FAIL/NOT READY. Retain failed runs. Transmission hardware is present, but the current HLRs assess S11; an S21 claim would need its own calibration, quantitative target and independent verification.

Power-test basis and evidence status

The 4.75–5.25 V input sweep and $\pm 3\%$ output window are proposed project acceptance targets, not values measured on the prototype. The TLV755P recommended input range extends to 5.5 V, and the DBV regulator specifies $\pm 1\%$ output accuracy over -40 to 85°C under its stated test conditions [14]. The wider $\pm 3\%$ project window allows margin for loading, wiring and measurement; passing must still be demonstrated on the assembled board. If instrument uncertainty overlaps a limit, resolve the measurement before assigning PASS.

The ZIP supplies the power topology but no board-level ripple, total-current or case-temperature requirement [13]. Record ripple with a short probe ground and stated bandwidth, steady-state and

startup current with instrument settings, and stabilized regulator case temperature together with ambient temperature. The IC's 500 mA output capability is not the board's expected current, and its junction-temperature rating is not a case-temperature limit. These diagnostic results support subsequent load and thermal assessment. Stop testing if abnormal heating or current occurs.

All verification tables are plans. The supplied package contains no assembled-board performance measurements. Before fabrication, resolve or justify electrical and layout check findings using a KiCad version compatible with the board file; a routing-completion log alone is not fabrication approval [13].

Reference List

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[2] Skyworks Solutions, “Si5351A/B/C-B,” Data sheet, Rev. 1.3, 2021.
<https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/data-sheets/Si5351-B.pdf>

[3] Texas Instruments, “TLV320AIC3204 Ultra Low Power Stereo Audio Codec,” Data sheet, Rev. E, 2019. <https://www.ti.com/lit/ds/symlink/tlv320aic3204.pdf>

[4] Texas Instruments, “TLV320AIC3204 Application Reference Guide,” SLAA557, Nov. 2012.
[Online]. Available: <https://www.ti.com/lit/pdf/slaa557>

[5] University of Illinois Urbana-Champaign, “Design Document,” ECE 445 Senior Design Laboratory. [Online]. Available:

<https://courses.grainger.illinois.edu/ece445/guidelines/design-document.asp>. Accessed: Sep. 30, 2026.

[6] University of Illinois Urbana-Champaign, "Design Document Check," ECE 445 Senior Design Laboratory. [Online]. Available:

<https://courses.grainger.illinois.edu/ece445/guidelines/design-document-check.asp>. Accessed: Sep. 30, 2026.

[7] University of Illinois Urbana-Champaign, "Design Review," ECE 445 Senior Design Laboratory. [Online]. Available:

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[8] University of Illinois Urbana-Champaign, "Safety," ECE 445 Senior Design Laboratory.

[Online]. Available: <https://courses.grainger.illinois.edu/ece445/guidelines/safety.asp>. Accessed: Sep. 30, 2026.

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<https://courses.grainger.illinois.edu/ece445/guidelines/ethical-guidelines.asp>. Accessed: Sep. 30, 2026.

[10] Keysight Technologies, "Validity of a Cal," network analyzer help. [Online]. Available:

https://helpfiles.keysight.com/csg/m9485a/s3_cals/quest_cal.htm. Accessed: Sep. 30, 2026.

[11] International Electrotechnical Commission, "IEC 61010-1:2010," standard scope summary.

[Online]. Available: <https://webstore.iec.ch/en/publication/4279>. Accessed: Sep. 30, 2026.

[12] International Electrotechnical Commission, “IEC 61326-1:2020,” standard scope summary. [Online]. Available: <https://webstore.iec.ch/en/publication/62793>. Accessed: Sep. 30, 2026.

[13] X. Liu, “NanoVNA_RF_Frontend_PCB_v1,” Rev A1, Oct. 1, 2026, team-supplied design package, including schematics, circuit.json, BOM and routing logs. Derived from NanoVNA by TTRFTECH/edy555; distinguish upstream material from the team's modifications and retain applicable license notices.

[14] Texas Instruments, “TLV755P 500-mA, Low-IQ, Small-Size, Low-Dropout Regulator,” datasheet. <https://www.ti.com/lit/ds/symlink/tlv755p.pdf>. Accessed Oct. 2, 2026.

[15] IEEE Spectrum, “Board of Directors Approves Revisions to the IEEE Code of Ethics,” 2020. <https://spectrum.ieee.org/board-of-directors-approves-revisions-to-the-ieee-code-of-ethics>. Accessed Oct. 2, 2026.