

Multi-Mode Table Tennis Target Training System

ECE 445 Design Document - Fall 2026

Project No. 22

Team Members: Alice Xu / alicex2, Ben Seo / seo58, Brandon Dang / bd16

TA: Abdullah Alawad

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Senior Design Laboratory
Department of Electrical and Computer Engineering

Contents

1. Introduction

- 1.1 Problem and Solution
- 1.2 Visual Aid
- 1.3 High-Level Requirements

2. Design

- 2.1 Physical Design
- 2.2 Block Diagram and Interfaces
- 2.3 Universal PCB and Power Subsystem
- 2.4 Impact-Sensing and Analog Front End
- 2.5 Embedded Control and Wireless Communication
- 2.6 Target Illumination
- 2.7 Central Controller and User Interface
- 2.8 Mechanical Target Subsystem
- 2.9 Software Design
- 2.10 Commercial Component Selection and Design

Risks

- 2.11 Tolerance Analysis

3. Cost and Schedule

- 3.1 Cost Analysis
- 3.2 Schedule

4. Societal Impact, Engineering Standards, Ethics, and Safety

5. References

1. Introduction

1.1 Problem and Solution

Problem. Shot placement is one of the most important controllable variables in table tennis, yet many placement drills still use passive tape, cones, or paper targets. Those methods show a player where to aim but do not automatically detect the first bounce, distinguish a correct target from an incorrect target, or preserve quantitative statistics across repeated practice. Research on table-tennis stroke effectiveness treats ball placement as a measurable component of performance, supporting the usefulness of placement-oriented training [1]. A second person can provide randomized instructions and score the outcome manually, but that reduces the accessibility and repeatability of independent practice.

Solution. The proposed system uses three movable electronic targets and one central controller. Each target combines a low-profile impact plate, a piezoelectric sensor, an analog signal-conditioning circuit, perimeter LEDs, an ESP32-S3 wireless controller, and a custom PCB. The controller selects the active target, classifies each reported impact as correct or wrong, manages Rapid-Fire and Serve Accuracy modes, and displays session statistics. Unlike passive tape/cone targets, the system automatically detects and scores impacts; unlike camera-based training systems, it does so without collecting video or requiring computer-vision processing. The removable targets can be repositioned on an existing table, so the design adds quantitative feedback without permanently modifying the table.

The design is intentionally modular. The same universal custom PCB is used in each of the three targets and in the central controller, reducing PCB variants and simplifying spare-board management. Each target makes the analog impact decision locally so that the small piezo signal does not travel across the table on long wires. Only digital messages are exchanged wirelessly. This differs from a passive target by adding closed-loop cueing, impact sensing, wrong-target identification, and automatic performance logging while remaining removable from a standard table.

1.2 Visual Aid

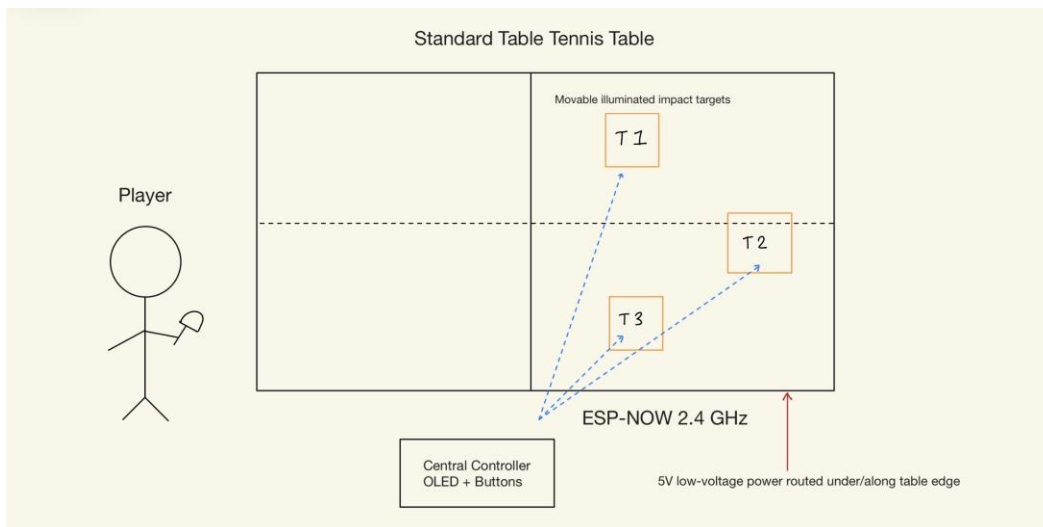


Figure 1. Use context for the training system. The player aims at one illuminated target while the central controller coordinates all three targets and records the result.

1.3 High-Level Requirements

- The system shall correctly detect at least 90% of direct table-tennis-ball impacts on each target during a controlled test of at least 30 impacts per target distributed across the target surface.
- When one target is active, the system shall correctly classify at least 90% of at least 30 controlled electronic-target impacts as either a correct-target hit or a wrong-target hit.
- The system shall complete both required training modes: at least 20 randomized target activations in Rapid-Fire Placement Mode and at least 10 serves using at least three target locations in Serve Accuracy Mode, while correctly

recording correct hits, wrong-target hits, misses/timeouts, total trials, and accuracy and automatically advancing to the next target when appropriate.

2. Design

2.1 Physical Design

Each target is designed as an approximately 10 in x 10 in removable pad with a rigid upper impact plate, a piezoelectric element bonded to the underside, perimeter illumination, a protected electronics enclosure near the rear edge, and four low-profile suction cups. The target height objective is less than 0.5 in over the usable impact area. The suction cups are used instead of rubber feet so that the target resists sliding while remaining repositionable between Rapid-Fire and Serve Accuracy drills. Because tabletop finish affects suction performance, the mounting system will be verified on the actual table rather than assumed from material data alone.

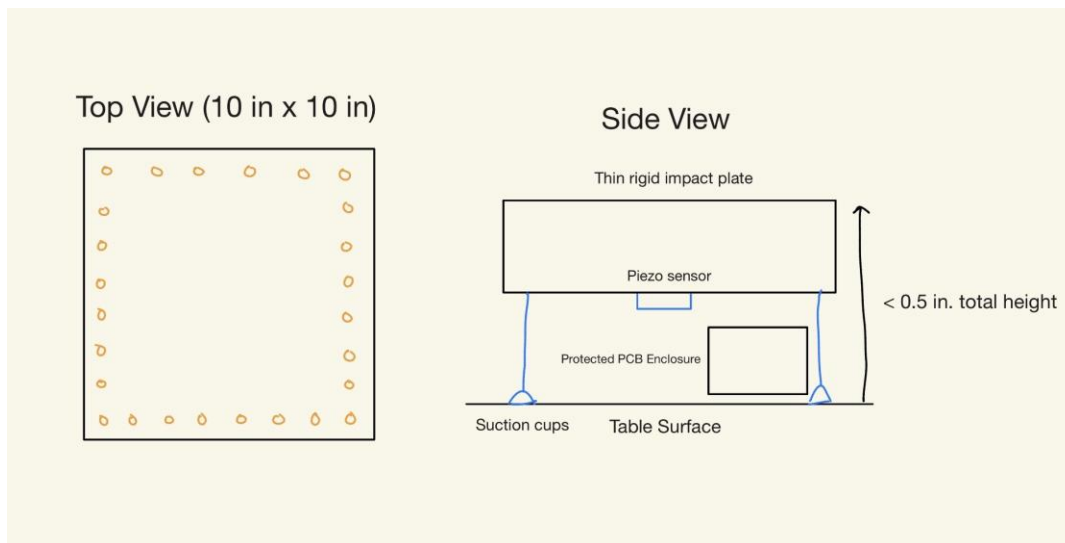
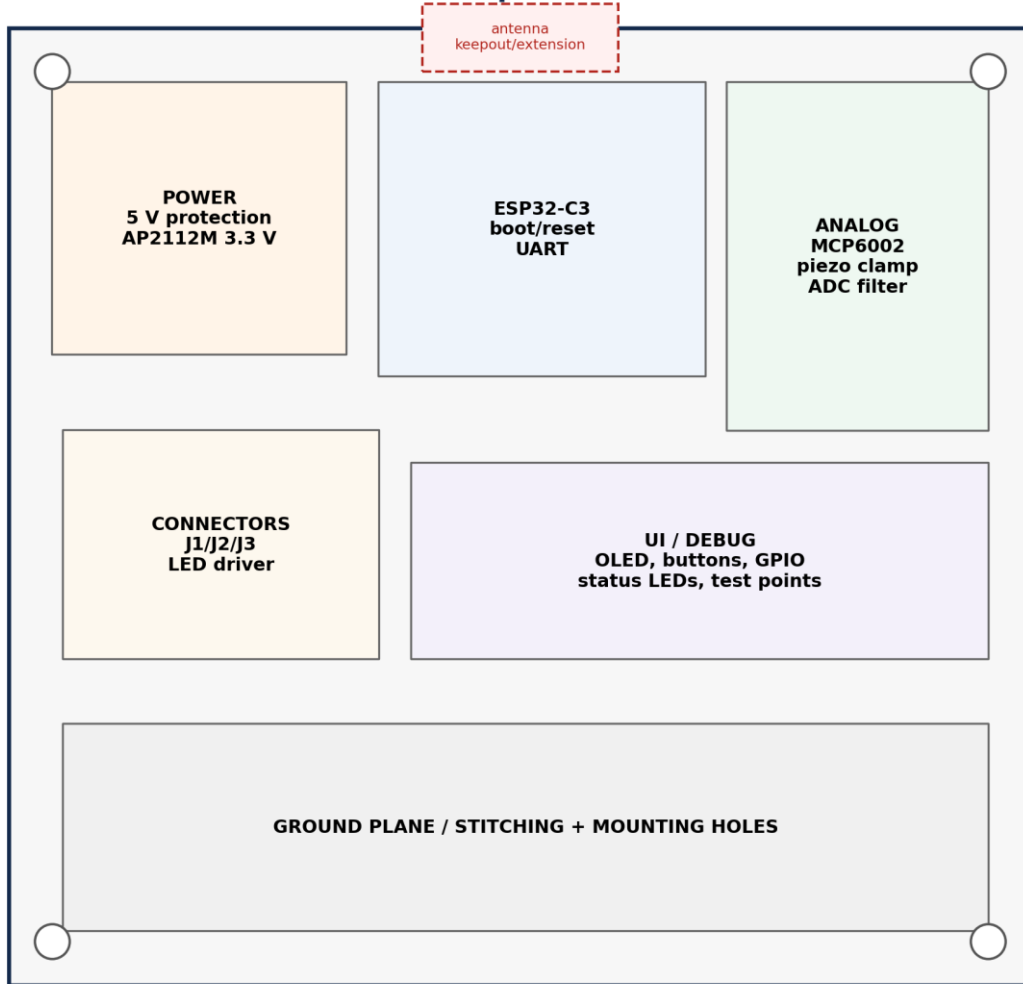


Figure 2. Mechanical target concept with low-profile suction cups, under-plate piezo sensor, perimeter LEDs, and protected electronics enclosure.

The central controller may be mounted at the table edge or on a small stand outside the primary ball path. All power cables are routed toward the table edge and then underneath the table. The 5 V supply is distributed in a star arrangement so LED switching and radio current from one target do not share long series return paths with another target. The custom PCB itself is approximately 94 mm x 88 mm and contains four 3.2 mm non-plated mounting holes. The ESP32-S3 module antenna is located at the board edge and requires clearance from conductive enclosure hardware and wiring [3].

Universal PCB Floorplan - 94 mm × 88 mm



Conceptual placement only; exact Rev B routing/footprints remain subject to native KiCad ERC/DRC.

Figure 3. Conceptual universal-PCB floorplan. It communicates functional placement and mechanical constraints, not final native KiCad routing.

2.2 Block Diagram and Interfaces

ECE 445 Multi-Mode Table Tennis Target Training System - Block Diagram

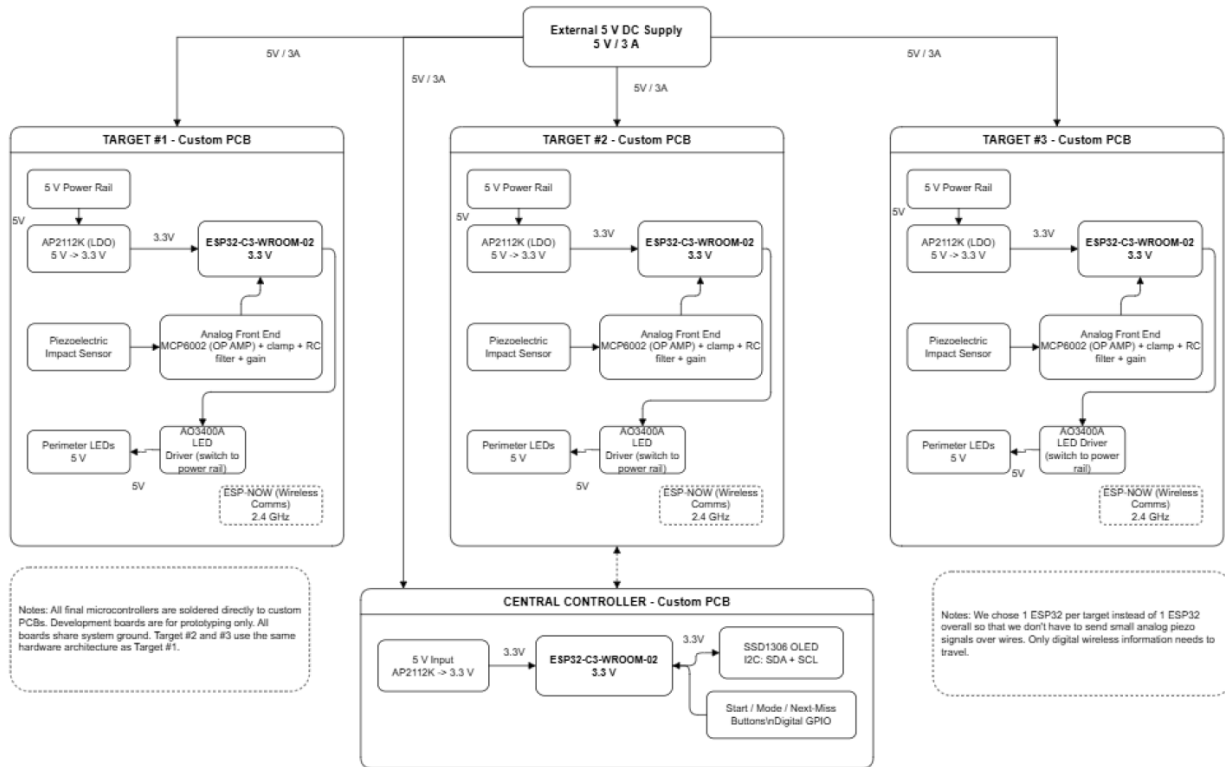


Figure 4. System block diagram showing four universal PCBs, 5 V distribution, local 3.3 V regulation, analog sensing, user-interface connections, and ESP-NOW wireless communication.

The critical architectural choice is local impact processing. Each target converts mechanical energy into an analog signal, conditions and samples that signal locally, and transmits only a digital event. This avoids carrying high-impedance analog signals over several feet of cabling. The central controller manages game state and statistics but does not directly sample remote piezos.

Table 1. Primary electrical and communication interfaces

Interface	Electrical level	Signals / protocol	Design notes
J1 board power	4.75-5.25 V DC	5 V + GND	Bench-supply compatible; star distribution in final system.
Local logic rail	3.3 V nominal	3.135-3.465 V design band	Powers ESP32-S3, MCP6002, pull-ups and UI logic.
Piezo -> AFE	Analog transient	AB2036B -> clamp -> op amp	High-impedance sensor path kept local to target.
AFE -> ESP32	0-2.5 V measurement target	ADC0, ≥ 20 ksample/s	6.8k/15k attenuation plus 4.7 nF low-pass.
Target LED	Protected ~5 V power	GPIO6 -> AO3400A	External LED assembly must include current limiting; ≤ 200 mA design ceiling.
Target <-> controller	3.3 V internal radio	ESP-NOW, 2.4 GHz	Peer-to-peer command/event packets; no access point required.
OLED	3.3 V	I2C: SDA GPIO4, SCL GPIO5	4.7k pull-ups on PCB; selected display wired by signal name.

Interface	Electrical level	Signals / protocol	Design notes
Buttons	0/3.3 V	Active-low GPIO18/19/3	10k pull-ups and 100 nF input filters.
Programming	3.3 V logic	UART TX/RX + BOOT/EN	External adapter red 5 V lead remains disconnected.

2.3 Universal PCB and Power Subsystem

The universal PCB is used in all four electronic units. J1 accepts regulated 5 V. A resettable PTC fuse and series SS14 Schottky diode provide overcurrent and reverse-polarity protection before the protected 5 V rail. The AP2112M-3.3TRG1 SOIC-8 LDO generates the local 3.3 V rail. This rail supplies the ESP32-S3 module, MCP6002 analog circuitry, pull-ups, status LED, and controller OLED. The external target perimeter LEDs remain on the protected 5 V rail so their current does not flow through the 3.3 V LDO. Bulk and local 100 nF bypass capacitors are distributed near the active devices. The PCB uses ground planes and stitching vias to reduce return-path impedance and EMI, following the course PCB guidance [18].

The design uses 3.3 V logic throughout. The selected OLED and USB-to-UART adapter are operated with 3.3 V I/O, so no general-purpose digital level shifter is required. A future 5 V-only device connected to the spare GPIO header would require a separately reviewed interface. The power board is deliberately bench-supply friendly so initial assembly can be current-limited before the MCU or peripherals are connected.

Power design release item: The AP2112M electrical voltage range is compatible with the design, but continuous thermal margin has not yet been demonstrated in the final enclosure. The selected PTC fuse is also still under review because its hold current derates with temperature. Both are treated as verification items rather than assumed successes.

Table 2. Universal PCB and power subsystem requirements and verification

Requirement	Verification procedure
PWR-1. With 4.75-5.25 V applied at J1, the local logic rail shall remain within 3.135-3.465 V during normal radio activity, OLED operation, and target LED switching.	Use a current-limited bench supply, DMM, and oscilloscope. Power one fully populated board at 4.75 V, 5.00 V, and 5.25 V. Run a firmware load that repeatedly transmits ESP-NOW packets and toggles the target LED load. Measure the 3.3 V rail at a test point for 60 s at each input voltage. Record minimum, maximum, and peak-to-peak ripple; verify the rail remains inside 3.135-3.465 V.
PWR-2. The local 3.3 V rail shall exhibit no more than 100 mV peak-to-peak transient ripple during radio transmit bursts and LED switching.	Probe the 3.3 V test point with a short-ground oscilloscope probe while transmitting at the maximum intended packet rate and toggling the external LED load. Capture at least 20 switching/radio events and record the largest peak-to-peak excursion.
PWR-3. LED switching shall produce no more than one false impact event during a five-minute stationary-target test.	Place the target on the table without ball impacts. Run an automated script that repeatedly switches the external LED assembly while ESP-NOW remains active. Log every impact event received by the controller for five minutes; pass if the count is ≤ 1 .
PWR-4. No power-path component shall exceed the team-selected 125 C junction-temperature design budget during a 20-minute worst-case operating session.	Operate a fully assembled board in the intended enclosure with radio traffic, OLED (controller board where applicable), and final LED assembly. Measure regulator case temperature with a thermocouple/IR method and estimate junction temperature using the final board-specific thermal model. Record steady-state current and temperature. Redesign the supply if the estimated junction exceeds 125 C.

2.4 Impact-Sensing and Analog Front End

The impact-sensing subsystem converts a first-bounce event into a robust digital hit message. An external PUI Audio AB2036B piezoelectric element is attached beneath the impact plate. The device has a nominal 25 nF capacitance and approximately 3.6 kHz resonant frequency [2]. Its raw impact waveform can contain positive and negative excursions, ringing, table vibration, and electrical interference. Therefore, the piezo is not connected directly to the ESP32 ADC.

The PCB first limits transient current with $R19 = 100 \text{ kohm}$ and a BAT54S dual-series Schottky clamp referenced to ground and the analog supply. MCP6002 channel A buffers a half-supply reference near 1.65 V. Channel B then amplifies the impact around that reference. JP1 selects approximately 2x gain when bridged or 6.7x gain when open. Initial bring-up will use 2x gain to reduce saturation risk. The output is then attenuated by 6.8 kohm / 15 kohm and filtered by 4.7 nF before ADC0. This network scales a rail-limited op-amp output by approximately 0.688 and produces a nominal 7.24 kHz low-pass pole. The firmware samples at no less than 20 ksample/s, establishes a baseline, computes the magnitude of the deviation from baseline, captures the first valid peak, and enters a calibrated lockout period to reject piezo ringing.

Target Impact-Sensing and Illumination Signal Paths

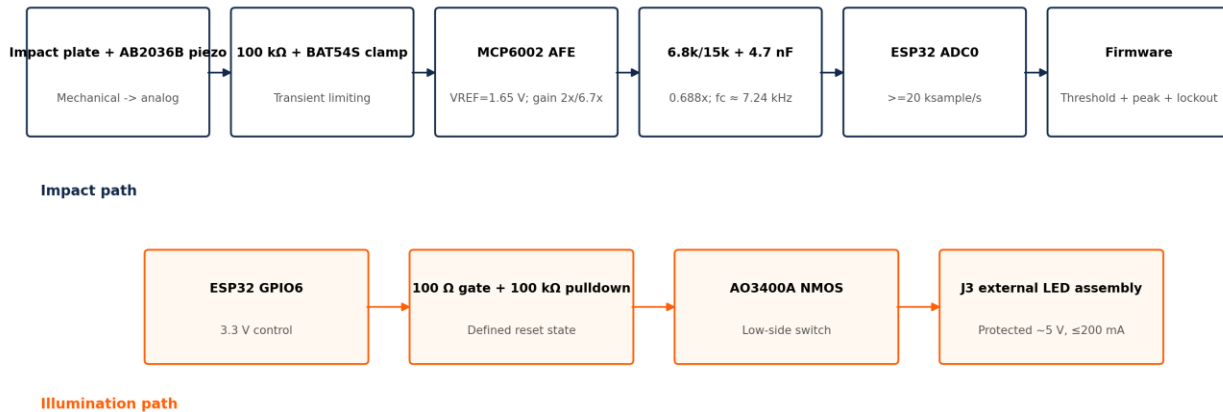
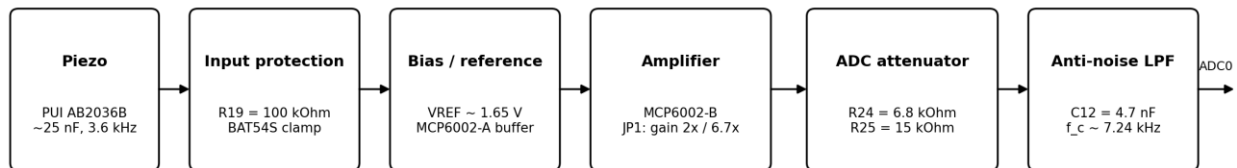


Figure 5. Target impact-sensing and illumination signal chains.

Rev B impact-sensing analog signal path



The analog path is local to each target; the ESP32 digitizes the conditioned waveform and applies threshold/lockout logic before wireless transmission.

Figure 5A. Rev B impact-sensing analog path with the component values used in the current PCB design.

Figure 5A makes the student-designed sensing path explicit: the piezo transient is current-limited and clamped, biased about a buffered half-supply reference, amplified with selectable gain, attenuated for ADC headroom, and low-pass filtered before sampling. These choices directly support SNS-1 through SNS-5.

Table 3. Impact-sensing subsystem requirements and verification

Requirement	Verification procedure
SNS-1. Each target shall detect at least 27 of 30 direct table-tennis-ball impacts distributed across center, edge, and corner regions of the usable impact area.	Mark at least five impact regions on the plate. Deliver 30 representative ball impacts distributed across those regions while recording a synchronized manual ground-truth tally and controller event log. Count a trial as detected when exactly one target event is produced within the acceptance window. Pass if $\geq 27/30$ are detected.
SNS-2. Each physical impact shall produce no more than one registered hit event.	During the 30-impact SNS-1 test, log all local detections and controller packets. For every physical impact, count events in the 200 ms following the first detection. Pass if every physical impact produces at most one accepted hit event.
SNS-3. Nearby table bounces and ordinary table vibration shall produce no more than one false target hit during a five-minute stationary test.	Place the target in normal use position. For five minutes, bounce balls on the bare table adjacent to but outside the target and create representative non-impact vibration. Record the controller log. Pass if ≤ 1 false hit is registered.
SNS-4. Local impact detection shall generate a timestamped hit event within 20 ms of the first threshold crossing.	Use an oscilloscope or logic analyzer. Probe the conditioned ADC signal and toggle a spare debug GPIO in firmware when the accepted hit event is created. Apply at least 20 impacts and measure the delay from first valid threshold crossing to debug transition. Pass if every measured delay is ≤ 20 ms.
SNS-5. The conditioned ADC node shall remain within the configured ESP32-S3 ADC measurement range during the controlled impact test.	Probe ADC0 with an oscilloscope while performing center and edge impacts using both gain settings. Use the final firmware attenuation setting. Record maximum and minimum measured voltages; verify they remain inside the selected measurement range without rail-clamp overstress.

2.5 Embedded Control and Wireless Communication

Each universal board uses an ESP32-S3-WROOM-02-N4 module. The target firmware samples ADC0, evaluates the impact detector, controls the local LED MOSFET, maintains a target identifier and trial identifier, and exchanges packets with the controller. ESP-NOW is selected because it provides direct peer-to-peer communication on the ESP32 2.4 GHz radio without requiring a local Wi-Fi infrastructure [7]. The central controller stores the MAC addresses/IDs of the three targets. Radio callbacks are kept short; received data are placed into the application state machine rather than performing display or scoring work directly in the radio callback.

A target-activation command includes the target ID and trial ID. A hit event includes the source target ID, trial ID, local timestamp, and optionally the measured peak ADC deviation for diagnostics. The controller uses the source target ID to classify correct and wrong-target hits. Because all three targets continue monitoring even when only one LED is active, a ball landing on an inactive electronic target is still reportable. Duplicate or stale packets are rejected by trial ID and event state.

Table 4. Embedded control and wireless subsystem requirements and verification

Requirement	Verification procedure
COM-1. At a 5 m indoor separation, each target shall successfully complete at least 99 of 100 command-response trials with the controller.	Place the central controller and one target 5 m apart in the intended indoor environment. Send 100 numbered activation commands and require a numbered application-level acknowledgement for each. Record transmitted, acknowledged, and duplicate messages. Repeat for all three targets. Pass each target at $\geq 99/100$.

Requirement	Verification procedure
COM-2. After a locally accepted hit, the controller shall receive the corresponding hit event within 50 ms for at least 99% of 100 injected test events.	Use firmware test mode to generate 100 timestamped local hit events without relying on ball placement. Compare target event timestamp with controller receive timestamp. Record all latencies and loss; pass if ≥ 99 events arrive and at least 99% of received events are ≤ 50 ms.
COM-3. Only the selected target shall illuminate, while all three targets continue to accept local impact events.	Run 30 randomized trials. Before every trial, record the commanded target, visually verify exactly one target is illuminated, then deliberately strike each of the three electronic targets across the sequence. Compare source target IDs in the log with the physical target struck. Pass if illumination selection is correct in all 30 trials and every struck electronic target produces its own source ID when detected.
COM-4. Reset or lost power on one target shall not corrupt controller statistics or cause another target to change ID.	Begin a 20-trial diagnostic session, power-cycle one target, and continue communicating with the other two. Confirm unique IDs remain unchanged and that stale packets from the restarted target are rejected until it rejoins with a valid current trial state.

2.6 Target Illumination

The active target is indicated by perimeter LEDs rather than a central light source so the primary rebound area remains unobstructed. GPIO6 drives the gate of an AO3400A N-channel MOSFET through a 100 ohm resistor; a 100 kohm gate pull-down holds the MOSFET off during reset. J3 provides the protected positive LED rail and a low-side switched return. The PCB intentionally does not place the perimeter LED current-limit resistors on-board because the final LED geometry is external and may change during visibility testing. Every final LED branch must therefore include its own current limiting or the team must select a complete resistored assembly.

A current prototype option is eight Kingbright WP7113SGC LEDs per target, each with a 330 ohm resistor. The calculated worst-case aggregate current for that candidate remains below the board design ceiling of 200 mA, but the number, viewing angle, diffuser, and mechanical height will be selected by the 3 m visibility test rather than by current alone.

Table 5. Target illumination subsystem requirements and verification

Requirement	Verification procedure
LED-1. An observer shall correctly identify the active target in at least 19 of 20 randomized trials from a distance of 3 m under normal indoor lighting.	Place all three targets on the table and an observer 3 m away. Randomly activate one target for each of 20 trials without telling the observer. Record the commanded target and observer response. Pass with ≥ 19 correct identifications.
LED-2. Visible target illumination shall begin within 100 ms of the central controller issuing a valid activation command.	Use a logic analyzer or oscilloscope on a controller debug pin marking command transmission and a photodiode or target debug pin marking LED activation. Measure 20 activation events at 5 m. Pass if each is ≤ 100 ms.
LED-3. LED switching shall not cause the impact subsystem to exceed its false-trigger requirement.	Execute PWR-3 with the final LED assembly, final cable length, and final target enclosure. Pass if the complete target produces ≤ 1 false hit in five minutes.

2.7 Central Controller and User Interface

The central controller uses the same PCB but connects an external 0.96 in SSD1306 OLED to J5 and three active-low user buttons to J6. The OLED operates from the 3.3 V rail and uses GPIO4 for SDA and GPIO5 for SCL, with 4.7 kohm pull-ups on the PCB. Start, Mode, and Miss/Next are connected to GPIO18, GPIO19, and GPIO3 respectively. The inputs use 10 kohm pull-ups and 100 nF filters; firmware additionally performs logical debounce. The selected display is wired by signal name because small SSD1306 modules do not have a universal connector pin order [8].

The display presents the current mode, active target, trial number, correct hits, wrong-target hits, misses/timeouts, accuracy, and streak where applicable. Serve Accuracy Mode uses the Miss/Next button because a ball that strikes no electronic target cannot create an automatic sensor event. No timing requirement is imposed on the player's serve.

Table 6. Central controller and user-interface requirements and verification

Requirement	Verification procedure
UI-1. The controller shall correctly maintain correct-hit, wrong-target, miss/timeout, total-trial, accuracy, and streak values through a 20-trial Rapid-Fire session.	Prepare a scripted 20-trial sequence containing known correct hits, wrong-target hits, and timeouts. Keep an independent manual truth table. Run the session and compare every final displayed/statistical field against the truth table. Pass if all counts and derived accuracy are exact.
UI-2. Serve Accuracy Mode shall accept correct hits, wrong-target hits, and manual misses over at least 10 serves using at least three target locations.	Run 10 scripted serve trials that include all three outcomes. For miss trials, press the Miss button. Compare displayed session statistics with a manual truth table. Pass if all 10 trials are classified and counted correctly.
UI-3. The OLED shall reflect a classified trial result within 250 ms.	Toggle a debug output when a trial is classified and use a camera/photodiode or firmware display-update marker to determine update completion. Measure at least 20 events. Pass if all updates occur within 250 ms.
UI-4. Each Start, Mode, and Miss input shall register exactly one application action for at least 30 presses per button.	Use a firmware counter screen or serial log. Press each button 30 times at varied speeds. Record physical presses and logical actions. Pass if each button produces exactly 30 logical actions with no doubles or misses.

2.8 Mechanical Target Subsystem

The mechanical subsystem establishes the impact geometry, sensor coupling, table attachment, and user-facing safety of the target. The target plate material will be selected experimentally. Polycarbonate and thin hardboard/plywood are practical prototypes because they are rigid, readily cut/drilled, and compatible with adhesive sensor attachment. Four low-profile suction cups hold each target to the table. Suction-cup performance depends on the table finish, so the final mounting choice must be demonstrated on the actual playing surface. The PCB and connector assembly are kept outside the primary bounce area and enclosed to protect both electronics and users.

Table 7. Mechanical target subsystem requirements and verification

Requirement	Verification procedure
MEC-1. The usable target assembly shall rise no more than 0.5 in (12.7 mm) above the table surface.	Use digital calipers or a height gauge at the center, edges, and over any under-plate hardware that lies within the usable impact area. Record the maximum height; pass if ≤ 12.7 mm.
MEC-2. During 20 representative ball impacts, no suction cup shall release and the target shall move no more than 2 cm from its initial position after any individual impact.	Mark the initial target outline on the table using removable reference tape. Apply 20 representative impacts including edge impacts. After each impact, measure maximum target displacement with a ruler and inspect all four suction cups. Pass if every displacement is ≤ 2 cm and no cup releases.
MEC-3. Average rebound height from the target shall be within 25% of the average bare-table rebound height over at least 10 fixed-height drops on each surface.	Create a fixed-height ball-drop fixture and place a vertical scale beside the bounce region. Record 10 bare-table and 10 target bounces using slow-motion video. Compute each mean rebound height and percent difference. Pass if $ H_{\text{target}} - H_{\text{table}} /H_{\text{table}} \leq 0.25$.
MEC-4. The PCB enclosure, wiring, LEDs, and suction hardware shall not expose sharp edges or loose wiring in the primary impact region.	Perform a pre-use mechanical inspection after final assembly. Pull gently on each cable to verify strain relief, inspect enclosure edges and fasteners, and verify the ball-impact region is free of protruding electronics.

2.9 Software Design

The firmware is split into target firmware and controller firmware. Target firmware owns ADC acquisition, baseline tracking, hit qualification, duplicate/ringing rejection, LED output, target identity, and ESP-NOW event transmission. Controller firmware owns mode selection, trial IDs, randomized target selection, timeouts, result classification, statistics, OLED output, and user-button processing. Shared packet definitions ensure that the same target ID, trial ID, event type, timestamp, and diagnostic fields are interpreted consistently at both ends.

Controller Firmware State Machines

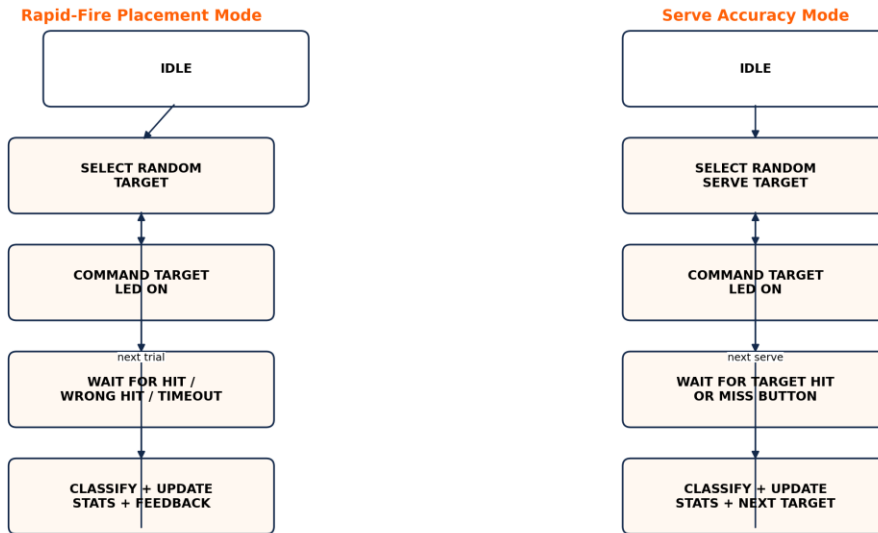


Figure 6. Required-mode controller state machines. Reaction Return Mode is intentionally excluded from the base success path.

Rapid-Fire Mode advances automatically after a valid correct hit, wrong-target hit, or timeout. To prevent unrealistic repetition, firmware may reject the immediately previous target when selecting the next target; this policy will be fixed before formal verification so the randomization rule is deterministic and testable. Serve Accuracy Mode has no automatic service timer: the player may complete a normal motion, and a manual Miss action advances the trial when no target is struck. All scoring uses the current trial ID so late wireless packets cannot modify a completed trial.

2.10 Commercial Component Selection and Design Risks

Table 8 summarizes the major component choices. Components were selected from the current procurement workbook and matched to the Rev B schematic/PCB properties. Package-fit and native KiCad DRC remain separate release tasks; this document does not treat a supplier part number alone as proof of manufacturability.

Table 8. Major component selection and design justification

Function	Selected part	Reason for selection	Important limitation / alternative
Wireless MCU	ESP32-S3-WROOM-02-N4	Integrated 2.4 GHz radio and ESP-NOW support; enough GPIO/ADC; one module can serve target or controller.	TA must confirm module satisfies course implementation rule; antenna clearance and exposed-pad assembly matter.
Piezo sensor	PUI AB2036B	Small 20 mm piezo element with known capacitance/resonance; inexpensive and easy to bond under target.	Impact amplitude and edge sensitivity are mechanical-system dependent; second sensor remains fallback if one sensor cannot cover the plate.
Analog front end	MCP6002-I/SN	Dual low-power op amp works from 3.3 V and allows reference buffer plus impact amplifier in one package.	Transient recovery and clamp behavior must be measured with the actual piezo.

Function	Selected part	Reason for selection	Important limitation / alternative
3.3 V regulator	AP2112M-3.3TRG1	Fixed 3.3 V LDO, simple low-noise supply, SOIC-8 package is easier to assemble than tiny alternatives.	Thermal HOLD: actual continuous current and enclosure temperature must be measured. A buck regulator is fallback if dissipation is excessive.
LED switch	AO3400A	Logic-level NMOS with low RDS(on) specified at 2.5 V gate drive.	External LED assembly still needs current limiting and visibility verification.
Display	0.96 in SSD1306 OLED (Adafruit 326 candidate)	Compact 128x64 display; I2C uses two signals; supports 3.3 V interfacing.	Module pin order is not standardized; current must remain within controller power budget.
Input protection	SS14 + BAT54S + PTC candidate	Reverse-polarity, piezo transient clamping, and overcurrent protection address likely integration mistakes.	PTC 1812L110/24DR remains on HOLD until current/temperature margin is reconciled.

Primary engineering risks: 1) detecting a lightweight ball across the full plate without ringing/false triggers; 2) maintaining LDO thermal margin under real radio/UI load; 3) choosing a PTC whose temperature-derated hold current does not nuisance-trip; 4) maintaining suction on the actual table finish; 5) keeping target/enclosure geometry below the mechanical height objective. Each risk has a bench or mechanical verification step before final release.

2.11 Tolerance Analysis

Impact sensing is the critical subsystem because the project fails if a lightweight table-tennis ball cannot be distinguished from ringing, adjacent bounces, and electrical noise. The analysis below checks whether the current analog bandwidth and ADC scaling can preserve the dominant piezo response while staying inside the intended ADC measurement range. It does not replace impact measurements; instead, it shows that the selected component values provide a feasible operating window.

2.11.1 Piezo high-pass behavior

The AB2036B nominal capacitance is approximately 25 nF [2]. With the 1 Mohm bias/return resistance, the sensor-network time constant and high-pass corner are:

$$\tau = R C = (1.0 \times 10^6 \text{ ohm})(25 \times 10^{-9} \text{ F}) = 25 \text{ ms}$$

$$f_{\text{HP}} = 1 / (2 \pi R C) = 6.37 \text{ Hz}$$

The 6.37 Hz corner is far below the piezo's approximately 3.6 kHz nominal resonance. The bias network therefore does not significantly suppress the fast impact content.

2.11.2 ADC low-pass behavior

The ADC network uses R24 = 6.8 kohm, R25 = 15 kohm, and C12 = 4.7 nF. The Thevenin resistance seen by the capacitor is:

$$R_{\text{TH}} = R24 \parallel R25 = 4.679 \text{ kohm}$$

$$f_{\text{LP}} = 1 / (2 \pi R_{\text{TH}} C12) = 7.24 \text{ kHz}$$

At 3.6 kHz, the low-pass magnitude is approximately 0.895 (-0.96 dB). Combined with the nearly unity high-pass magnitude at that frequency, the ideal network preserves about 89.5% of a 3.6 kHz component while increasingly attenuating higher-frequency electrical noise.

A worst-case component-tolerance check further demonstrates feasibility. The AB2036B capacitance is specified with approximately +/-30% tolerance and its resonance is approximately 3.6 kHz with a +/-0.5 kHz tolerance [2]. Therefore, with R = 1 MOhm, the piezo high-pass corner remains between approximately 4.90 Hz and 9.09 Hz, still more than two orders of magnitude below the lowest expected resonance frequency (3.1 kHz).

For the ADC low-pass network, using +/-1% resistor tolerance and +/-10% C12 tolerance gives a corner-frequency range of approximately 6.51 kHz to 8.12 kHz. Evaluating the worst combination at the highest expected sensor resonance (4.1 kHz) gives a combined high-pass/low-pass magnitude of at least 0.846 (-1.45 dB). Thus, even at the tolerance extremes, the intended piezo resonance band is not strongly attenuated before digitization.

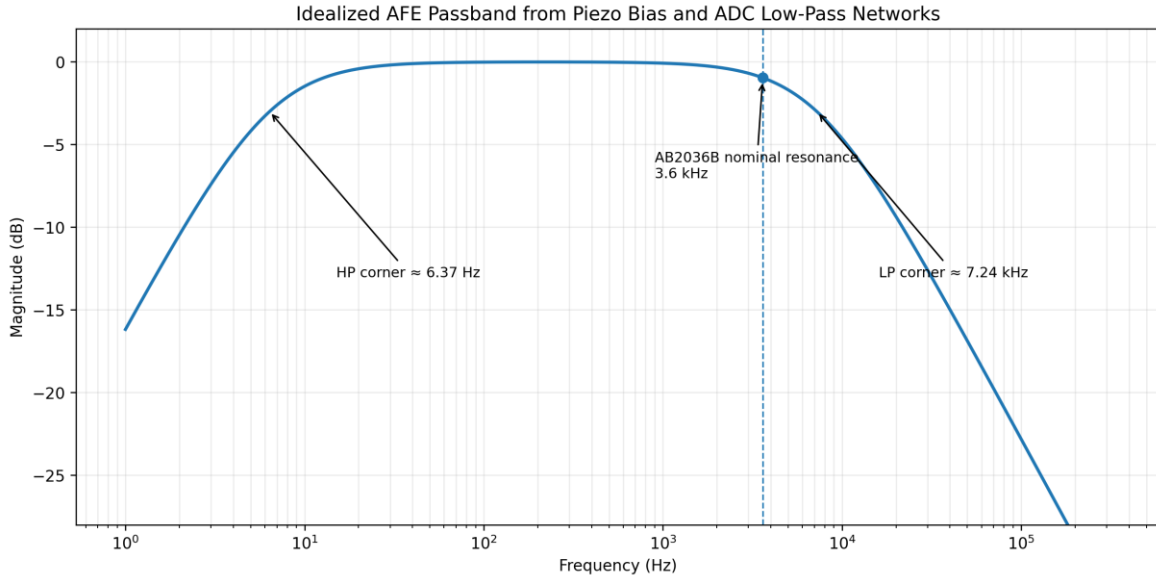


Figure 7. Idealized magnitude response formed by the piezo bias high-pass and ADC low-pass networks.

2.11.3 Sampling and ADC headroom

At the planned minimum sample rate of 20 ksample/s, the Nyquist frequency is 10 kHz and a 3.6 kHz component is represented by approximately 5.56 samples per cycle. This is sufficient for threshold/peak event detection, although it is not a claim of high-fidelity waveform reconstruction. The ADC divider ratio is:

$$k = 15 / (6.8 + 15) = 0.6881$$

With a 1.65 V quiet AFE output, the expected ADC baseline is approximately 1.135 V. For a conservative static rail of 3.465 V and worst-direction 1% resistor tolerances, the divider ratio rises to approximately 0.69235, which gives:

$$V_{\text{ADC,max}} = 3.465 \text{ V} \times 0.69235 = 2.399 \text{ V}$$

This leaves approximately 0.101 V of static margin below the 2.5 V measurement range used for the ESP32-S3 high-attenuation ADC configuration. The calculation demonstrates feasibility under the stated steady-state assumptions, but does not bound ESD, supply overshoot, or piezo-generated transient energy. Those effects are covered by the clamp/current-limiting network and must be verified with an oscilloscope during the impact test. The gain jumper provides a second degree of freedom: gain 2 is used initially to maximize headroom; gain 6.7 is available if measured edge impacts are too small.

2.11.4 Secondary power-risk check

The 5 V-to-3.3 V LDO is a secondary feasibility risk. Ignoring small quiescent power, LDO dissipation is approximately $P = (V_{\text{IN}} - V_{\text{OUT}})I$. With an illustrative 4.95 V regulator input and 0.40 A continuous 3.3 V load, P is about 0.66 W. Using the AP2112M SOIC-8 datasheet thermal resistance of approximately 114 C/W [5] and a 40 C local ambient gives an illustrative junction estimate near 115 C. At 0.50 A the same simple model rises to roughly 134 C. Therefore, the design is plausible for the expected transient-heavy ESP32 load but cannot be released based on the 600 mA nameplate alone. Actual average/current-burst measurements and enclosure temperature determine whether the LDO remains or a switching regulator is required.

3. Cost and Schedule

3.1 Cost Analysis

The course design-review guidance recommends an engineering labor rate near \$50/hour with a 2.5x overhead multiplier [10]. For planning, this document assumes three team members and 80 engineering hours per person over the semester. The labor estimate is therefore:

$$\text{\$50/hour} \times 2.5 \times 80 \text{ hours} = \text{\$10,000 per team member}$$

$$\text{Total labor} = 3 \times \text{\$10,000} = \text{\$30,000}$$

Table 9 is a complete procurement-oriented bill of materials for the current four-board build. It lists the exact manufacturer part number and purchase link for each purchased electronic part group, plus external and fabricated mechanical items. Rows marked HOLD or REVIEW are included for traceability but are not treated as fabrication-release approval. Prices are low-quantity planning estimates and should be rechecked immediately before ordering.

Table 9. Complete project bill of materials and purchase sources

Description	Manufacturer / part #	Key specification / status	Qty	Unit (\$)	Ext. (\$)	Purchase link
ESP32-S3 wireless MCU (U1)	Espressif ESP32-S3-WROOM-02-N4	3.3 V; 4 MB flash; PCB antenna Status: REVIEW - TA / RF	4	3.38	13.52	Supplier
3.3 V LDO regulator (U2)	Diodes Incorporated AP2112M-3.3TRG1	3.3 V fixed LDO; 600 mA electrical rating Status: HOLD - THERMAL	4	0.37	1.48	Supplier
Dual op amp / AFE (U3)	Microchip MCP6002-I/SN	Dual RRIO op amp; 1.8-6 V operation Status: REVIEW - TRANSIENTS	4	0.42	1.68	Supplier
2-pin headers (J1-J3)	Samtec TSW-102-07-G-S	1 x 2 male header; 2.54 mm pitch Status: REVIEW - MECHANICAL	12	0.21	2.52	Supplier
4-pin headers (J5-J6)	Samtec TSW-104-07-G-S	1 x 4 male header; 2.54 mm pitch Status: REVIEW - MECHANICAL	8	0.38	3.04	Supplier
6-pin headers (J4, J7)	Samtec TSW-106-07-G-S	1 x 6 male header; 2.54 mm pitch Status: REVIEW - MECHANICAL	8	0.58	4.64	Supplier
Reverse-polarity Schottky diode (D1)	Vishay SS14-E3/61T	40 V reverse; 1 A Schottky rectifier Status: REVIEW - LOAD	4	0.47	1.88	Supplier
Piezo clamp diode (D2)	Diodes Incorporated BAT54S-7-F	Dual SERIES Schottky; 30 V reverse Status: REVIEW - TRANSIENTS	4	0.22	0.88	Supplier
On-board green indicator LEDs (D3-D4)	Kingbright APT2012SGC	Green 0805 LED; typical Vf 2.2 V Status: NOMINAL MATCH	8	0.20	1.60	Supplier
LED switching MOSFET (Q1)	Alpha & Omega Semiconductor AO3400A	30 V NMOS; RDS(on) <=48 mOhm at VGS=2.5 V Status: NOMINAL MATCH	4	0.52	2.08	Supplier
Resettable PTC fuse candidate (F1)	Littelfuse 1812L110/24DR	1.10 A hold at 20 C; 24 V; 1.95 A trip Status: REVIEW - REPLACEMENT	4	0.81	3.24	Supplier

Description	Manufacturer / part #	Key specification / status	Qty	Unit (\$)	Ext. (\$)	Purchase link
10 kOhm 0805 resistors (11 placements)	Yageo RC0805FR-0710KL	10k; 1%; 0.125 W Status: NOMINAL MATCH	44	0.10	4.40	Supplier
470 Ohm 0805 resistors (R5-R6)	Yageo RC0805FR-07470RL	470 ohm; 1%; 0.125 W Status: NOMINAL MATCH	8	0.10	0.80	Supplier
100 Ohm 0805 resistor (R7)	Yageo RC0805FR-07100RL	100 ohm; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
100 kOhm 0805 resistors (R8, R19)	Yageo RC0805FR-07100KL	100k; 1%; 0.125 W Status: NOMINAL MATCH	8	0.10	0.80	Supplier
2.2 kOhm 0805 resistor (R9)	Yageo RC0805FR-072K2L	2.2k; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
1 kOhm 0805 resistor (R10)	Yageo RC0805FR-071KL	1k; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
4.7 kOhm I2C pull-ups (R11-R12)	Yageo RC0805FR-074K7L	4.7k; 1%; 0.125 W Status: NOMINAL MATCH	8	0.10	0.80	Supplier
10 Ohm analog-rail resistor (R16)	Yageo RC0805FR-0710RL	10 ohm; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
1 MOhm piezo-bias resistor (R20)	Yageo RC0805FR-071ML	1M; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
47 kOhm gain resistor (R23)	Yageo RC0805FR-0747KL	47k; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
6.8 kOhm ADC divider resistor (R24)	Yageo RC0805FR-076K8L	6.8k; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
15 kOhm ADC divider resistor (R25)	Yageo RC0805FR-0715KL	15k; 1%; 0.125 W Status: NOMINAL MATCH	4	0.10	0.40	Supplier
22 uF / 10 V bulk capacitors (C1, C3)	Samsung Electro-Mechanics CL31A226KPHNNNE	22 uF; 10 V; X5R; +/-10% Status: REVIEW - DC BIAS	8	0.47	3.76	Supplier
100 nF decoupling/filter capacitors (9 placements)	Yageo CC0805KRX7R9BB104	100 nF; 50 V; X7R; +/-10% Status: NOMINAL MATCH	36	0.18	6.48	Supplier
10 uF / 10 V capacitors (C5, C8)	Samsung Electro-Mechanics CL21A106KPFNNWE	10 uF; 10 V; X5R; +/-10% Status: REVIEW - DC BIAS	8	0.21	1.68	Supplier

Description	Manufacturer / part #	Key specification / status	Qty	Unit (\$)	Ext. (\$)	Purchase link
1 uF / 25 V capacitors (C7, C10)	Murata GRM219R71E105KA88D	1 uF; 25 V; X7R; +/-10% Status: NOMINAL MATCH	8	0.26	2.08	Supplier
4.7 nF C0G ADC-filter capacitor (C12)	KEMET C0805C472K5GECAUTO	4.7 nF; 50 V; C0G; +/-10% Status: NOMINAL MATCH	4	0.27	1.08	Supplier
Reset and Boot switches (SW1-SW2)	Omron / Aratas B3F-1000	Normally-open momentary tactile switch Status: REVIEW - MECHANICAL	8	0.35	2.80	Supplier
Piezo sensors	PUI Audio AB2036B	External 20 mm piezo bender; 25 nF nominal, 3.6 kHz resonance. Short wires to J2. Drive-voltage ratings do not bound impact-generated transients. Status: REVIEW - PROTOTYPE	3	1.30	3.90	Supplier
OLED display	Adafruit Adafruit product 326	Additional display, not J5 itself. Power at 3.3 V. Wire GND / 3V3 / SCL / SDA by name. Verify worst-pattern current <=40 mA; do not assume connector order. Status: REVIEW - CURRENT	1	17.50	17.50	Supplier
USB-to-UART programmer	Adafruit Adafruit product 954	TX/RX are 3.3 V logic, but RED wire is +5 V. Leave red insulated. Black to J4-1, white RX to J4-2, green TX to J4-3; manual Boot/Reset. Status: REVIEW - WIRING	1	9.95	9.95	Supplier
Remote Start / Mode / Miss switches	Omron / Aratas B3F-1000	Extra switches beyond SW1/SW2 already on each PCB. Need separate mounting/perfboard and wiring. Dry contacts to J6 ground; no 5 V on input. Status: REVIEW - ASSEMBLY	3	0.35	1.05	Supplier
Prototype perimeter LEDs	Kingbright WP7113SGC	Optional starting assembly: 8 green 5 mm LEDs, each with its own 330-ohm resistor. Narrow viewing angle and 8.6 mm body need visibility/height testing. Not a finished perimeter product. Status: REVIEW - OPTIONAL	24	0.23	5.52	Supplier
Perimeter current-limit resistors	Yageo CFR-25JB-52-330R	330 ohm, 5%, 0.25 W, through-hole. External assembly only, not the R0805 board footprint. Each LED gets a resistor; no direct bare-LED connection to J3. Status: REVIEW - OPTIONAL	24	0.11	2.64	Supplier
External 5 V supply	Mean Well GST18U05-P1J	5 V / 3 A US wall adapter, center-positive 5.5 x 2.1 mm barrel. Needs mating connector, protected star harness to four J1 connectors, and loaded voltage check. Not directly pluggable into PCB headers. Status: REVIEW - HARNESS	1	14.10	14.10	Supplier
Bare PCBs	PCBWay / ECE 445 course order	2-layer, <=100 mm x 100 mm; 10 boards	1	5.00	5.00	Supplier

Description	Manufacturer / part #	Key specification / status	Qty	Unit (\$)	Ext. (\$)	Purchase link
Target impact plates	McMaster-Carr 8574K122 candidate	1/8 in x 12 in x 12 in clear polycarbonate; cut to target size; final material subject to rebound test	3	8.00	24.00	Supplier
Low-profile suction cups	SignSite SIGN_ACC_SCUPSM candidate	1.168 in diameter, #8-32 stud; final use subject to table-adhesion/no-damage test	12	1.40	16.80	Supplier
PCB enclosures / print material	Team-fabricated	Low-profile protective enclosure; dimensions finalized after PCB/target fit check	4	4.00	16.00	N/A - fabricated/lab stock
Wire, harness, strain relief	Lab stock / purchased hookup wire	5 V star power harness plus sensor/UI wiring and strain relief	1	15.00	15.00	N/A - fabricated/lab stock
Estimated parts total					195.90	

BOM note: supplier links identify the intended purchased part or candidate source. F1 and U2 remain engineering HOLD items, and fabricated/lab-stock rows are explicitly marked N/A rather than omitting sourcing information. All prices are planning estimates, not quotations.

Estimated grand total = labor (\$30,000) + parts (\$195.90) = \$30,195.90.

3.2 Schedule

The schedule assigns one primary task to each member every week, as required for clear division of labor. Member 1 owns hardware/PCB and analog bring-up; Member 2 owns firmware/wireless; Member 3 owns mechanical/UI work. All members still participate in integration and R&V, but each row below gives a single accountable task per member and a measurable weekly exit condition.

Table 10. Remaining Fall 2026 project schedule

Week	Member 1 - Hardware/PCB	Member 2 - Firmware/Wireless	Member 3 - Mechanical/UI	Shared exit condition
Sep 28-Oct 2	Freeze Rev B schematic/BOM; document F1/U2 risks.	Freeze packet format and firmware pin map.	Freeze target dimensions/suction-cup prototype plan.	Design Document complete; open review issues documented.
Oct 5-9	Run ERC/DRC/parity and footprint audit; incorporate Design Review feedback.	Build UART/ESP32 smoke-test firmware and test packet structs.	Build first target plate mock-up and verify suction-cup attachment concept.	Fabrication candidate reviewed by team/TA.
Oct 12-16	Breadboard power + AFE; measure 3.3 V rail, VREF, ADC baseline.	Implement ≥ 20 ksample/s acquisition and serial logging.	Run plate material and rebound pilot tests; finalize enclosure concept.	Measured piezo waveform and power-stage evidence captured.
Oct 19-23	Assemble and staged-power-up first PCB; characterize gain/clamp/thermal behavior.	Program first board; implement threshold/lockout detector.	Mount piezo/LED assembly on first mechanical target.	One complete target detects real ball impacts.
Oct 26-30	Assemble remaining boards and repair assembly faults.	Implement ESP-NOW addressing, trial IDs, ACK/retry, duplicate rejection.	Build remaining two targets and central-controller enclosure/buttons.	Three targets + controller communicate on bench.
Nov 2-6	Measure supply ripple and LED-switching interference.	Implement Rapid-Fire state machine and statistics.	Run 3 m LED visibility and cable-routing checks.	20-trial Rapid-Fire session operates end-to-end.
Nov 9-13	Support any hardware fixes from integrated testing.	Implement Serve Accuracy mode and OLED/UI updates.	Run formal rebound, stability, and movement tests.	Both required modes and mechanical requirements functional.
Nov 16-20	Execute power/AFE R&V and thermal measurements.	Execute wireless/UI/latency R&V and fix firmware defects.	Execute mechanical/visibility R&V and finalize strain relief.	Complete preliminary R&V matrix with saved raw evidence.
Nov 23-27	Analyze hardware test data; prepare only necessary ECOs.	Code cleanup, comments, release tagging, and log formatting.	Documentation photos/CAD cleanup; no architecture changes.	Fall-break buffer; design frozen except verified corrective fixes.

Week	Member 1 - Hardware/PCB	Member 2 - Firmware/Wireless	Member 3 - Mechanical/UI	Shared exit condition
Nov 30-Dec 4	Own hardware readiness and spare-board plan for demo.	Own demo firmware build and configuration backup.	Own target setup, table layout, and user-facing demo flow.	Final demonstration and presentation completed.
Dec 7-10	Write hardware verification/cost sections of final report.	Write software/wireless verification sections.	Write mechanical/societal/safety sections; assemble figures.	Final report/notebooks/archive submitted.

4. Discussion of Societal Impact, Engineering Standards, Ethics, and Safety Considerations

4.1 Societal, Economic, Environmental, Cultural, and Global Impact

The project is intended to improve access to structured table-tennis practice by allowing one player to perform repeatable placement drills without requiring a second person to call locations and keep score. This is a modest welfare contribution rather than a medical or safety-critical intervention: the system supports recreation, skill development, and quantitative feedback. Because it attaches to an existing table instead of replacing the table, the design also lowers the economic barrier to use in clubs, schools, and recreational spaces.

Economically, using the same universal PCB in all four electronic units reduces non-recurring design effort and spare-part variety. Environmentally, the design avoids custom rechargeable batteries and instead uses one external low-voltage supply. Removable targets and modular boards can be repaired independently rather than discarding a complete specialized table. Culturally and globally, the primary cue is visual illumination and the controller output is numeric, so the core training interaction requires little language localization.

4.2 Engineering Standards and Regulatory Considerations

The project is a low-voltage educational prototype rather than a certified consumer product, but applicable wireless, electrical-safety, laboratory, and cord-management standards are used as design constraints. UL/CSA 62368-1 is used as a hazard-based safety reference for AV/ICT electronics [19], while FCC Part 15 and IEEE 802.11-related requirements govern the integrated 2.4 GHz radio implementation [3], [14].

- IEEE 802.11 / ESP32-S3 radio implementation: the selected ESP32-S3-WROOM-02 module contains a 2.4 GHz Wi-Fi/Bluetooth radio. ESP-NOW uses that radio for peer-to-peer communication; the team will follow Espressif antenna-clearance and supply recommendations [3], [7].
- 47 CFR Part 15, including Section 15.247: the 2.4 GHz radio operates in the 2400-2483.5 MHz ISM band under intentional-radiator rules. The project uses an integrated commercial RF module and will not modify the module RF power stage or antenna [14].
- ECE 445 PCB and verification guidance: board release requires programming access, appropriate connectors, power traces, test points, ground planes/stitching, hand-solderable parts, DRC, and a verification plan driven by quantitative subsystem requirements [9], [18].
- OSHA flexible-cord principles are applicable to the user-facing low-voltage power harness: cables will be protected from mechanical damage and provided with strain relief where they enter enclosures [15].

Table 11. Standards and safety design response

Standard / guidance	Why it applies	Concrete design response
IEEE 802.11 / Espressif ESP-NOW	2.4 GHz radio link between targets and controller.	Use the certified ESP32-S3-WROOM-02 RF module, preserve antenna clearance, and verify the required 5 m indoor link.
47 CFR Part 15.247	Intentional radiator operation in the 2400-2483.5 MHz band.	Do not modify the module RF section or transmit outside approved module/channel settings; retain the commercial RF module implementation.
UL/CSA 62368-1 (safety reference)	Hazard-based safety standard for AV/ICT electronic equipment; relevant as a safety-	Keep mains confined to a commercial external adapter, use only SELV/low-voltage rails on custom boards, enclose electronics, and

Standard / guidance	Why it applies	Concrete design response
	design reference for the powered controller/target electronics.	provide overcurrent/reverse-polarity protection.
OSHA 29 CFR 1910.305 / flexible-cord principles	Low-voltage cords can still create damage, snag, or strain-relief hazards.	Route cables toward/under the table, add strain relief, remove damaged cords from use, and keep connectors out of the player path.
ECE 445 laboratory safety and PCB review guidance	Governs safe development, board release, and lab practice.	Use current-limited staged power-up, complete safety training, avoid working alone where prohibited, and require ERC/DRC/TA review before fabrication.

These standards are not treated as a claim of product certification. They are used to drive specific design choices: isolate users from mains voltage, keep custom electronics at 5 V/3.3 V, protect the power path, secure wiring, preserve the RF module antenna region, and verify the final assembly before normal play.

4.3 Ethics

The IEEE Code of Ethics requires engineers to make decisions consistent with public safety and welfare and to be honest and realistic about technical claims [12]. For this project, that means reporting measured impact accuracy, wireless reliability, rebound behavior, and failure modes rather than describing an unverified prototype as reliable. A 90% requirement is not reported as 100% success, and unresolved power or sensing risks remain documented until tested.

The ACM Code of Ethics similarly emphasizes contributing to society and avoiding harm [13]. The system does not require cameras, microphones, cloud accounts, or biometric data, so the required design intentionally minimizes privacy exposure. If future work adds stored player identities or cloud logging, that would introduce a new privacy/security review rather than being silently added to the base system. The optional response-time metric will be labeled as target-response time rather than pure human reaction time because it also contains stroke and ball-flight delay.

4.4 Electrical and Mechanical Safety

The user-accessible system operates from a commercial 5 V wall supply and local 3.3 V rails. Mains voltage remains enclosed inside the commercial adapter and is not present on a custom PCB. The custom input path includes overcurrent and reverse-polarity protection, and initial bring-up uses a current-limited bench supply. During development, team members will follow the ECE 445 requirement that nobody work alone in the senior design lab and that required safety training be completed [11].

Mechanical hazards are dominated by trip/snag risks, target movement, loose wiring, and sharp/protruding hardware. Cables are routed toward and underneath the table and secured with strain relief. Suction cups and plate edges are inspected before use. The PCB is enclosed away from the primary impact region, and conductive or sharp hardware is kept away from the ESP32 antenna and the player-facing surface. Because a target changes the bounce surface, rebound behavior is itself a safety/usability verification item: a target that stops the ball unpredictably or releases from the table is not acceptable.

4.5 Safety Procedures

1. Before first power, inspect polarity, connector orientation, solder bridges, and resistance from each power rail to ground with power removed.
2. Populate and test the input protection/regulator stage before installing the ESP32 and analog ICs. Apply 5 V from a bench supply with a low current limit and stop immediately if the supply current-limits unexpectedly or any component heats rapidly.
3. After MCU installation, increase the current limit only to the level required for ESP32 startup. Keep external LEDs and OLED disconnected until UART programming, reset, and 3.3 V regulation are verified.
4. Characterize the piezo with an oscilloscope at low gain first. Verify the clamp/ADC node before switching to the high-gain option.
5. Route final low-voltage cables underneath the table, provide strain relief, and keep connectors out of the player movement area. Do not operate the system with damaged cables.

6. Before each play session, verify all suction cups are seated, the target is flat, enclosure screws are secure, and no sharp edge or loose wire is exposed.
7. Run wireless and impact tests using table-tennis balls only; do not strike the electronic targets with hard tools as a substitute for normal use.
8. Document any failed protection device, overheated regulator, repeated false trigger, or mechanical release and correct the root cause before continuing integrated testing.

5. References

- [1] T. Belli et al., “Reproducibility and Validity of a Stroke Effectiveness Test in Table Tennis Based on the Temporal Game Structure,” *Frontiers in Psychology*, vol. 10, art. 427, Feb. 2019, doi: 10.3389/fpsyg.2019.00427. Available: <https://www.frontiersin.org/journals/psychology/articles/10.3389/fpsyg.2019.00427/full>
- [2] PUI Audio, “AB2036B Piezo Bender,” product specifications. [Online]. Available: <https://puiaudio.com/product/benders/AB2036B>. Accessed: Oct. 2, 2026.
- [3] Espressif Systems, “ESP32-S3-WROOM-02 & ESP32-S3-WROOM-02U Datasheet,” ver. 1.7, Mar. 2026. Available: https://documentation.espressif.com/esp32-s3-wroom-02_datasheet_en.pdf
- [4] Microchip Technology Inc., “MCP6001/1R/1U/2/4 1 MHz, Low-Power Op Amp,” datasheet. Available: <https://ww1.microchip.com/downloads/en/DeviceDoc/MCP6001-1R-1U-2-4-1-MHz-Low-Power-Op-Amp-DS20001733L.pdf>
- [5] Diodes Incorporated, “AP2112 600mA CMOS LDO Regulator with Enable,” datasheet. Available: <https://www.diodes.com/assets/Datasheets/AP2112.pdf>
- [6] Alpha & Omega Semiconductor, “AO3400A 30 V N-Channel MOSFET,” datasheet. Available: <https://www.aosmd.com/sites/default/files/res/datasheets/AO3400A.pdf>
- [7] Espressif Systems, “ESP-NOW,” ESP-IDF Programming Guide. Available: https://docs.espressif.com/projects/esp-idf/en/stable/esp32s3/api-reference/network/esp_now.html
- [8] Adafruit Industries, “Monochrome 0.96 in 128x64 OLED Graphic Display - SSD1306,” Product 326. Available: <https://www.adafruit.com/product/326>
- [9] University of Illinois Urbana-Champaign, ECE 445 Senior Design Laboratory, “Requirements and Verification.” Available: <https://courses.grainger.illinois.edu/ece445/guidelines/requirements-and-verification.asp>
- [10] University of Illinois Urbana-Champaign, ECE 445 Senior Design Laboratory, “Design Review.” Available: <https://courses.grainger.illinois.edu/ece445/guidelines/design-review.asp>
- [11] University of Illinois Urbana-Champaign, ECE 445 Senior Design Laboratory, “Safety.” Available: <https://courses.grainger.illinois.edu/ece445/guidelines/safety.asp>
- [12] IEEE, “IEEE Code of Ethics.” Available: <https://www.ieee.org/about/corporate/governance/p7-8.html>
- [13] Association for Computing Machinery, “ACM Code of Ethics and Professional Conduct.” Available: <https://www.acm.org/code-of-ethics>
- [14] Federal Communications Commission, “47 CFR Sec. 15.247 - Operation within the bands 902-928 MHz, 2400-2483.5 MHz, and 5725-5850 MHz.” Available: <https://www.ecfr.gov/current/title-47/chapter-I/subchapter-A/part-15/subpart-C/section-15.247>
- [15] Occupational Safety and Health Administration, “29 CFR 1910.305 - Wiring methods, components, and equipment for general use.” Available: <https://www.osha.gov/laws-regs/regulations/standardnumber/1910/1910.305>
- [16] Mean Well, “GST18U Series 18 W AC-DC Reliable Green Industrial Adaptor,” datasheet. Available: <https://www.meanwellusa.com/upload/pdf/GST18U/GST18U-spec.pdf>
- [17] Littelfuse, “1812L Series Resettable PTCs,” datasheet. Available: <https://www.littelfuse.com/assetdocs/resettable-ptcs-1812l-datasheet>
- [18] University of Illinois Urbana-Champaign, ECE 445 Senior Design Laboratory, “Board Review.” Available: <https://courses.grainger.illinois.edu/ece445/guidelines/board-review.asp>
- [19] UL Solutions, “Navigating the Requirements of UL/CSA 62368-1, 4th Edition,” 2025. [Online]. Available: <https://www.ul.com/insights/navigating-requirements-ulcsa-62368-1-4th-edition>. Accessed: Oct. 2, 2026.