

Adaptive Power Factor Correction Device

Design Document:

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Introduction:

Problem:

Power factor (PF) correction is an important process in commercial electrical systems because many common loads, such as motors and transformers, are inductive. A poor power factor causes a system to draw more current and apparent power for the same amount of real power, increasing system losses, reducing available electrical capacity, and potentially increasing equipment and utility costs. Power factor correction, also known as reactive power compensation, improves power factor toward unity by supplying compensating reactive power. Because most commercial loads are inductive, this is commonly accomplished using capacitor banks.

Existing power factor correction solutions are often either non-adaptive or designed for large-scale commercial and industrial applications. Systems such as commercial automatic capacitor banks can be expensive and oversized for smaller commercial tenants, making them impractical for installation at the individual tenant-panel level.

There is therefore a need for a low-cost, adaptive power factor correction device that can be implemented at the tenant-panel level.

Solution:

Our project aims to establish the groundwork for an adaptive power factor correction system that could eventually be scaled to a commercial 480 Volt (V) electrical panel. The system will dynamically adjust reactive power compensation as load conditions change, helping reduce unnecessary current draw, electrical losses, equipment requirements, and potential utility costs.

To accomplish this, we are designing and implementing a single phase adaptive power factor correction prototype operating from a 15 V AC source. This allows the system to demonstrate the same sensing, computation, and capacitor-switching concepts at a voltage that is manageable for laboratory development and testing.

The system has four main subsystems:

1. **Sensing** – Measures the Alternating Current (AC) voltage and current waveforms and conditions them into signals that can be safely sampled by the microcontroller.
2. **Microcontroller Unit (MCU)** – Samples the voltage and current signals, computes root mean squared values (RMS) voltage and current, real power, apparent power, reactive power, and power factor, and determines the required capacitive compensation.
3. **Capacitive Switching** – Uses photomos relays for switching to connect or disconnect discrete capacitor stages in parallel with the load based on commands from the microcontroller.
4. **AC-to-DC Power Conversion** – Converts the 15 V AC input into approximately 3.3 V Direct Current (DC) to provide the low-voltage power supply required by the microcontroller and supporting electronics.

During operation, the microcontroller continuously samples the voltage and current waveforms and calculates the current power factor. The controller evaluates whether compensation changes are required at approximately 10-second intervals. To prevent unnecessary switching caused by small fluctuations or measurement noise, the controller will only modify the connected capacitor stages if the measured power factor changes by more than a predefined threshold, initially expected to be approximately 0.04.

If an adjustment is required, the controller determines the amount of reactive power compensation needed and selects the appropriate combination of discrete capacitor stages. Capacitors are then switched into or out of the circuit using isolated photomos relays. Switching is synchronized with the AC waveform to reduce switching transients and inrush current, while bleeder resistors allow disconnected capacitors to discharge safely.

The final prototype will demonstrate adaptive power factor correction using a variable inductive load supplied from 15 V AC. As the load changes, the system will detect the resulting change in power factor and, when the change exceeds the defined threshold, automatically adjust the connected capacitance to maintain the power factor near the desired target of approximately 0.95. To reasonably meet this goal with a manageable amount of capacitors we will have a target range for PF of 0.93 - 0.97.

Visual Aid:

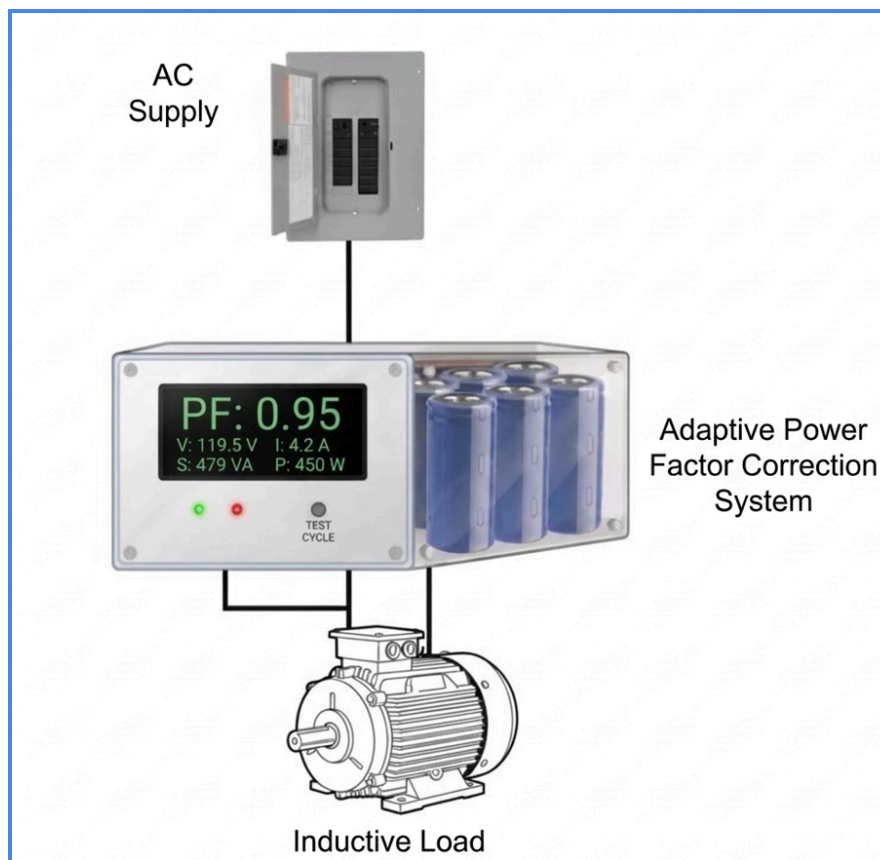


Figure 1: Visual Aid

High Level Requirements:

1. The system shall measure AC voltage and current waveforms at 60 Hz and compute power factor with an absolute accuracy of ± 0.05 compared to a calibrated reference measurement device under steady-state operating conditions.
2. The system shall sample voltage and current waveforms at a rate between 5 kHz and 10 kHz with a maximum inter-channel timing mismatch of 10 μ s to ensure accurate waveform reconstruction, phase detection, and real-time power factor calculation.
3. The system shall dynamically adjust reactive compensation to maintain the load power factor within the range of 0.93 to 0.97 under steady-state conditions, and shall achieve this correction within 2 seconds following a step change in load.
4. The system shall perform capacitor switching only at or within ± 1 ms of AC voltage zero-crossings and limit inrush current to within the safe operating limits of the switching components.

Design:

Block Diagram:

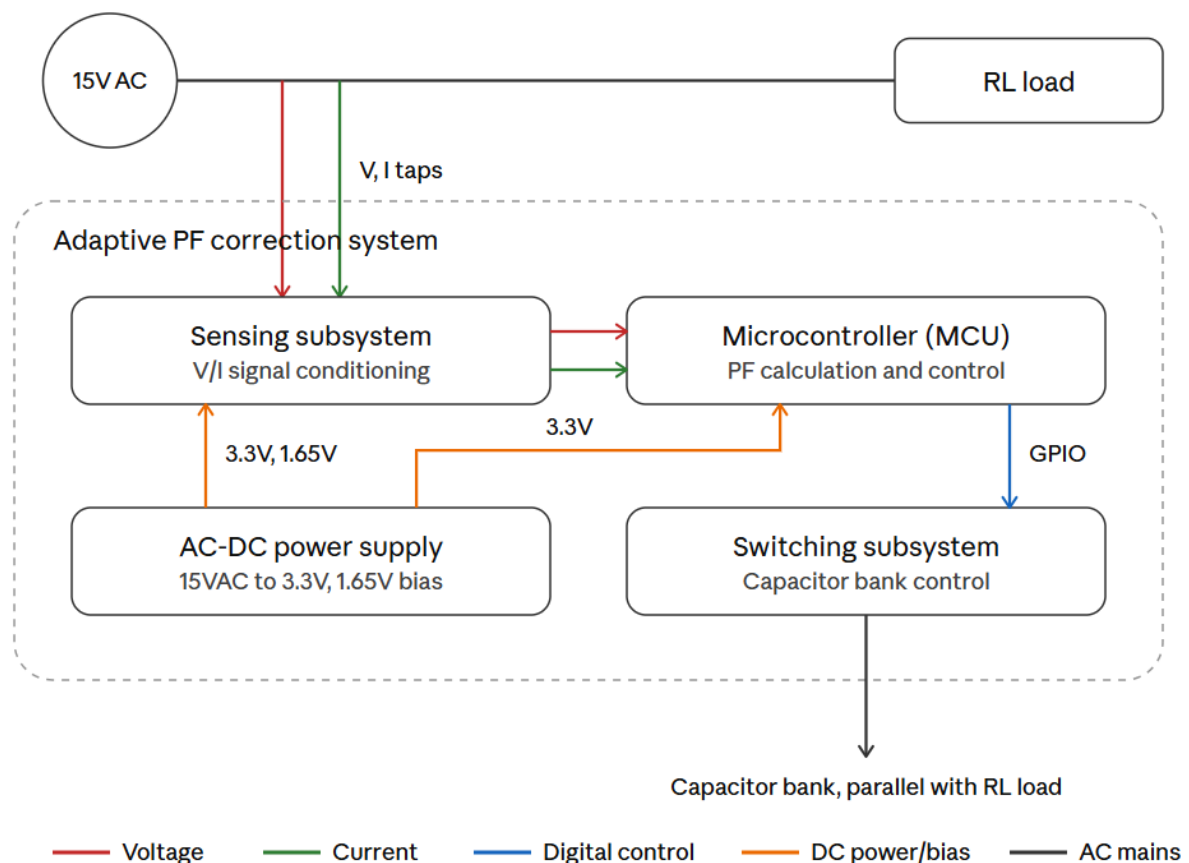


Figure 2: High Level Block Diagram

Sensing Subsystem:

Overview:

The sensing subsystem measures the AC voltage and current of the load and converts them into analog signals that are adjusted for the microcontroller's analog to digital converter (ADC) inputs. This subsystem directly interacts with the AC load and provides real-time waveform data to the MCU subsystem for power factor computation and control decisions.

The voltage sensing block uses a resistive voltage divider and a biasing network that shifts the scaled AC waveform into the appropriate input range of the ADC. The current sensing block uses a current transformer to scale the current and produce a proportional signal, which is also biased to match the ADC input parameters.

Both sensing blocks will rely on a reference voltage that is provided by the DC Power Supply subsystem so that the AC waveforms stay within the 0–3.3 V ADC range. The outputs will be continuous-time analog signals that represent the original voltage and current waveforms with accurate amplitude and phase information so the MCU subsystem can accurately reconstruct the signals and perform power factor calculations.

The key design considerations for this subsystem include input signal integrity, minimizing phase difference errors (for accurate PF calculations), and ensuring that all signals remain within safe voltage limits for the ADC. Filtering may be added to reduce high-frequency noise without significantly distorting the waveform or introducing phase shift.

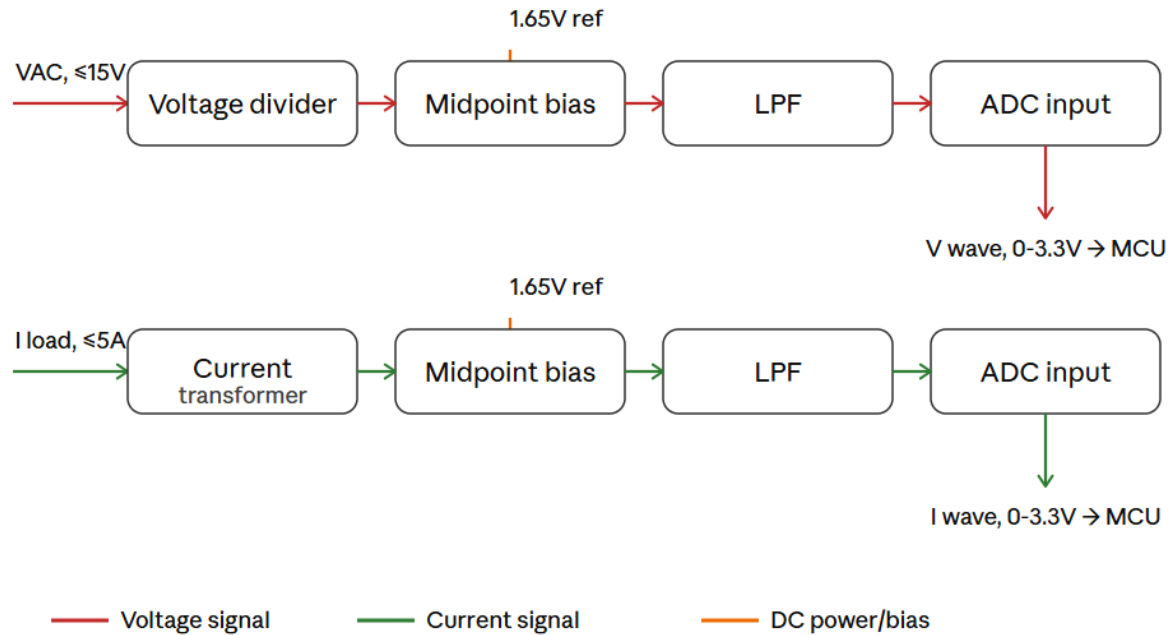


Figure 3: Sensing System Block Diagram

Voltage Scaling Stage

The AC input voltage (15 V RMS, ~21.2 V peak) is scaled down using a resistive voltage divider to a level compatible with the ADC.

$$V_{out} = V_{in} \frac{R_2}{R_1 + R_2} \quad (1)$$

Using example values:

- $R_1 = 100\text{k}\Omega$
- $R_2 = 10\text{k}\Omega$

$$V_{out} \approx 21.2 \frac{10}{110} \approx 1.93\text{V} \quad (2)$$

This ensures the waveform amplitude remains safely within the ADC range after biasing.

A resistive divider is selected due to its simplicity, linearity, and low cost. Since the system operates at low voltage, isolation is not required for this prototype.

Current Sensing

Load current is measured using a current transformer (SCT-013-005), which produces a proportional voltage output (1 V at full-scale current).

Key characteristics:

- Rated current: 5 A
- Output: 1 V (with built-in burden resistor)

The CT provides:

- Electrical isolation
- Minimal insertion loss
- Linear scaling of current

The output voltage is proportional to the instantaneous current waveform, preserving phase information required for power factor calculation.

AC Coupling and Biasing

Both voltage and current signals are AC-coupled and biased to shift the waveform into the ADC input range.

Since the ADC cannot measure negative voltages, a DC offset is added:

$$V_{\text{biased}} = V_{\text{signal}} + 1.65 \text{ V} \quad (3)$$

This is implemented using:

- Coupling capacitor ($\approx 1 \mu\text{F}$)
- Bias network (from DCPS Subsystem)
- Buffered reference (op-amp)

The resulting waveform:

- Oscillates around 1.65 V
- Remains within 0–3.3 V

Biasing is used instead of rectification to preserve waveform shape and phase information. Rectification would eliminate phase information and prevent accurate computation of real power and power factor.

Signal Conditioning

A low-pass RC filter is applied to both signals to reduce high-frequency noise while preserving the 60 Hz fundamental.

Example:

- $R = 1k\Omega$
- $C = 100nF$

$$f_c = \frac{1}{2\pi RC} \approx 1.6kHz \text{ (4)}$$

This cutoff frequency is much higher than 60 Hz so there's no distortion of signal, and low enough to attenuate switching and environmental noise

An op-amp buffer (MCP6002) is used to provide low output impedance, stabilize the bias voltage, and to prevent loading effects from the ADC

Sensing Subsystem Requirements and Verification:

Requirement:	Verification:
The voltage sensing circuit should scale the input AC waveform to a range of 0–3.3 V for a 15 V RMS input.	Apply 15 V RMS sinusoidal input. Measure output of sensing circuit using oscilloscope. Verify waveform remains within ADC range with no clipping. Record waveform image.
The sensing output should be centered at $1.65 \text{ V} \pm 50 \text{ mV}$.	Measure DC offset of waveform using oscilloscope mean measurement. Confirm center voltage lies within specified tolerance.
The sensing subsystem should preserve waveform shape with less than 5% amplitude distortion.	Compare input waveform and sensed waveform using oscilloscope (dual channel). Measure peak amplitudes and calculate percent difference.
The current sensing circuit should produce a proportional voltage corresponding to load current within $\pm 5\%$ accuracy over 0–5 A range.	Pass known AC current through load (use known resistor + AC source). Measure CT output voltage and compare against expected scaling. Record error difference.
The sensing subsystem should support signal frequencies up to 500 Hz without attenuation greater than 3 dB.	Inject sinusoidal signals at increasing frequencies (60 Hz $\rightarrow$ 500 Hz). Measure output amplitude and compare to 60 Hz baseline. Plot frequency response.

DC Power Supply Subsystem (DCPS):

Overview:

The DC power supply subsystem converts the 15 V AC input into regulated DC voltages used to power the microcontroller and supporting electronics, while also generating a stable reference voltage for signal biasing in the sensing subsystem. This subsystem interfaces with all other subsystems by supplying the primary power rails, a common ground reference, and the mid-supply bias voltage used for ADC signal conditioning.

The power conversion path is as follows:

AC Input → Rectifier → Filter → Voltage Regulator → Bias Generation

The AC input is first rectified to produce a pulsating DC signal, which is smoothed out using a filtering stage (bulk capacitor) to reduce ripple. The resulting DC voltage is regulated to 5 V using a buck converter, followed by a linear regulator to generate a stable 3.3 V rail for the microcontroller and associated circuitry. A mid-supply reference voltage of ~1.65 V is taken from the regulated rail and used by the sensing subsystem to bias AC signals into the ADC input range.

The key design considerations for this subsystem include maintaining voltage regulation accuracy, minimizing ripple and noise, sufficient current delivery, and providing a stable ground reference. Bias voltage stability is especially important, since fluctuations directly impact measurement accuracy in the sensing subsystem.

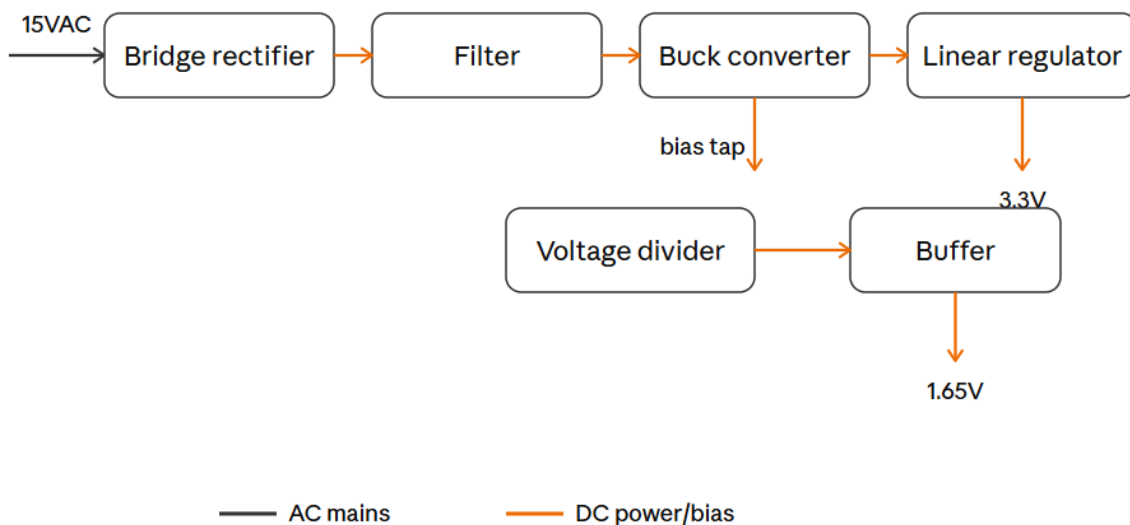


Figure 4: DC Power Supply Block Diagram

AC-to-DC Rectification

A full-bridge rectifier (B40C2300) is used to convert the 15 V RMS AC input into a pulsating DC signal.

$$V_{\text{peak}} = 15\sqrt{2} \approx 21.2\text{V} \quad (5)$$

Accounting for two diode drops (~ 0.7 V each):

$$V_{\text{DC}} \approx 21.2\text{V} - 1.4\text{V} \approx 19.8\text{V} \quad (6)$$

A bridge rectifier is selected over a center-tapped configuration to eliminate the need for a specialized transformer and simplify implementation.

Filtering Stage

A 3300 μF electrolytic capacitor is used to smooth the rectified waveform by adding approximately linear discharge voltage from the capacitor between the rectified waves.

The ripple voltage is estimated using:

$$\Delta V = \frac{I}{fC} \quad (7)$$

Assuming:

- Load current: 100 mA
- Ripple frequency: 120 Hz

$$\Delta V = \frac{0.1}{120 * 3300\mu\text{F}} = 0.25\text{V} \quad (8)$$

This ensures a relatively stable DC input for the switching regulator.

Buck Converter

A switching regulator (LM2596S-5) steps the ~20V DC input down to a regulated 5V output.

Key components:

- Inductor: 40 μ H
- Output capacitor: 300 μ F
- Freewheeling diode: Schottky (More efficient, cleaner switching, less voltage drop)

The feedback pin is connected to the output node after the inductor to ensure proper voltage regulation.

The buck converter is selected for its high efficiency (>75%), reducing thermal losses compared to a linear regulator.

Linear Regulator

An AMS1117-3.3 linear regulator converts the 5V rail to a clean 3.3V supply for the microcontroller and analog circuitry.

Input and output capacitors (10 μ F) are included to ensure regulator stability.

Power dissipation:

$$P = (5 - 3.3) * I \quad (9)$$

For a 200 mA load:

$$P = 1.7 * 0.2 = 0.34 \text{ W} \quad (10)$$

This is within safe limits for the package with PCB heat dissipation.

Bias Voltage Generation

A resistor divider (10k Ω / 10k Ω) generates a mid-supply reference:

$$V_{bias} = V_{in} \frac{R_2}{R_1 + R_2} = 3.3 \frac{10k}{2(10k)} = \frac{3.3}{2} = 1.65V \quad (11)$$

This voltage is buffered using an MCP6002 op-amp in a unity-gain configuration to provide a low-impedance reference for ADC inputs.

DC Power Supply Subsystem Requirements and Verification:

Requirement:	Verification:
The power supply should provide a regulated output voltage of 5.0 V $\pm$ 5% for load currents from 0 to 300 mA.	Use a DC electronic load or a resistor bank to draw currents from 0 to 300 mA in 50 mA increments. Measure output voltage using a digital multimeter or oscilloscope at each load point. Record results in a table and verify that all values fall within 4.75–5.25 V.
The power supply should provide a regulated output voltage of 3.3 V $\pm$ 2% for load currents from 0 to 150 mA.	Apply load using a resistor bank. Measure output at LDO output using DMM. Record voltage at multiple load points and confirm values remain between 3.234 V and 3.366 V.
The 5V rail should have peak-to-peak ripple less than 100 mV under full load.	Connect oscilloscope probes across 5V output capacitor. Set scope to AC coupling. Measure ripple at maximum load (300 mA). Record waveform and peak-to-peak voltage.
The system should generate a stable bias voltage of 1.65 V $\pm$ 50 mV.	Measure bias node using digital multimeter. Confirm voltage remains within 1.60–1.70 V under normal operation. Also observe with oscilloscope for noise (<20 mV ripple).
The power supply should operate from a 15 V RMS $\pm$ 10% AC input without failure. .	Use variable AC source (or transformer tap variation). Sweep input from 13.5V to 16.5V RMS. Verify outputs remain within regulation limits.

Microcontroller Subsystem:

Overview

The microcontroller subsystem is the computational core of the adaptive power factor correction system. It samples the conditioned voltage and current signals from the sensing subsystem, computes real-time power factor, and determines the reactive power compensation needed to bring the system into the target operating window.

MCU Selection: The subsystem will use a microcontroller for three key features: (1) dual, hardware-synchronizable ADC channels, allowing simultaneous sampling of voltage and current so that phase information is preserved; (2) a hardware timer capable of triggering ADC conversions at a fixed rate without CPU intervention, ensuring consistent sample spacing; and (3) an onboard hardware floating-point unit (FPU), which allows the RMS, power, and power factor calculations to be performed efficiently in real time.

A hardware timer is configured to trigger simultaneous ADC conversions on the voltage and current channels at 5–10 kHz. Samples are transferred via DMA (Direct Memory Access) directly into memory buffers, avoiding CPU-induced timing jitter that would otherwise distort the phase relationship between the two signals. Each buffer captures multiple full AC cycles to support averaged, cycle-aligned calculations.

Because the sensing subsystem biases both waveforms to sit within the ADC's input range, the MCU first removes this DC offset from each sample to recover the original zero-centered waveform, then scales the result using the known voltage-divider and current-transformer ratios to obtain true voltage and current values.

Power and Power Factor Calculation

Using the reconstructed waveforms, the MCU computes the root-mean-square (RMS) voltage and current:

$$V_{rms} = \sqrt{[(1/N) \sum v(t)^2]} \quad (12)$$

$$I_{rms} = \sqrt{[(1/N) \sum i(t)^2]} \quad (13)$$

The apparent power is calculated as:

$$S = V_{rms} \times I_{rms} \quad (14)$$

Real power is calculated by averaging the instantaneous power over an integer number of AC cycles:

$$P = (1/N) \sum v(t) \times i(t) \quad (15)$$

The power factor is calculated as:

$$PF = P/S \quad (16)$$

For the predominantly inductive, sinusoidal load, reactive power is calculated as:

$$Q = \sqrt{S^2 - P^2} \quad (17)$$

Where:

V_{rms} = RMS voltage (V)

I_{rms} = RMS current (A)

$v(t_n)$ = instantaneous voltage at sample n (V)

$i(t_n)$ = instantaneous current at sample n (A)

N = number of samples over an integer number of AC cycles

P = real power (W)

S = apparent power (VA)

PF = power factor (dimensionless)

Q = reactive power (VAR)

The conditioned voltage signal is passed through a comparator circuit that produces a clean digital pulse at each zero crossing. This pulse is routed to an MCU General Purpose Input Output (GPIO) pin configured as an external interrupt (EXTI). On each interrupt, the MCU timestamps the crossing using a free-running hardware timer. This timing information serves two purposes: aligning the RMS/power calculation window to whole AC cycles, and synchronizing capacitor-switching commands to the switching subsystem.

Approximately every 10 seconds, the MCU evaluates the measured power factor and determines whether a change in compensation is required. If correction is needed, the MCU calculates the required reactive power compensation and selects the closest available combination from the seven binary-weighted capacitor stages of 1, 2, 4, 8, 16, 32, and 64 μ F. The measured capacitance of each stage will be stored in firmware so that stage selection is based on actual rather than nominal capacitance.

For each capacitor stage, the MCU provides separate control outputs for the main switching device and the inrush-resistor bypass device. When enabling a stage, the main switching command is synchronized with the AC waveform. The bypass command is then asserted two full AC cycles, approximately 33.3 ms at 60 Hz, after the main command so that the capacitor inrush transient has time to decay before the inrush-limiting resistor is bypassed. A disconnected stage will not be re-enabled for at least 10 seconds to allow its bleeder resistor to discharge the capacitor.

The MCU initializes all switching-control outputs to the inactive state during startup and reset. The subsystem also outputs live values including RMS voltage, RMS current, real power, apparent power, reactive power, power factor, and active capacitor stages through the universal asynchronous receiver-transmitter (UART) interface for testing and demonstration.

Other Useful calculations for MCU:

Samples per AC Cycle:

At a 60 Hz line frequency and a 6 kHz sampling rate,

$$N = f_s / f = 6000 / 60 = 100 \text{ samples/cycle}$$

This gives exactly 100 samples per 60 Hz cycle, which simplifies cycle-aligned RMS, real power, and power factor calculations.

ADC Resolution:

For a 12-bit ADC with a 3.3 V input range,

$$\text{ADC resolution} = 3.3 \text{ V} / 4096 = 0.806 \text{ mV/count}$$

For a conditioned waveform with approximately 1 V peak amplitude,

$$\text{Quantization percentage} = 0.806 \text{ mV} / 1 \text{ V} \times 100\% = 0.081\%$$

This shows that ADC quantization error is small compared with the $\pm 2\%$ power measurement accuracy requirement.

Sampling Timing Error:

For a 60 Hz signal and a 5 μs timing mismatch between the voltage and current samples,

$$\Delta\phi = 2\pi(60)(5 \times 10^{-6}) = 0.108^\circ$$

$$\text{At PF} = 0.1, \phi = \cos^{-1}(0.1) = 84.26^\circ$$

PF error ≈ 0.00188 , or 1.88% relative error.

This shows that keeping the voltage-current sampling mismatch below 5 μs keeps the timing-related PF error below the $\pm 2\%$ requirement.

Sampling Buffer Size:

For a 6 kHz sampling rate averaged over 6 AC cycles,

$$N = 6000 \times (6 / 60) = 600 \text{ samples/channel}$$

For two channels with 16-bit storage,

$$\text{Memory} = 600 \times 2 \text{ channels} \times 2 \text{ bytes}$$

Memory = 2400 bytes

This shows that the MCU can easily store several complete AC cycles for cycle-aligned averaging and power calculations.

Capacitor Stage Combinations:

With 7 independently controlled capacitor stages,

Number of possible combinations = $2^7 = 128$

The MCU can evaluate all 128 possible stage combinations using the measured capacitance values and select the combination closest to the required compensation.

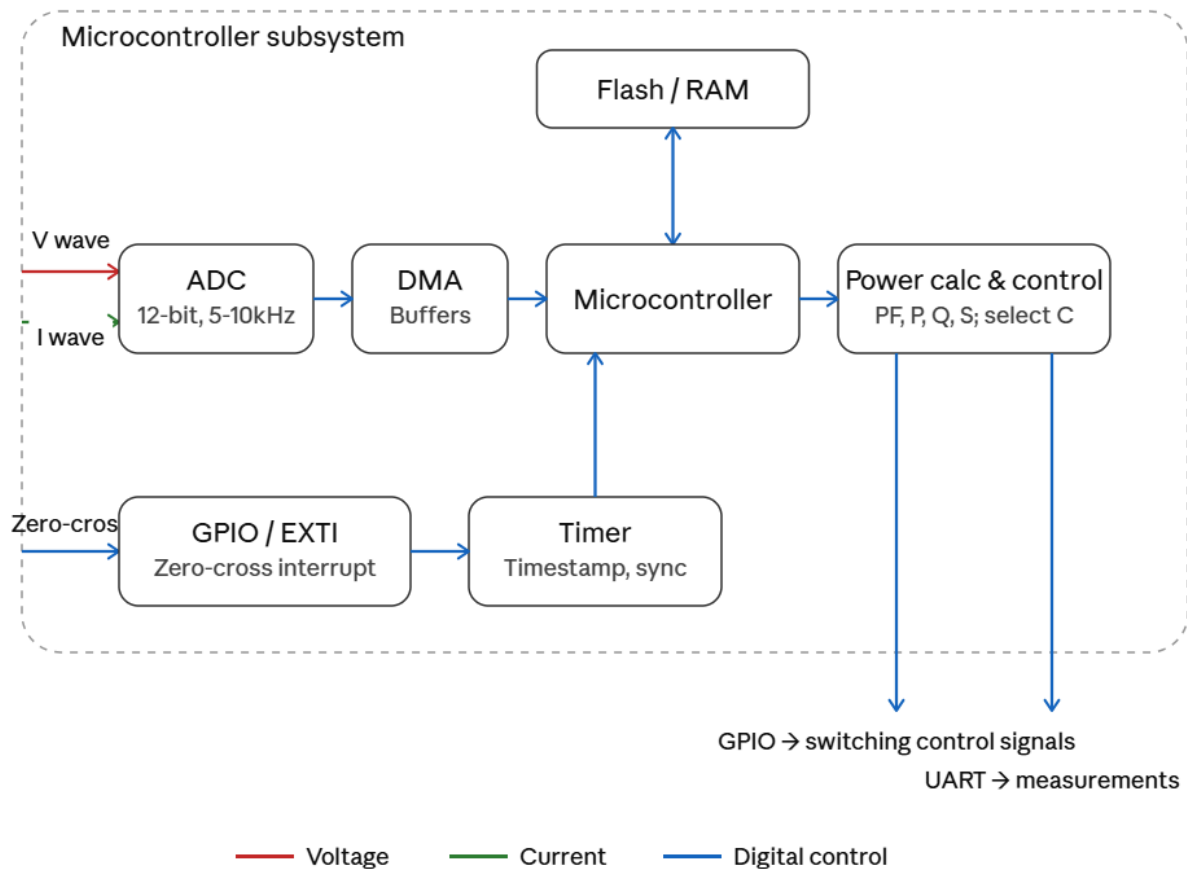


Figure 5: MCU System Block Diagram

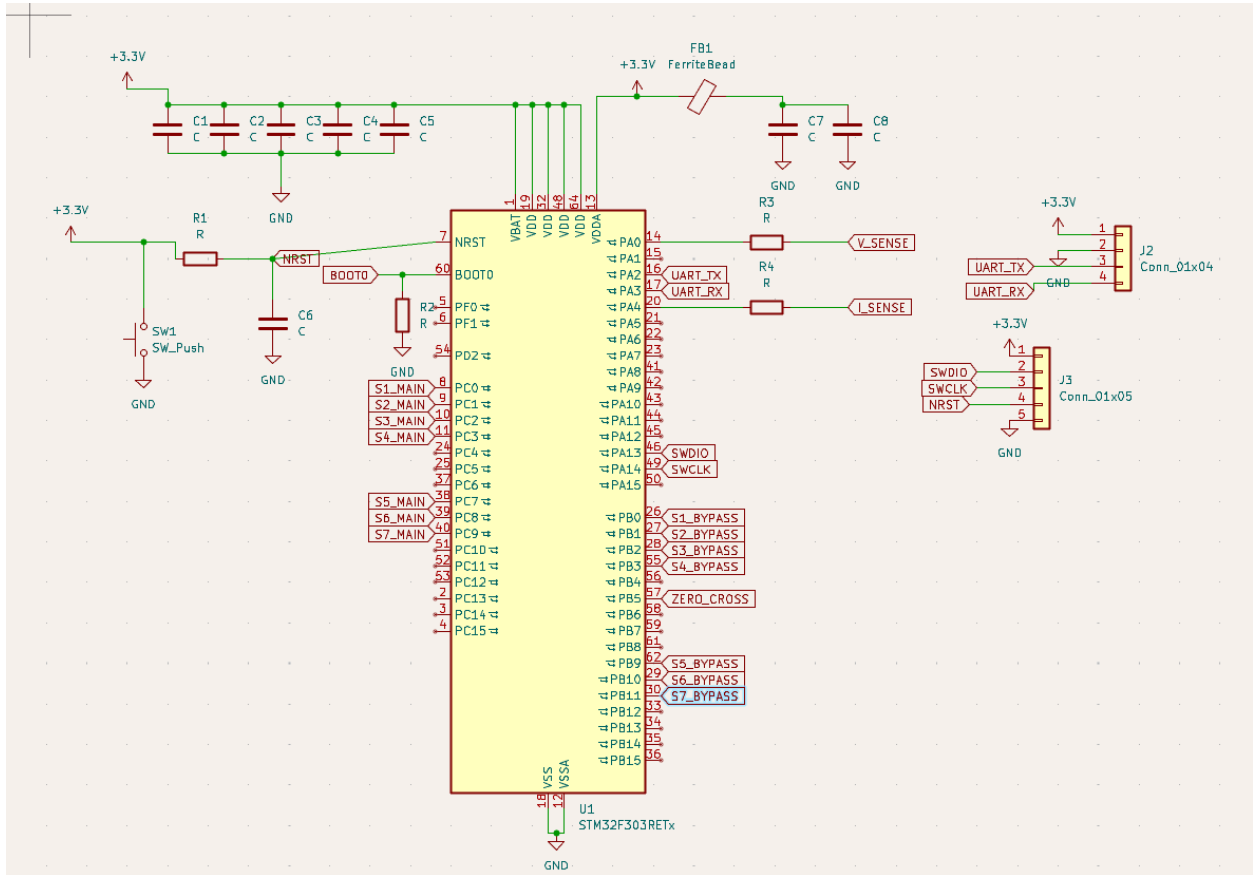


Figure 6: Schematic MCU Subsystem

MCU Subsystem Requirements and Verification:

Requirement:	Verification:
Synchronized Real-Time Sampling: The MCU shall sample the conditioned voltage and current signals at 5–10 kHz using hardware-timed ADC acquisition. Relative timing mismatch between the voltage and current channels shall not exceed 5 μ s.	Apply the same 60 Hz sinusoidal signal to both ADC inputs. Capture at least 10 complete cycles using the MCU data buffer and export the samples through UART. Calculate the measured sampling rate and relative phase between channels. Pass: sampling rate is within 5–10 kHz and equivalent channel timing mismatch is $\leq 5 \mu$ s.
Accurate Power Computation: The MCU shall calculate V_{rms} , I_{rms} , P , S , Q , and PF within $\pm 2\%$ of a reference measurement	Connect the MCU to the sensing subsystem and variable RL load. Record MCU and reference-meter measurements at several load settings spanning approximately PF = 0.1–0.9.

device.	Calculate percent error for each quantity. Pass: each calculated value is within $\pm 2\%$ of the reference.
Zero-Cross Detection: The MCU shall detect every 60 Hz AC zero crossing without missed or additional events and timestamp the crossing within $\pm 100 \mu\text{s}$ of the measured voltage zero crossing.	Display the AC voltage and zero-cross signal simultaneously on an oscilloscope. Capture at least 100 zero crossings and measure the timing difference. Pass: no missed/extra events and every detected crossing is within $\pm 100 \mu\text{s}$
Threshold-Based Control: The MCU shall evaluate compensation approximately every 10 s and prevent unnecessary changes for PF variations smaller than approximately 0.04.	Hold the system at a steady load, then create PF changes below and above 0.04 while logging PF and switching commands. Pass: changes smaller than 0.04 do not unnecessarily reconfigure the bank, while an out-of-range change greater than 0.04 causes a new compensation decision at the next evaluation.
Capacitor Stage Selection: The MCU shall calculate required compensation and select the combination of the seven measured capacitor stages that minimizes the difference between required and available capacitance.	Store measured stage capacitances in firmware. For at least 20 test values of required capacitance, independently calculate all 128 possible stage combinations and compare the expected best combination with the MCU output. Pass: the MCU selects the minimum-error combination for every test case.
Switching Sequence: The MCU shall provide independent main and bypass commands for all seven capacitor stages. The bypass command shall occur $33.3 \text{ ms} \pm 1 \text{ ms}$ after the corresponding main command.	Monitor the main and bypass GPIO signals with an oscilloscope while commanding several stages. Measure the delay between edges. Repeat for all stages. Pass: every bypass delay is between 32.3 and 34.3 ms and all outputs remain inactive during reset/startup.
Capacitor Reconnection Lockout: A stage that is disconnected shall not be commanded on again for at least 10 s.	Command a stage off and immediately request it on again through the control algorithm. Monitor the GPIO output and

	firmware log. Pass: the MCU prevents reactivation for at least 10 s.
Status Reporting: The MCU shall report V_{rms} , I_{rms} , P , S , Q , PF, and active capacitor stages through UART at least once per second during normal operation.	Connect a serial terminal and operate the system for at least 60 s while changing the load. Pass: all required values are reported at ≥ 1 Hz without missing or corrupted fields.

MCU Timing and Sampling Tolerance Analysis

Accurate power factor calculation depends on preserving the phase relationship between the voltage and current samples. As briefly mentioned earlier, A relative sampling delay Δt produces a phase error of

$$\Delta\phi = 2\pi f\Delta t.$$

At 60 Hz, limiting the relative voltage-current sampling mismatch to 5 μs gives

$$\Delta\phi = 2\pi(60 \text{ Hz})(5 \mu\text{s}) = 0.001885 \text{ rad} = 0.108^\circ.$$

The worst timing sensitivity occurs at the lowest designed load power factor of 0.1. The corresponding phase angle is

$$\phi = \cos^{-1}(0.1) = 84.26^\circ.$$

Including the worst-case 0.108° sampling error gives a maximum power-factor error of approximately 0.00188. Relative to $\text{PF} = 0.1$, this is approximately 1.88%, which remains below the MCU requirement of $\pm 2\%$. At $\text{PF} = 0.95$, the same timing error produces only approximately 0.00059 PF error, or 0.062%.

Therefore, maintaining relative voltage-current sampling mismatch below 5 μs is sufficient for the MCU timing contribution to remain within the $\pm 2\%$ power-factor accuracy requirement across the designed operating range. Hardware-triggered simultaneous ADC sampling and Direct Memory Access (DMA) will be used to minimize timing variation.

Switching Subsystem:

Design Overview:

The capacitive switching subsystem dynamically connects and disconnects capacitor stages in parallel with the load to provide reactive power compensation and improve the system power factor. It receives GPIO control signals from the microcontroller and uses the DC signals to turn on respective AC Capacitive banks. The bank contains seven binary-weighted stages (1, 2, 4, 8, 16, 32, and 64 μF), and each stage uses the switching path shown in Figure 7:

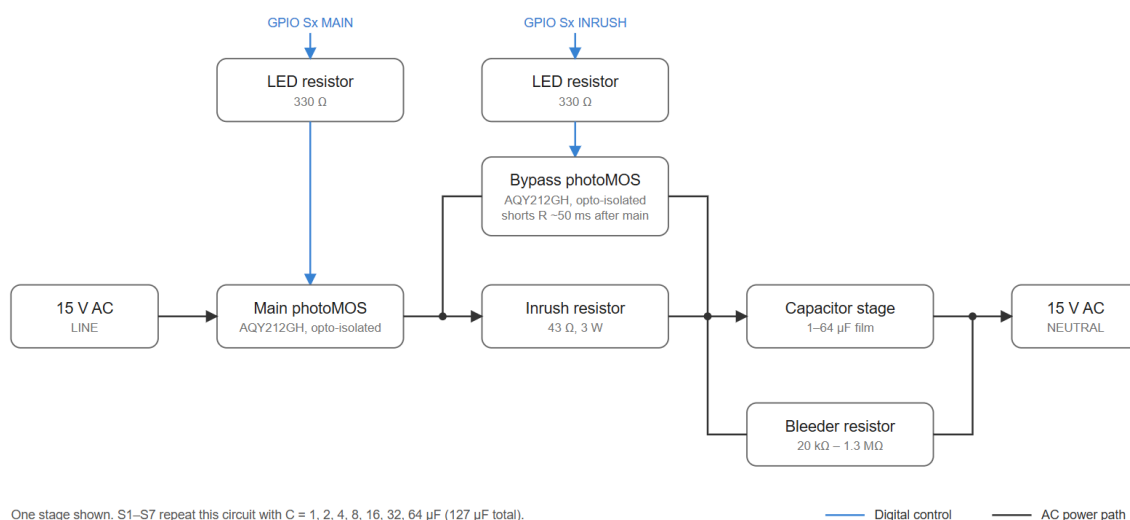


Figure 7: Switching System Block Diagram

Each stage is switched by a PhotoMOS relay. The relay's input is an LED that is optically coupled to a MOSFET output. This provides isolation between the low-voltage microcontroller and the AC circuitry. The GPIO pin drives the LED directly through a 330 Ω series resistor. When the LED is on, the output conducts in both directions with an on-resistance of 0.34 Ω typical and 0.7 Ω maximum, and it can open on command at any point in the AC cycle.

Two primary design considerations for this subsystem are switching synchronization and capacitor inrush current. The microcontroller times switching commands to the voltage zero-crossing. However, the specified PhotoMOS turn on time is 1.3 ms typical and 5.0 ms maximum. At 60 Hz this corresponds to 28° to 108° of the AC cycle, so a stage commanded at a zero-crossing may close as late as the voltage peak. Zero-cross timing alone therefore cannot guarantee low inrush, and a series inrush-limiting resistor is required on every stage. In the worst case, the relay closes at the voltage peak into a discharged capacitor, and the 47 Ω resistor limits the peak current to approximately 0.49 A. This is below the 0.5 A breadboard current limit and

well below the relay's 3.0 A peak load-current rating. Supporting calculations are provided below. A second PhotoMOS is connected across each inrush-limiting resistor as a bypass. Leaving $47\ \Omega$ in series during normal operation would reduce each stage's reactive power output and dissipate power in the resistor, so the bypass is required. The microcontroller closes the bypass two full AC cycles (33.3 ms) after commanding the main relay. This delay exceeds the approximately 18.8 ms needed for the main relay's worst-case turn-on time plus five time constants of the inrush transient in the largest stage, so the transient has decayed before the resistor is shorted. Each inrush resistor is rated 3 W so it can conduct continuously (about 2.7 W in S7) if a bypass relay fails to close.

A bleeder resistor is connected in parallel with each capacitor stage to provide a controlled discharge path after the stage is disconnected. The bleeder resistors are sized as large as possible to balance consuming real power when the stage is providing reactive power compensation and discharging the capacitor in a fast manner. Each stage must be fully discharged within 10 seconds which corresponds to the 10 second MCU delay, where fully discharged means five time constants (5τ), which leaves about 0.14 V of the 21.2 V peak. This ensures that no stage is reclosed while charged, and the controller does not reconnect a stage within 10 s of disconnecting it. For added margin, each bleeder is sized so that 5τ is at most 7 seconds, using the largest standard resistance that meets this limit. The selected values range from $1.3\ \text{M}\Omega$ (S1) to $20\ \text{k}\Omega$ (S7), giving 5τ between 6.4 s and 6.9 s. Keeping the resistance large keeps the losses negligible. The worst-case bleeder (S7, $20\ \text{k}\Omega$) dissipates 11.25 mW while connected, and each bleeder draws only about 0.2% of its capacitor's current, so its effect on power factor correction is minimal.

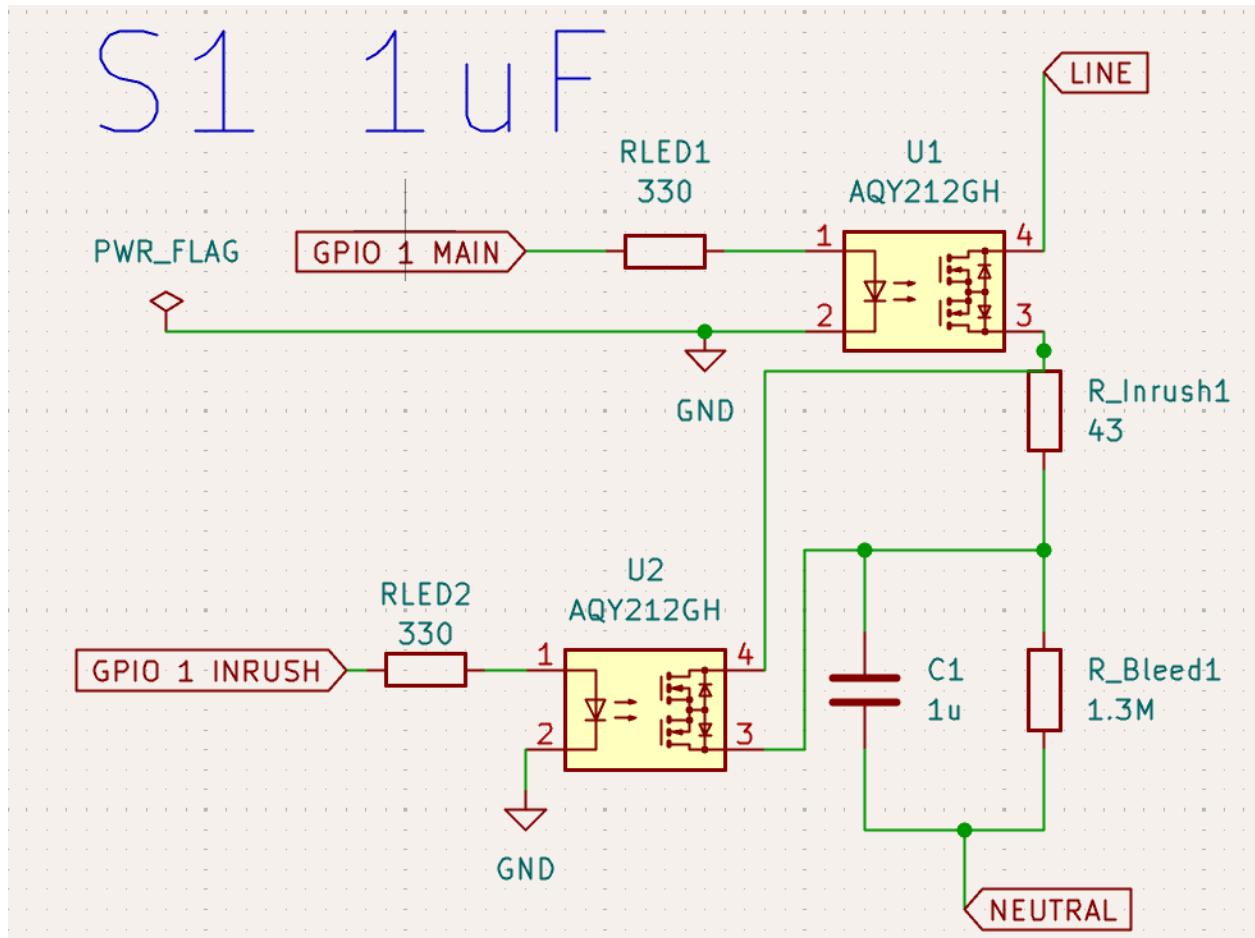


Figure 8: Schematic Switching Subsystem S1 Stage

The values for the 7 stages are as follows:

Stage	Capacitor Sizing (Micro Farads)	Inrush Resistor (Ohms)	Bleeder Resistor (Ohms)	LED Resistor (Ohms)
Stage 1	1	47	1300000	330
Stage 2	2	47	680000	330
Stage 3	4	47	330000	330
Stage 4	8	47	162000	330
Stage 5	16	47	82000	330
Stage 6	32	47	43000	330
Stage 7	64	47	20000	330

Figure 9: Values for design of Switching subsystem

Design calculations:

Load Sizing

The test load is a fixed inductor in series with a variable resistor. It is sized so that the power factor can be swept from 0.1 to 0.9 without exceeding the 0.5 A breadboard current limit.

Because the breadboard rating is a continuous (RMS) rating, the load is sized on RMS current; the corresponding peak current is 0.71 A. Maximum current occurs at the lowest power factor, where the load impedance is smallest:

$$|Z_{min}| = V_{rms} / I_{max} = 15 V / 0.5 A = 30 \Omega \quad (18)$$

Where:

$|Z_{min}|$ = minimum load impedance magnitude (Ω)

V_{rms} = RMS line voltage (V)

I_{max} = maximum RMS load current (A)

The minimum load resistance sets the lowest power factor:

$$R_{min} = PF_{min} \times |Z_{min}| = (0.1)(30 \Omega) = 3 \Omega \quad (19)$$

Where:

R_{min} = minimum load resistance (Ω)

PF_{min} = minimum load power factor (dimensionless)

$|Z_{min}|$ = minimum load impedance magnitude (Ω)

The inductive reactance required at the lowest power factor is:

$$X_L = |Z_{min}| \times \sin(\cos^{-1}(PF_{min})) = (30 \Omega)(0.995) = 29.85 \Omega \quad (20)$$

Where:

X_L = load inductive reactance (Ω)

$|Z_{min}|$ = minimum load impedance magnitude (Ω)

PF_{min} = minimum load power factor

The corresponding load inductance is:

$$L = X_L / (2\pi f) = 29.85 \Omega / 377 \text{ rad/s} = 79.18 \text{ mH} \quad (21)$$

Where:

L = load inductance (H)

X_L = load inductive reactance (Ω)

f = line frequency (Hz)

With the inductance fixed, the resistance required for the upper power factor limit is:

$$R_{max} = X_L / \tan(\cos^{-1}(PF_{max})) = 29.85 \Omega / 0.484 = 61.6 \Omega \quad (22)$$

Where:

R_{max} = maximum load resistance (Ω)

X_L = load inductive reactance (Ω)

PF_{max} = maximum load power factor (dimensionless)

A potentiometer range of 3 Ω to 61 Ω is selected, which gives a power factor of $0.898 \approx 0.9$ at the upper limit. At this setting, the load current is:

$$I_{load} = V_{rms} / \sqrt{(R_{max}^2 + X_L^2)} = 15 \text{ V} / 67.9 \Omega = 0.221 \text{ A} \quad (23)$$

Where:

I_{load} = RMS load current at R_{max} (A)

V_{rms} = RMS line voltage (V)

R_{max} = maximum load resistance (Ω)

X_L = load inductive reactance (Ω)

Capacitor Bank Sizing

The most compensation is required at $PF = 0.1$. RMS values are used throughout this section because real and reactive power are defined in terms of RMS quantities. The real power drawn by the load at this operating point is:

$$P = I_{max}^2 \times R_{min} = (0.5 \text{ A})^2(3 \Omega) = 0.75 \text{ W} \quad (24)$$

Where:

P = load real power (W)

I_{max} = maximum RMS load current (A)

R_{min} = minimum load resistance (Ω)

The reactive power drawn by the load is:

$$Q_L = I_{max}^2 \times X_L = (0.5 \text{ A})^2(29.85 \Omega) = 7.46 \text{ VAR} \quad (25)$$

Where:

Q_L = load reactive power (VAR)

I_{max} = maximum RMS load current (A)

X_L = load inductive reactance (Ω)

The reactive power the bank must supply to reach the 0.95 target is:

$$Q_C = Q_L - P \times \tan(\cos^{-1}(PF_{target})) = 7.46 - (0.75)(0.329) = 7.21 \text{ VAR} \quad (26)$$

Where:

Q_C = required capacitive reactive power (VAR)

Q_L = load reactive power (VAR)

P = load real power (W)

PF_{target} = target corrected power factor (dimensionless)

The capacitance required to supply this reactive power is:

$$C_{req} = Q_C / (\omega V_{rms}^2) = 7.21 / ((377 \text{ rad/s})(15 \text{ V})^2) = 85.0 \mu\text{F} \quad (27)$$

Where:

C_{req} = required compensation capacitance (F)

Q_C = required capacitive reactive power (VAR)

ω = angular frequency, $2\pi f$ (rad/s)

V_{rms} = RMS line voltage (V)

A bank of n binary-weighted stages with a smallest stage C_{LSB} has a maximum capacitance of $C_{LSB}(2^n - 1)$. The number of stages required is therefore:

$$n \geq \log_2(C_{req} / C_{LSB} + 1) = \log_2(85.0 + 1) = 6.43 \quad (28)$$

Where:

n = number of binary-weighted stages

C_{req} = required compensation capacitance (F)

C_{LSB} = smallest stage capacitance (F)

Seven stages are required. Six stages provide only 63 μF , while seven provide 127 μF , about 50% margin over the worst case. The smallest stage must be finer than the width of the 0.93–0.97 window, which is narrowest at PF = 0.1:

$$\Delta C = P \times [\tan(\cos^{-1}(0.93)) - \tan(\cos^{-1}(0.97))] / (\omega V_{rms}^2) = 1.28 \mu\text{F} \quad (29)$$

Where:

ΔC = capacitance width of the target PF window (F)

P = load real power (W)

ω = angular frequency, $2\pi f$ (rad/s)

V_{rms} = RMS line voltage (V)

A 1 μF smallest stage satisfies $C_{LSB} < \Delta C$, giving the bank stages of 1, 2, 4, 8, 16, 32, and 64 μF .

Bleeder Resistor Sizing

When a stage is disconnected, it may hold up to the peak line voltage of 21.2 V. Its bleeder resistor then discharges it exponentially:

$$v_C(t) = V_{peak} \times e^{(-t/\tau)} \quad (30)$$

Where:

$v_C(t)$ = stage capacitor voltage after disconnection (V)

V_{peak} = peak line voltage (V)

t = time after disconnection (s)

τ = discharge time constant (s)

The discharge time constant is set by the bleeder resistance and the stage capacitance:

$$\tau = R_{bleed} \times C_{stage} \quad (31)$$

Where:

τ = discharge time constant (s)

R_{bleed} = bleeder resistance (Ω)

C_{stage} = stage capacitance (F)

A stage is considered fully discharged after five time constants, when the remaining voltage is:

$$v_C(5\tau) = V_{peak} \times e^{-5} \approx 0.0067 \times V_{peak} \quad (32)$$

Where:

$v_C(5\tau)$ = stage capacitor voltage after five time constants (V)

V_{peak} = peak line voltage (V)

To guarantee full discharge within a target time t_d :

$$5\tau \leq t_d \quad (33)$$

Where:

τ = discharge time constant (s)

t_d = discharge time target (s)

Substituting (20) into (22) gives the maximum bleeder resistance:

$$R_{bleed} \leq t_d / (5C_{stage}) \quad (34)$$

Where:

R_{bleed} = bleeder resistance (Ω)

t_d = discharge time target (s)

C_{stage} = stage capacitance (F)

While the stage is connected, the bleeder dissipates power:

$$P_{bleed} = V_{rms}^2 / R_{bleed} \quad (35)$$

Where:

P_{bleed} = bleeder power dissipation (W)

V_{rms} = RMS line voltage (V)

R_{bleed} = bleeder resistance (Ω)

The bleeder also draws a fraction of the stage current:

$$I_{bleed} / I_{stage} = X_C / R_{bleed} = 1 / (\omega R_{bleed} C_{stage}) \quad (36)$$

Where:

I_{bleed} = bleeder current (A)

I_{stage} = stage capacitor current (A)

X_C = stage capacitive reactance (Ω)

R_{bleed} = bleeder resistance (Ω)

ω = angular frequency, $2\pi f$ (rad/s)

C_{stage} = stage capacitance (F)

A large R_{bleed} minimizes both quantities in (24) and (25), while (23) sets its upper limit. A target of $t_d = 7$ s is used to give margin under the 10 s requirement. Each stage uses the largest standard resistance that satisfies (23), as listed in Table X.

Switching Subsystem Requirements:

Requirement:	Verification:
Safe Dynamic Capacitor Switching: The subsystem shall connect each capacitor stage to the energized 15 V RMS line through an inrush-limiting resistor so that the peak stage current at main relay closure does not exceed 0.5 A for any closing angle, including closure at the 21.2 V voltage peak, with the stage initially discharged to 0.2 V or less.	Equipment: 15 V AC source, oscilloscope with current probe, DC Supply. 1. Connect the AC source to LINE. Put CH1 on LINE voltage and CH2 (current probe) on the LINE lead. 2. Set the scope to single trigger on CH2. With the photomos off, pulse GPIO_S7_MAIN to 3.3 V at a random time. 3. Record the peak current and the closing angle. Take 3 trails 4. Repeat for S1-6. Pass: all peaks are 0.5 A or less.
Power Factor Correction Capability: The capacitor bank shall provide at least 85 μF of total switchable capacitance, the compensation required to correct the worst-case load (0.5 A RMS at PF 0.1) to the 0.95 target. Capacitance shall be selectable in increments of no more than 1 μF, so that at least one stage combination places the corrected power factor within the 0.93–0.97 window for loads from PF 0.1 to 0.9.	Equipment: 15 V AC source, RL load, bench DC supply (3.3 V), reference power meter. 1. Connect the AC source, RL load, and board, with the power meter at the source. 2. Set the pot to 3 Ω (PF 0.1). Compute the required capacitance, then set the matching stage combination by applying 3.3 V to the corresponding GPIO_Sx_MAIN and GPIO_Sx_INRUSH pins. 3. Record the corrected PF. 4. Repeat at load settings for PF 0.3, 0.5, 0.7, and 0.9. Pass: the corrected PF is between 0.93 and 0.97 at every load setting.

Electrical Isolation: The low-voltage control side (GPIO) shall be isolated from the AC side (LINE/NEUTRAL), with a resistance greater than 20 MΩ between any control-side pin and either AC terminal.	Equipment: Multimeter. 1. With the board unpowered, measure the resistance from the GPIO header's GND pin to the LINE screw terminal, and to the NEUTRAL screw terminal. 2. Repeat from each GPIO header pin to the LINE and NEUTRAL screw terminals. Pass: every reading is greater than 20 MΩ
Capacitor Discharge: After a stage is disconnected at any point in the AC cycle, its voltage shall fall to 0.2 V or less (1% of the 21.2 V peak) within 10 s. The bleeder resistors are designed to discharge each stage in five time constants within 7 s to provide margin.	Equipment: 15 V AC source, bench DC supply (3.3 V), oscilloscope 1. Connect the AC source to the LINE and NEUTRAL terminals, and probe across the stage capacitor. 2. Turn the stage on by applying 3.3 V to its main and bypass GPIO pins. 3. Set the scope to single capture at 2 s/div, then remove the 3.3 V from both pins. 4. Record the capacitor voltage at disconnection and the time it takes to reach 0.2 V. 5. Repeat per stage, including at least one disconnection with the capacitor at 18 V or more. Pass: every discharge time is 10 s or less.
Control Interface: Each main and bypass relay shall turn on for a GPIO input of 3.0–3.6 V DCt, and shall remain off for inputs of 0.8 V or less. A stage shall begin conducting within 8.3 ms (one half-cycle) of a rising control edge and stop conducting within 1 ms of a falling edge.	Equipment: bench DC supply, multimeter, 15 V AC source, oscilloscope. 1. With AC off, apply 3.0 V to a GPIO pin and measure the resistance across that relay's output pins. 2. Repeat at 3.6 V and at 0.8 V. 3. Repeat steps 1–2 for all 14 GPIO pins. 4. With AC on, drive one main GPIO pin with a 1 Hz, 0–3.3 V square wave. Put

	CH1 on the GPIO pin and CH2 across the stage capacitor. 5. Over 20 cycles, measure the delay from each rising edge until the capacitor voltage begins following the line, and from each falling edge until it stops following the line. Pass: • At 3.0–3.6 V, the relay output reads less than 1 Ω. • At 0.8 V, the main relay reads more than 1 MΩ, and the bypass reads about 47 Ω because its inrush resistor is in parallel. • Turn-on delay is 8.3 ms or less, and turn-off delay is 1 ms or less.
Bypass Closure Current: The peak stage current when the bypass relay shorts the inrush-limiting resistor shall not exceed 3.0 A.	Equipment: 15 V AC source, bench DC supply (3.3 V), oscilloscope with current probe. 1. Connect the AC source to the LINE and NEUTRAL terminals, and put the current probe on the LINE lead. 2. Apply 3.3 V to S7's main GPIO pin. 3. Set the scope to single trigger at 0.6 A, then apply 3.3 V to S7's bypass GPIO pin. 4. Record the peak current at bypass closure. 5. Turn the stage off, wait 10 s, and repeat 20 times. 6. Repeat for S6 and S5. Pass: every peak current is 3.0 A or less.

Fail-Safe Off State: With all control inputs low or floating, or with the microcontroller unpowered or held in reset, every stage shall draw less than 1 mA RMS from the line.	Equipment: 15 V AC source, multimeter, bench DC supply. 1. Connect the AC source to the LINE and NEUTRAL terminals with the multimeter in series with the LINE lead. 2. With the GPIO header unplugged (inputs floating), record the current. Pass: every reading is less than 1 mA RMS.
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Tolerance Analysis - Switching Subsystem:

The most critical function of the switching subsystem is placing the corrected power factor within the 0.93–0.97 target window (High-Level Requirement 3). The most demanding operating point is the worst-case load at PF 0.1. There, the real power is smallest, so the window of acceptable capacitance is narrowest. This analysis shows that, at this operating point, standard film capacitor tolerances are wide enough to push the corrected power factor outside the window. It then presents the mitigation used in this design.

The capacitance that produces a given corrected power factor is found by rearranging (15) and (16):

$$C(PF) = [Q_L - P \times \tan(\cos^{-1}(PF))] / (\omega V_{rms}^2) \quad (37)$$

Where:

$C(PF)$ = capacitance that produces the corrected power factor PF (F)

Q_L = load reactive power, 7.462 VAR at PF 0.1 (VAR)

P = load real power, 0.750 W at PF 0.1 (W)

PF = corrected power factor (dimensionless)

ω = angular frequency, $2\pi f$ (rad/s)

V_{rms} = RMS line voltage (V)

Evaluating (26) at the window limits gives the range of acceptable capacitance:

$$C_{low} = C(0.93) = (7.462 - 0.750 \times 0.3952) / ((377 \text{ rad/s})(15 \text{ V})^2) = 84.48 \mu\text{F} \quad (38)$$

Where:

C_{low} = capacitance at the lower edge of the PF window (F)

$$C_{high} = C(0.97) = (7.462 - 0.750 \times 0.2506) / ((377 \text{ rad/s})(15 \text{ V})^2) = 85.76 \mu\text{F} \quad (39)$$

Where:

C_{high} = capacitance at the upper edge of the PF window (F)

The acceptable range is therefore only 1.28 μF wide, consistent with (18). The controller corrects this load with the combination S7 + S5 + S3 + S1. Using the built (nominal) stage values:

$$C_{sel} = C_{S7} + C_{S5} + C_{S3} + C_{S1} = 64.2 + 16.0 + 3.98 + 1.0 = 85.18 \mu\text{F} \quad (40)$$

Where:

C_{sel} = nominal capacitance of the selected stage combination (F)

$C_{S7}, C_{S5}, C_{S3}, C_{S1}$ = nominal capacitance of each selected stage (F)

At its nominal value, this combination gives a corrected PF of 0.954, inside the window. However, each film capacitor has a manufacturing tolerance t . In the worst case, all selected capacitors deviate in the same direction:

$$C_{actual} = C_{sel} \times (1 \pm t) \quad (41)$$

Where:

C_{actual} = actual capacitance of the selected combination (F)

t = capacitor tolerance (dimensionless)

The corrected power factor for any actual capacitance is:

$$PF = P / \sqrt{(P^2 + (Q_L - \omega C_{actual} V_{rms})^2)} \quad (42)$$

Where:

PF = corrected power factor (dimensionless)

P = load real power (W)

Q_L = load reactive power (VAR)

ω = angular frequency, $2\pi f$ (rad/s)

C_{actual} = actual capacitance of the selected combination (F)

V_{rms} = RMS line voltage (V)

The largest tolerance the selected combination can have and still remain within the window is:

$$t_max = (C_high - C_low) / (2C_sel) = 1.28 \mu F / (2 \times 85.18 \mu F) = 0.75\% \quad (43)$$

Where:

t_max = maximum allowable capacitor tolerance

C_high, C_low = capacitance limits of the PF window (F)

C_sel = nominal capacitance of the selected combination (F)

Standard film capacitors have tolerances of $\pm 5\text{--}10\%$, which is 7–13 times wider than this limit. If the controller selects stages using nominal values, it cannot guarantee correction into the window at low power factors. Over-correction to a leading power factor is also possible. At the PF 0.9 end of the load range, only about 5.6 μF is needed and the window is about 5 μF wide, so tolerance there is not a concern.

In order to mitigate this instead of nominal values, each stage's actual capacitance is measured on the assembled board with a benchtop LCR meter before operation. The seven measured values are stored in the microcontroller firmware. The controller computes the true capacitance of all 128 stage combinations from these measurements and selects the combination closest to the required capacitance. This removes the capacitor manufacturing tolerance from the error budget.

Tolerance Analysis:

Sensing Subsystem - Bias Error:

An important tolerance that would lead to error is not having the correct bias voltage. If the intended bias of 1.65 V deviates by 50 mV, this represents a 5% offset relative to a ~1 V peak signal. This introduces a DC offset in the reconstructed waveform after sampling, which affects the real power calculation and by extension, the power factor calculation. To mitigate this, the system will calculate the average of sampled values in software and then remove the bias. This way, bias-related errors will be significantly reduced.

DC Power Supply Subsystem - Rectifier Ripple and Filtering:

One thing to look out for in the power supply is the ripple introduced by the AC-to-DC conversion stage, which must be reduced to avoid affecting the downstream regulation. For a 15 V_{RMS} input assuming a full-wave rectifier and a load current of 0.3 A, the ripple voltage is approximately 2.5 V with a 1000 microfarad capacitor. This level of ripple is too large for direct use, but it is reduced by the voltage regulation stage, which provides a stable 5 V output. This will then get regulated with an LDO providing a 3.3V rail. Increasing the bulk capacitance or using additional filtering further reduces ripple, which would allow for proper regulator operation.

MCU Timing and Sampling:

Accurate power factor calculations require synchronized voltage and current sampling. At a 5 kHz sampling rate, the sampling interval is 200 μ s. For a 60 Hz AC source, a 10 μ s timing mismatch introduces a phase error of approximately 0.216°, resulting in a power factor error of approximately 0.0012 at PF = 0.95. Hardware-timed sampling and direct memory access (DMA) will minimize timing errors. Synchronization will be verified using an oscilloscope, and power factor accuracy will be checked against a reference measurement device to meet the $\pm 2\%$ requirement.

Schedule

Week	Member	Task
Week 10/4	Ryan Irvin	Finalize and order PCB for switching subsystem

	Saadullah Ehsan	Finalize and order PCB for MCU subsystem
	Luke Kang	Finalize and order PCB for Power Supply and Sensing subsystems
Week of 10/11	Ryan Irvin	Model and demo one capacitor switching system for breadboard demo and verification
	Saadullah Ehsan	Breadboard and demo MCU synchronized voltage/current sampling and power factor calculation using two known AC input signals; verify calculated PF through UART output.
	Luke Kang	Model and demo sensing system using power generator input and 343 power supply PCB with multimeter
Week of 11/18	Ryan Irvin	Design and Manufacture enclosing for Capacitive system
	Saadullah Ehsan	Complete MCU firmware for RMS voltage/current, real power, apparent power, reactive power, and power factor calculations.
	Luke Kang	Test and design for inter-PCB connectivity as well as increasing accuracy levels of measurements
Week of 10/25	Ryan Irvin	Solder PCB of Switching Subsystem
	Saadullah Ehsan	Solder and bring up MCU PCB; verify power rails, SWD programming, UART, ADC inputs, and GPIO outputs.
	Luke Kang	Solder PCB for Power supply and sensing subsystems

Week of 11/1	Ryan Irvin	Troubleshoot PCB/Verify requirements specified in design document
	Saadullah Ehsan	Troubleshoot MCU PCB and verify MCU subsystem requirements specified in the design document.
	Luke Kang	Troubleshoot PCB/Verify requirements specified in design document
Week of 11/8	Ryan Irvin	Prepare for mock demo and organize data for Requirements and verification
	Saadullah Ehsan	Prepare for mock demo and organize data for Requirements and verification
	Luke Kang	Prepare for mock demo and organize data for Requirements and verification
Week of 11/15	Ryan Irvin	Final Presentation and demo preparation
	Saadullah Ehsan	Final Presentation and demo preparation
	Luke Kang	
Week of 11/22 (UIUC Fall Break)	Ryan Irvin	Fall Break
	Saadullah Ehsan	Fall Break
	Luke Kang	Fall Break
Week of 11/29	Ryan Irvin	Final Demo/Presentation preparation/ Final report writing
	Saadullah Ehsan	Final Demo/Presentation preparation/ Final report writing
	Luke Kang	Final Demo/Presentation preparation/ Final report writing

Cost Analysis:

Sensing Subsystem	
Labor (~6 hr/week)	\$15,000
PCB for subsystem and eshop/self-service parts	\$31.50
Current Transformer – SCT-013-005, 5 A : 1 V	~\$10.00
MCP6002T-I/SN rail-to-rail dual op-amp	\$0.41 (DigiKey)
100 k Ω $\pm$ 1% voltage-divider resistor	\$0.12 (DigiKey)
10 k Ω $\pm$ 1% resistors x3–4	$\sim 4 \times \$0.10 = \0.40 (DigiKey)
1 μ F AC-coupling capacitors x2	$2 \times \$0.10 = \0.20 (DigiKey)
100 nF filter/decoupling capacitors x3	\$0.30
1 k Ω filter/protection resistors, 2 required	\$0.20
Connectors / test points for voltage sense, CT input, and ADC outputs	~\$2.00
DC Power Supply Subsystem	
Labor (~10 hr/week)	\$25,000
PCB for subsystem and eshop/self-service parts	\$31.50
Bridge Rectifier – B40C2300-1500B	\$1.20
Bulk Capacitor – 3300 μ F electrolytic	\$2.50
LM2596S-5 Buck Converter IC	\$2.00
Inductor – 40 μ H	\$1.50
Schottky Diode – 1N5822	\$0.80
Output Capacitor – 300 μ F electrolytic	\$1.50
Input/decoupling capacitors (0.1 μ F, etc.)	\$0.50
AMS1117-3.3 LDO Regulator	\$0.50

LDO input/output capacitors (10 μ F, etc.)	\$0.20
Connectors / test points / power routing	\$2.00
MCU Subsystem	
Microcontroller	STM32F303RET6, LQFP-64 = \$12.23
Digital decoupling capacitors x4	100 nF = \$0.40
MCU bulk capacitor	4.7 μ F = \$0.20
Analog supply capacitors	1 μ F and 10 nF = \$0.15 + \$0.10 = \$0.25
Ferrite bead	Filter between 3.3 V and 3.3 VA = \$0.15
ADC input resistors x2	100 Ω = \$0.10
BOOT0 pull-down	10 k Ω = \$0.10
NRST capacitor	100 nF = \$0.10
Reset pushbutton	Normally-open momentary switch = \$0.40
SWD header	5-pin = \$0.50
UART header	4-pin = \$0.40
MCU PCB	Custom PCB ~\$25–30
Switching Subsystem:	
Part/Expense	Cost
Labor (~16 per week)	\$40,000
PCB for subsystem and eshop/self service parts	\$31.50
Film Capacitors (B32529C0105K189 TDK Film Capacitors DigiKey)	14 x \$0.60 = \$8.4
AQY212GH Panasonic Industry Solid State Relays (SSR) DigiKey	\$35.17
RR03J43RTB TE Connectivity Passive Product Through Hole Resistors DigiKey	\$2.44

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Ethics, Safety, and Societal Impact

Ethics

The primary ethical consideration for this project is ensuring that the 15 V AC prototype operates safely and that its capabilities are represented accurately, both to instructors during evaluation and to any future audience of the design. This aligns with the IEEE Code of Ethics commitment "to hold paramount the safety, health, and welfare of the public" and "to be honest and realistic in stating claims or estimates based on available data" [2]. In practice, this means the design incorporates isolation, controlled capacitor switching, inrush limiting, and capacitor discharge protection to reduce risk to users, technicians and equipment, and the team will clearly distinguish between the demonstrated 15 V AC system and the broader concept of scaling the same architecture to higher-voltage, 480 V commercial applications. Any commercial implementation would require additional component ratings, protection, and regulatory compliance appropriate to the higher operating voltage, and the team will avoid overstating the prototype's readiness for such deployment.

Safety

Although the 15 V AC laboratory prototype falls outside the practical scope of most NEC installation requirements, the design is intended as a scalable proof of concept, so relevant requirements of NEC Article 460, which addresses capacitor installations used for applications such as power factor correction, are considered in the design [1].

- NEC 460.3 — Enclosing and Guarding: Capacitor terminals and other energized components must be protected from accidental contact. This design addresses that requirement through physical separation of the MCU and AC circuitry, optical isolation between the microcontroller and switching hardware, and protection of energized components during operation [1].
- NEC 460.6 — Discharge of Stored Energy: Capacitors must have a means of automatically discharging stored energy after being disconnected. This design uses a bleeder resistor across each capacitor stage to provide this discharge path [1].

Societal Impact

As electrical power demand continues to increase, improving the efficiency and utilization of existing electrical infrastructure becomes increasingly important. Power factor correction reduces unnecessary reactive current, which can lower system losses and free capacity in conductors, transformers, and other distribution equipment. An automated power-factor-correction system can therefore help facilities use electrical infrastructure more efficiently while supporting reliable

grid operation as demand grows, with broader economic and environmental benefits from reduced generation and transmission losses.

References

[1] National Fire Protection Association, *NFPA 70: National Electrical Code*, Quincy, MA: National Fire Protection Association, 2023.

[2] IEEE, "IEEE Code of Ethics." Available:
<https://www.ieee.org/about/corporate/governance/p7-8.html>