

ECE 445 SENIOR DESIGN PROJECT LAB

Design Document

Non-Shock Ultra-Wideband Virtual Boundary Pet Collar

Team No. 2

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1 Introduction

Physical gates can obstruct a doorway, while a virtual boundary could warn a pet without blocking people. This project explores a local, non-shock alternative using UWB ranging, vibration and sound. It is a prototype for demonstrating sensing and feedback; it does not establish animal-training effectiveness or replace a physical barrier.

Two wall-powered anchors define a finite boundary segment. A battery-powered collar measures its distance to that segment and requests vibration in the warning zone, then a tone closer to the line. The boundary works from either side. Compared with signal-strength thresholds, time-of-flight ranging gives us a geometric distance to test. Indoor reflections, body obstruction and antenna orientation remain important limitations.

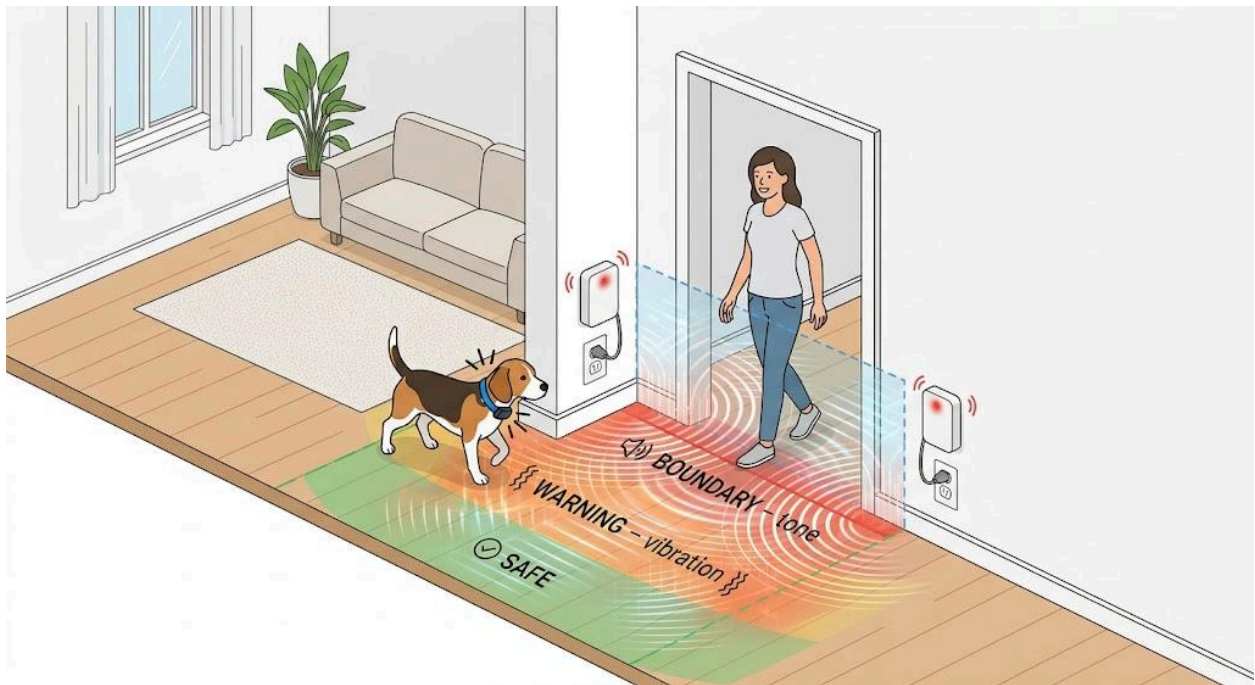


Figure 1. Intended use across a doorway. The illustration is conceptual, not to scale.

1.1 Scope and high-level requirements

The first demonstration uses two existing Makerfabs boards as anchors and one custom collar. A third owned board supports collar firmware development. More anchors, BLE setup and long battery life remain extensions. All performance values below are design targets until measured.

- Accuracy: The collar shall achieve boundary-distance $RMSE \leq 0.5$ m at each of 10 surveyed positions, including doorway and obstructed-path cases. Report bias, valid-update percentage and gaps alongside RMSE.

- Responsiveness: Under valid ranging conditions, the electrical motor or buzzer drive shall begin within 50 ms of a measured zone crossing. A stationary collar shall show no repeated safe/warning toggling during a 15-minute hysteresis test.
- Safe feedback: Invalid geometry, stale data or an anchor fault shall mute both outputs. Feedback shall also stop after 10 s of continuous non-safe dwell and remain off until the rearm condition is met.

A mass below 60 g is a packaging goal. Battery runtime is recorded if convenient, but 24-hour operation is not a prototype acceptance requirement.

2 System architecture and physical design

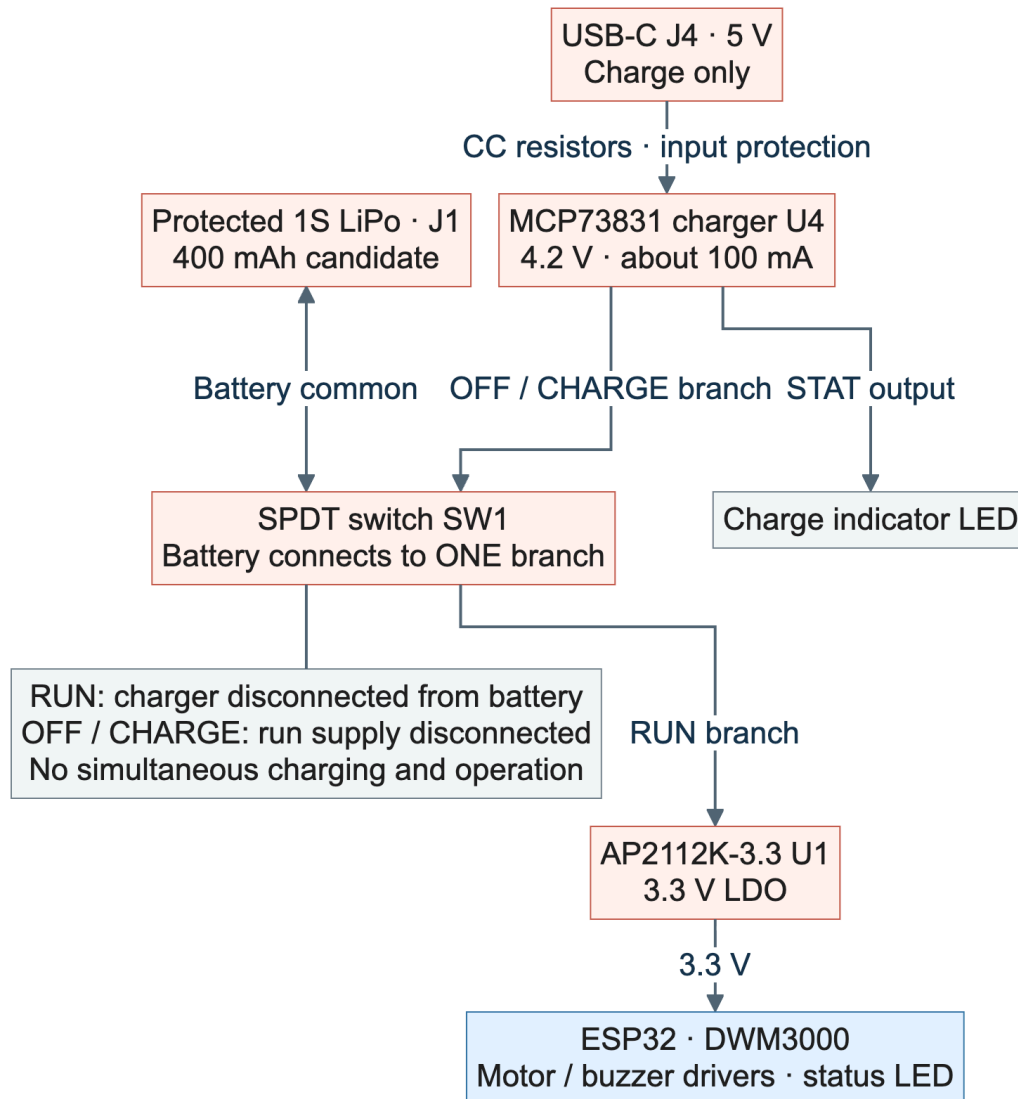


Figure 2a. Collar power and off-only charging. SW1 connects the battery to either the run supply or the charger.

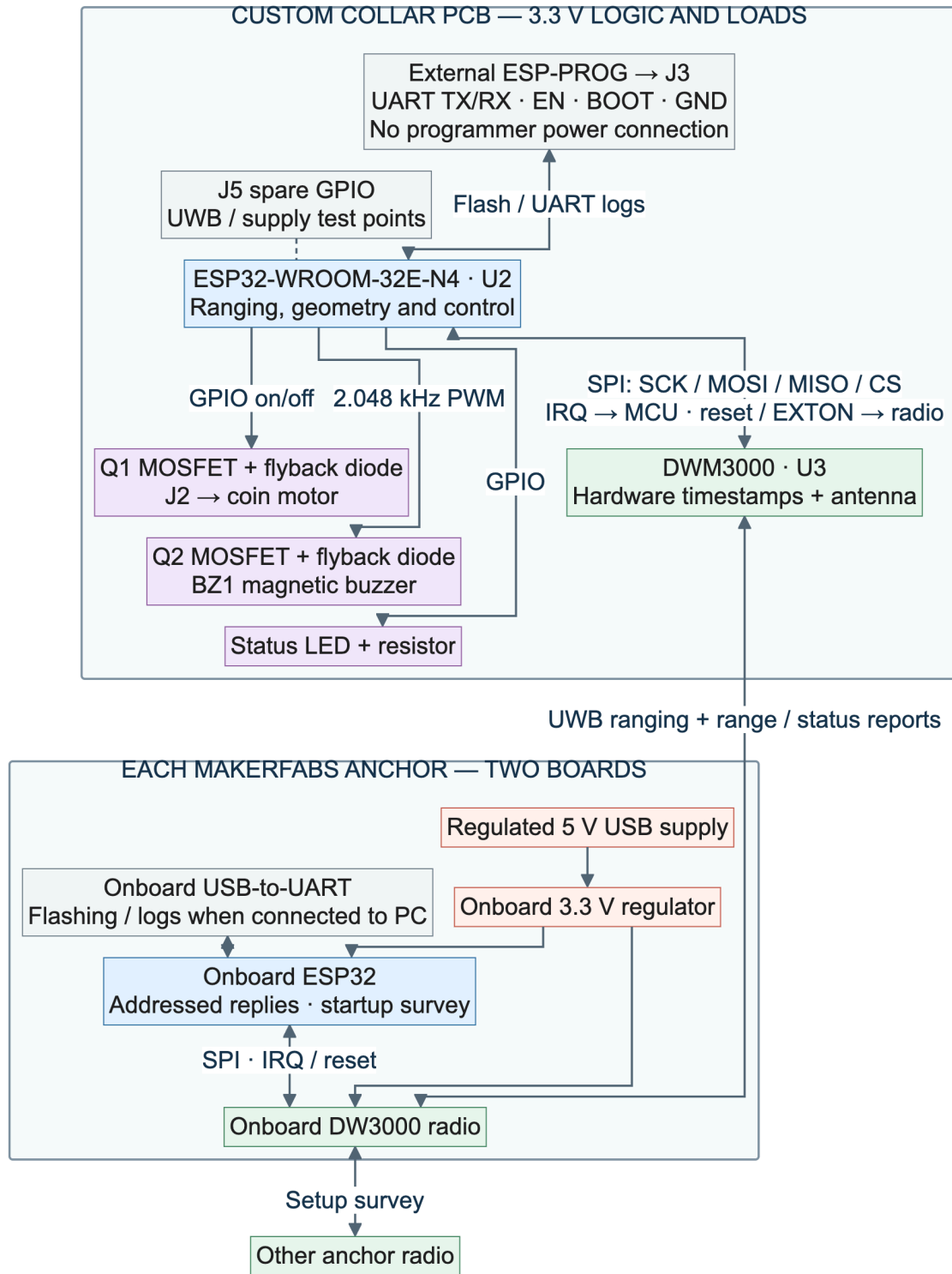


Figure 2b. Hardware interfaces for the collar and existing Makerfabs anchors. Collar logic and actuator loads use the 3.3 V run rail; all wired interfaces share ground.

Only the collar needs a custom PCB. It uses an ESP32-WROOM-32E-N4 and a DWM3000 radio module. The anchors retain their Makerfabs ESP32/DW3000 hardware and USB supplies. Separate firmware board profiles accommodate their different GPIO assignments. All collar logic interfaces use 3.3 V.

[1]–[3]

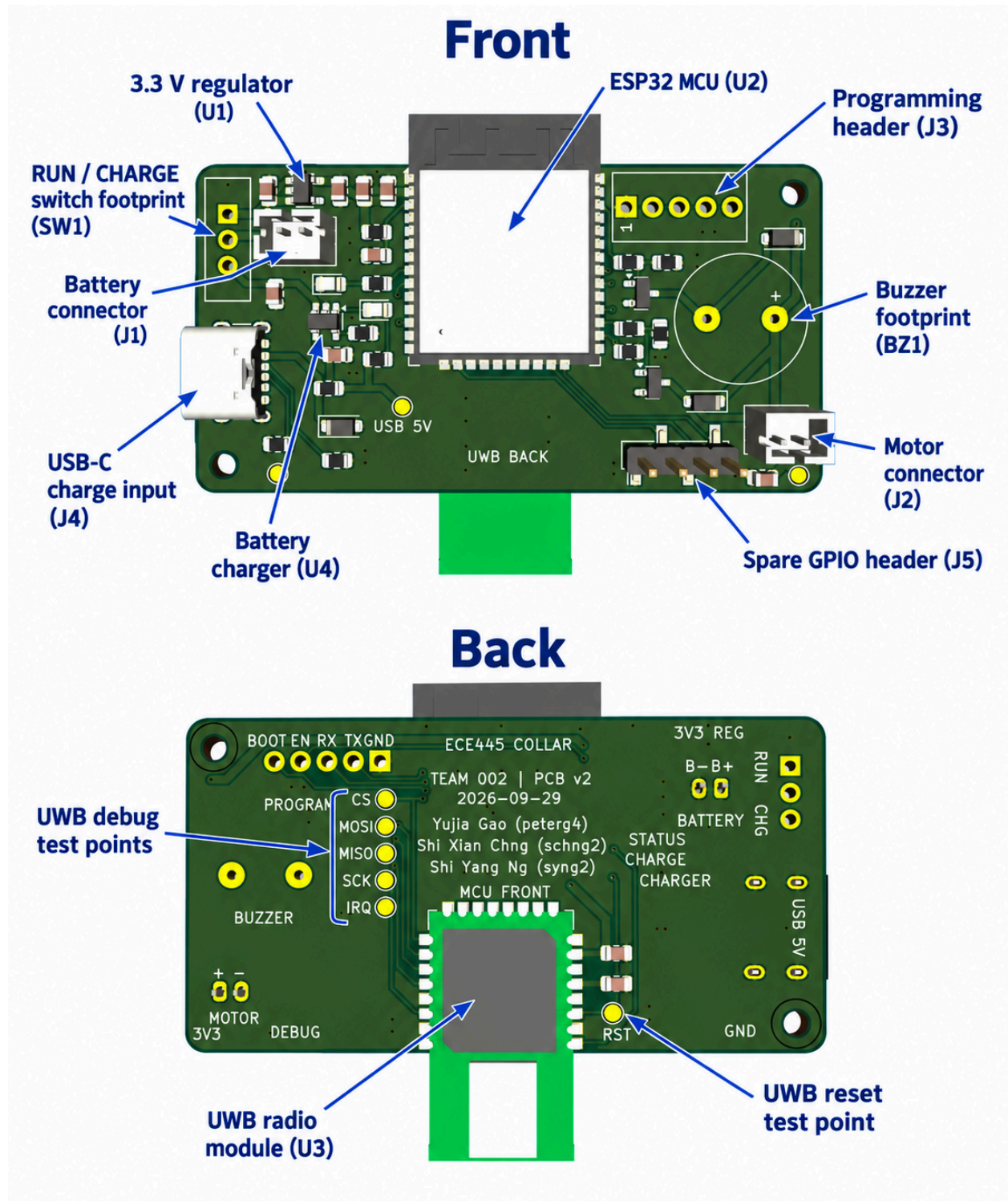
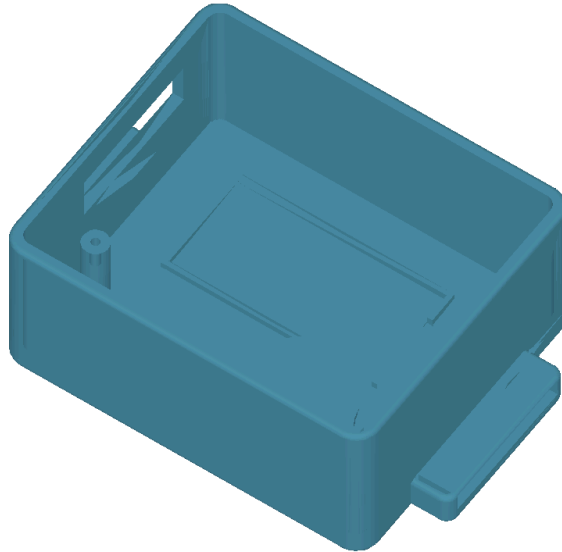


Figure 3. Collar PCB front (top) and back (bottom), annotated with the main components and connectors. Empty component locations are labeled as footprints.

Collar enclosure — v2 CAD model



Body: $66 \times 55.5 \times 31$ mm · 80 mm across strap ears

Figure 4. Enclosure base from the saved v2 CAD model. Nominal dimensions are shown; physical fit remains unverified.

The 60×32 mm PCB mounts on two M2 posts above the battery and coin motor. The PETG case body is $66 \times 55.5 \times 31$ mm, or 80 mm across the strap ears. Bond the motor to its seat so vibration reaches the case; retain the battery with thin foam adhesive without compressing the pouch. Keep both antenna regions clear of metal and wiring. The USB/switch window and lid buzzer openings follow the saved v2 CAD. A trial print must confirm fit, access and mass; the case is not weatherproof.

3 Subsystem design and verification

These are planned acceptance tests, not completed results. Use a bench supply, multimeter, oscilloscope or logic analyzer, surveyed positions and timestamped UART logs. Keep raw measurements and record the firmware revision, board profile, geometry and test conditions.

3.1 Anchor power, ranging and survey

Each anchor uses its existing onboard regulator and a regulated 5 V USB supply. Its ESP32 schedules DW3000 responses, surveys neighboring anchors and reports spacing and health to the collar. Reusing these boards avoids a second PCB design. Only the addressed node replies; node IDs and sequence numbers prevent delayed packets from being treated as current data. [1]

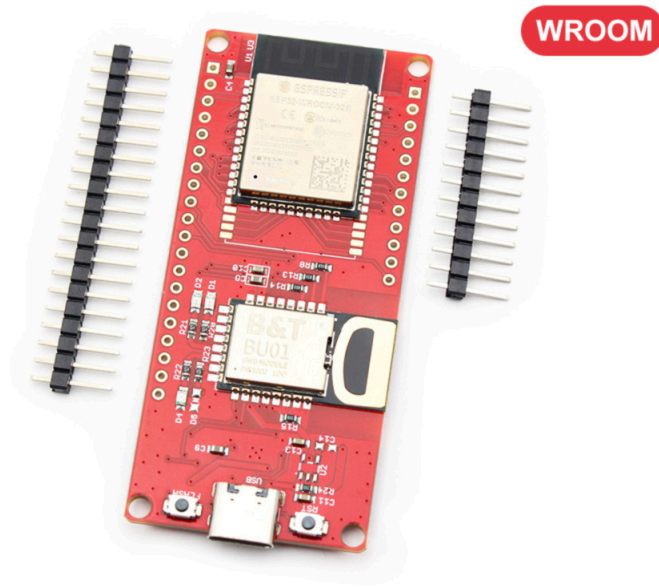


Figure 5. Makerfabs ESP32 UWB board, shown for illustration. The pictured radio differs from the DW3000 variant specified for this project.

Table 1. Anchor requirements and verification.

Requirement	Verification and pass condition
Addressed ranging and fault handling	Run 1,000 exchanges per anchor. Confirm only the addressed node replies. Inject wrong IDs, old sequence numbers and timeouts; none may become a valid range.
Usable spacing estimate	At the initial 2 m baseline, repeat the startup survey 10 times and compare each result with a tape measurement. Target absolute spacing error ≤ 0.10 m; retain the signed error for tolerance analysis.
Wall-powered operation	Run both anchors for 30 min through ranging and survey cycles. Pass with no brownout or reset and no unexplained loss of one anchor. Disconnect one anchor and confirm the collar reports the fault.

3.2 Collar processing, radio and programming

The ESP32 handles ranging, geometry, zone control and feedback. The DWM3000 supplies UWB hardware timestamps over SPI; IRQ signals events, and RST_N is driven low then released using

open-drain behavior. Retain local 100 nF and bulk capacitors: low average processing speed does not eliminate fast current transients. Use the module antenna keep-out regions in the PCB and enclosure. [2], [3]

J3 exposes GND, MCU TX, MCU RX, EN and BOOT for the external Olimex ESP-PROG. Normal power-up boots the application automatically. J4 USB-C is charge-only. J5 exposes GPIO13, GPIO15 and GPIO2 for debugging; keep GPIO2 low or floating during flashing. Do not connect a programmer power pin, and disconnect its signals before switching the collar off. [9]

Table 2. Collar and development-board GPIO assignments.

Signal	Custom collar v2 GPIO	Makerfabs development profile
SPI SCK / MISO / MOSI / CS	17 / 18 / 19 / 21	18 / 19 / 23 / 4
UWB IRQ / reset	4 / 27	34 / 27
Motor / buzzer / status LED	16 / 22 / 32	External test outputs configured separately
UART TX / RX; UWB EXTON	1 / 3; 33	Use board UART; profile-specific control

Table 3. Collar ranging and programming verification.

Requirement	Verification and pass condition
Correct programming and SPI access	Flash each board by role and ID. Read the expected radio device ID, print the selected pin map, then power-cycle 10 times. All boots must enter the application with outputs off.

Requirement	Verification and pass condition
Boundary RMSE ≤ 0.5 m	With anchors at (0,0) and (2,0) m, test collar positions (1,0), (1,0.2), (1,0.3), (1,1.0), (1,1.2), (1,1.5), (0.1,0.3), (1.9,-0.3), (-0.3,0.2) and (2.3,-0.2) m at equal antenna height. Collect $\geq 1,000$ updates at each position in LOS, then repeat with a closed wooden door blocking one path. Record door thickness, placement and radio orientation. Tabulate valid-sample RMSE and signed bias; every case must meet 0.5 m RMSE.
Usable updates, not just accurate survivors	At those positions, target $\geq 95\%$ valid updates and no gap over 100 ms. Report these separately; a low conditional RMSE cannot compensate for many rejected samples.
Complete ranging cycle ≤ 25 ms	Log cycle start, both anchor exchanges, final distance report and delivery to the controller for 1,000 cycles. The complete two-anchor cycle must meet 25 ms in the declared demonstration conditions.

For the planar demonstration, place the anchors and collar radio at the same height. With only two ranges, vertical separation is indistinguishable from horizontal distance away from the line. Equal-height performance does not establish accuracy for a pet moving freely in 3D.

3.3 Battery, supply and charging

The protected 1S LiPo connects through J1. SW1, an Adafruit 805 SPDT switch rated 500 mA DC, selects RUN or OFF/CHARGE. RUN feeds the AP2112K-3.3 LDO. OFF/CHARGE connects the battery to the MCP73831 charger and disconnects the run supply. Pack protection handles cell over-discharge/over-current; the charger controls charging. There is no separate DW01A/FS8205A circuit or battery-voltage ADC. Keep ESP32 brownout detection enabled. [4], [5], [7], [10]

The AP2112 is simpler to assemble than the former buck-boost supply, but cannot boost a depleted battery. We accept reduced usable capacity and recharge before demonstrations. A working load estimate is 80 mA for the ESP32 with Wi-Fi/BLE off, 100 mA for the active radio, 80 mA for the motor, 40 mA for the buzzer and 10 mA for other loads: about 310 mA if all are active. These are planning allowances,

not measured maxima. At 4.2 V and 310 mA, LDO dissipation is about $(4.2 - 3.3) \times 0.31 = 0.28$ W. Verify temperature, startup peaks and the switch rating during bring-up.

J4 is the USB4125-GF-A-0190: six SMT contacts plus four soldered shell stakes. Each CC pin has its own 5.1 k Ω pull-down. R19 (2.2 Ω) and D5 (SMF4L5.0A) condition the 5 V input. R15 = 10 k Ω sets nominal charging current near 100 mA; C13/C14 are 10 μ F nominal and must retain at least 4.7 μ F at working bias. Charging is intended for a protected 4.2 V, approximately 400 mAh pack; Adafruit 3898 remains the candidate. The charge LED being off does not by itself prove a full battery. [5]–[7]

Table 4. Power and charging verification.

Requirement	Verification and pass condition
Stable run rail and adequate current margin	Remove the battery and feed J1 with a current-limited bench supply, observing polarity. In RUN, sweep 3.7–4.2 V and load the 3.3 V rail from idle to 310 mA total. Probe TP2 (+3V3) against TP1 (GND) with a DMM and oscilloscope; repeat with actual ranging and output transitions. Pass: 3.3 V $\pm$ 5%, no resets, and peak current within component ratings. Record current peaks, rail extrema and LDO temperature; 310 mA is a planning load, not a measured maximum.
Off-only charging	With a partly discharged approved pack, verify charging only in OFF/CHARGE and zero collar actuation in that state. Test both USB-C plug orientations. RUN must disconnect the charger from the battery.
Correct charge behavior	Measure roughly 100 mA during constant-current charging (working acceptance band 85–115 mA), then verify voltage regulation near 4.2 V within the charger specification and current taper/termination. Stop if the pack heats, swells or exceeds its limits.

3.4 Feedback and mechanical assembly

A coin ERM motor on J2 provides vibration, Adafruit 1201 remains the candidate. BZ1 is a CEM-1203(42) magnetic transducer, driven at 2048 Hz with 50% PWM. It is not a piezo or a self-oscillating buzzer. Each output uses an AO3400A low-side MOSFET, a 330 Ω gate resistor, a 100 k Ω

gate pull-down and an SS14FL clamp diode. Pull-downs keep outputs off during reset. Both loads use the regulated 3.3 V rail. [8], [16]

Table 5. Feedback and assembly verification.

Requirement	Verification and pass condition
Controllable vibration and tone	Command each output on the bench. Confirm vibration by touch and an audible tone. Probe the buzzer MOSFET gate against TP1 (GND): require 2048 Hz $\pm 2\%$ and 50% ± 5 percentage points. Probe the motor gate for commanded on/off behavior. No steady-high buzzer command.
Default-off outputs	Observe both MOSFET gates across power-up, reset, flashing and controller faults. They must remain low until an approved feedback request arrives.
Physical fit and access	Trial-print the case and assemble the PCB, candidate pack and motor. Pass if both mounting holes align, nothing strains the connectors, the switch/USB port are accessible and antenna clearance is maintained. Record mass against the <60 g goal.

4 Firmware and control

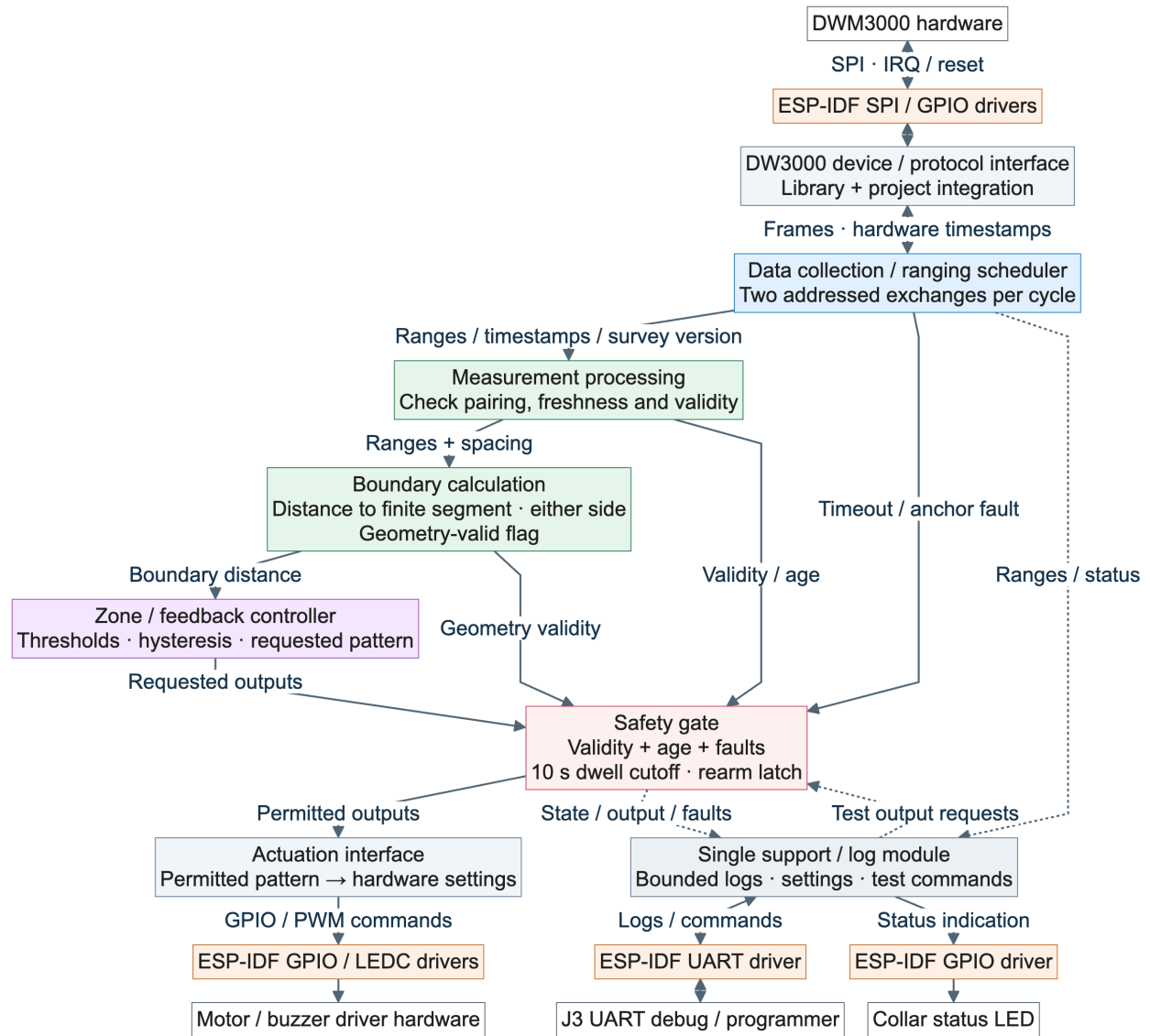


Figure 6a. Collar software architecture. ESP-IDF drivers are reused; all motor and buzzer requests pass through the safety gate. Dotted links carry diagnostic events and commands.

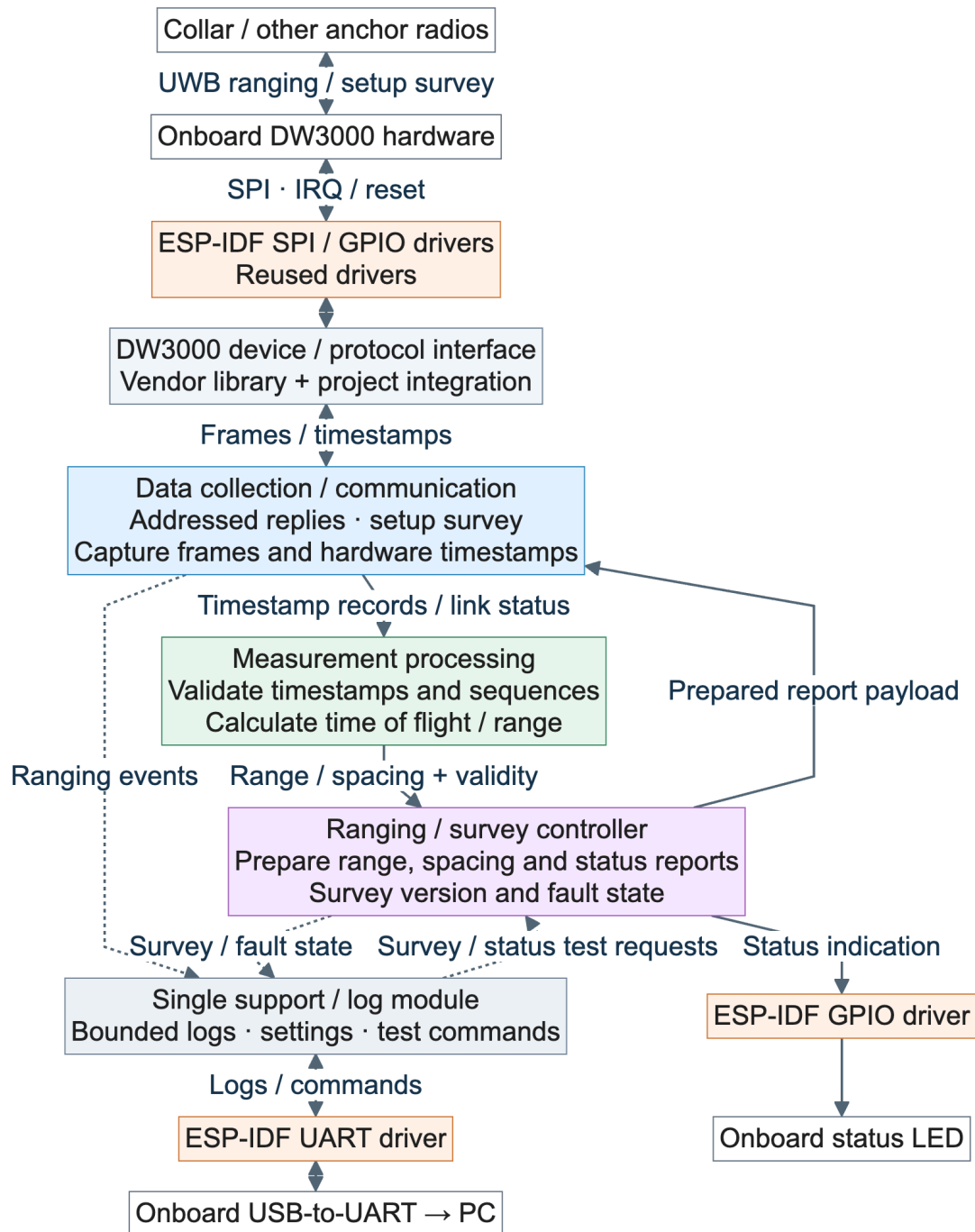


Figure 6b. Anchor software architecture, repeated on each Makerfabs board. One support/log module handles diagnostics; surveys establish spacing before operation.

4.1 Ranging protocol

Use double-sided two-way ranging (Figure 7). The collar sends a poll and final; the addressed anchor sends a response, calculates time of flight and reports range. The final carries the collar's poll-TX,

response-RX and final-TX hardware timestamps; the anchor already has the other three timestamps. For round-trip intervals R_1 , R_2 and reply delays D_1 , D_2 , time of flight is $(R_1R_2 - D_1D_2)/(R_1 + R_2 + D_1 + D_2)$. Subtract timestamps with wrap handling and convert intervals to common units before applying the formula. [3]

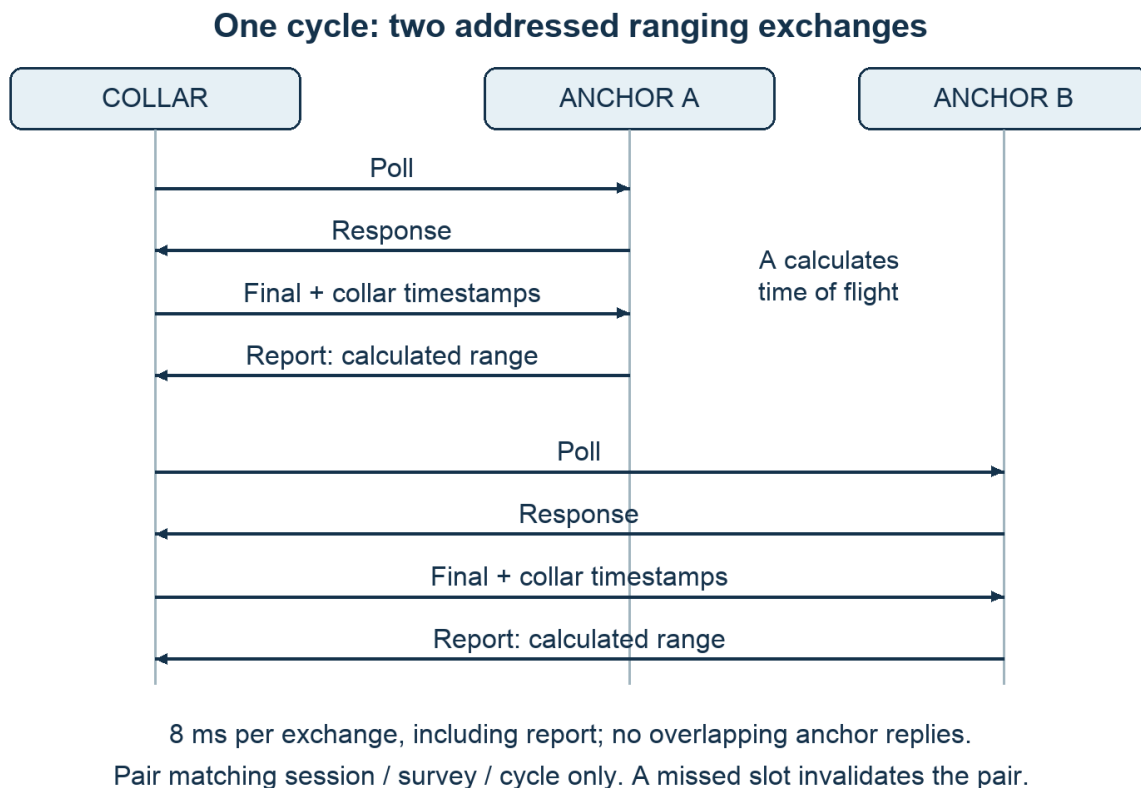


Figure 7. Addressed two-anchor ranging. Each report belongs to the current cycle; the receiving anchor calculates range.

Start a new cycle every 25 ms. Budget 8 ms per anchor, including its report, 3 ms for validation/geometry and 1 ms for safety/output; 5 ms remains for guard time. A crossing just after sampling waits at most one 25 ms period, then a 20 ms active cycle: a 45 ms scheduling budget leaves 5 ms against the 50 ms target. This assumes the next valid pair detects the crossing; noise can delay that detection, so the physical crossing test remains required. No retries may overrun a slot. Survey runs before feedback is enabled and pauses normal ranging.

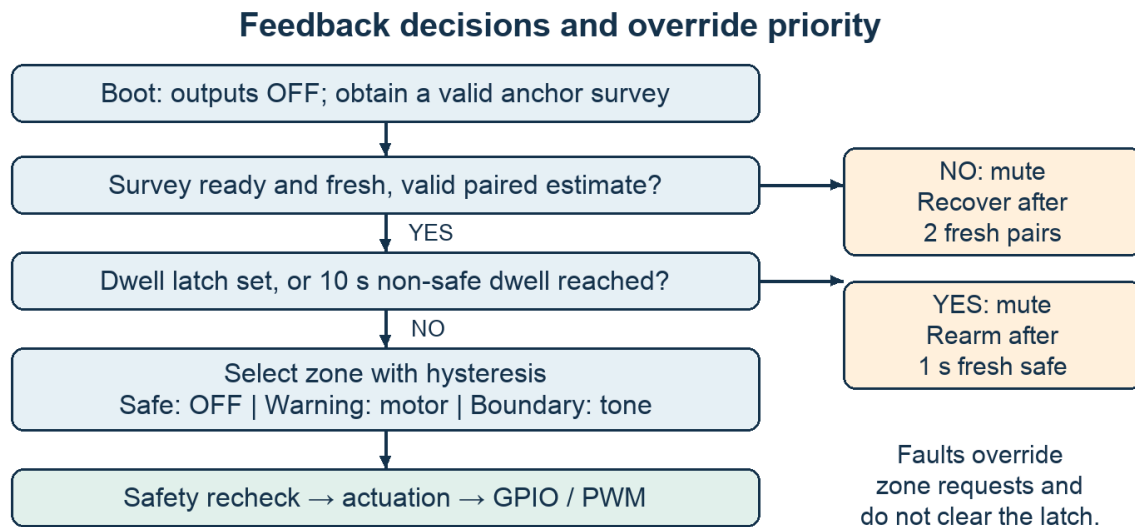
Use the application fields in Table 6 with vendor MAC framing and CRC. Pair only A and B reports from the same session, survey version and cycle; require collar-local measurement times within 16 ms. A missing/late report invalidates the pair, without combining it with an older cycle. Keep range, timestamp, age, validity and correction status in the internal record. Hardware timestamp units are converted in

measurement processing; controller distances use metres. Start without temporal filtering so no hidden smoothing delay enters the timing budget.

Table 6. Planned application messages; vendor framing and CRC retained.

Message / scope	Fields and units	Receiver action
All messages	Version, type, source ID, destination ID: uint8 each; session: uint32; cycle and survey version: uint16 each. Multi-byte fields are little-endian.	Check CRC, addressed ID, session, cycle, survey version and expected message type. Reject late or duplicate frames.
Poll / response	Common fields only; radio records TX/RX timestamps.	Only the addressed anchor responds. Collar uses delayed TX for the final.
Final	Three 40-bit collar hardware timestamps: poll TX, response RX, final TX.	Anchor combines these with its local timestamps to calculate range.
Range report	Signed int32 range in millimetres; uint8 status (valid / failed / reboot).	Use only valid, positive ranges from the same cycle. A failed slot mutes feedback.
Survey report	Signed int32 anchor spacing in millimetres; uint8 validity; new survey version in common fields.	Install spacing before enabling feedback. Resurvey after anchor movement or reboot; clear old pairs.

4.2 Zones, safety and logging



Run control at least every 5 ms. A direct Safe → Boundary transition is allowed.

Figure 8. Control priority. Fault handling and the dwell latch override all zone and debug output requests.

Provisional thresholds are 1.0 m for warning and 0.3 m for tone, with 0.2 m exit hysteresis. These values are tunable; the tolerance results below show that a 0.3 m zone is not yet validated. A merged zone/feedback controller requests outputs. The safety gate may mute or limit that request immediately before actuation converts it to GPIO/PWM. It also applies to debug commands.

Table 7. Zone transitions and safety overrides.

State	Requested behavior / transition
Safe	Both outputs off. Enter boundary directly at ≤ 0.3 m; otherwise enter warning at ≤ 1.0 m.
Warning	Vibration. Return to safe above 1.2 m; enter boundary at ≤ 0.3 m.
Boundary	Tone; motor off. Above 1.2 m go directly to safe; otherwise return to warning above 0.5 m.
Fault / stale	Mute within 5 ms of a failed estimate, reported fault or missed slot; mute by age 100 ms if updates cease. At startup/reboot, require a valid survey and two consecutive fresh pairs. Anchor movement requires a manual re-survey; it is not automatically detected.
Dwell timeout	After 10 s continuously outside safe, mute and latch. Brief invalid samples do not reset the timer. Rearm only after 1 s of fresh valid safe readings.

A single support/log module on each device collects status and writes bounded, non-blocking UART logs through the drivers. Log ranges, rejected samples, geometry, state, faults and output commands. The current repository provides role-based flashing and a radio SPI-ID diagnostic; ranging and control remain implementation work.

Table 8. Control and timing verification.

Requirement	Verification and pass condition
Crossing-to-drive ≤ 50 ms	Move the collar fixture across a marked zone threshold with an optical reference or equivalent synchronized ground truth. Scope the reference and MOSFET gate for ≥ 20 crossings each direction; all must meet 50 ms. Separately time record-received $\rightarrow$ GPIO. Mechanical motor spin-up is recorded separately.

Requirement	Verification and pass condition
Stable hysteresis	Replay threshold-crossing traces, then hold the fixture near a zone threshold for 15 min. After settling, no repeated safe/warning oscillation. Repeat near the 0.3/0.5 m tone thresholds.
Mute and dwell cutoff	Inject invalid geometry, old sequences, missing reports and anchor faults. Scope an injection-marker GPIO and both MOSFET gates, with probe grounds at TP1. Mute within 5 ms of a detected fault or failed slot, and by 100 ms sample age for silent data loss. After 10 s non-safe dwell, cutoff must occur within 5 ms and stay latched until 1 s of fresh safe readings. Log detection, gate transitions and recovery.

5 Tolerance analysis

5.1 Geometry and the error metric

The difficult interface is range measurement $\rightarrow$ boundary distance. Let anchors be $A = (0,0)$ and $B = (L,0)$, with measured ranges r_A and r_B . Compute $x = (r_A^2 - r_B^2 + L^2)/(2L)$ and $q = r_A^2 - x^2$. Reject nonpositive inputs and impossible triangles before using the result. For valid geometry, distance to the finite segment is r_A when $x < 0$, r_B when $x > L$, and $\sqrt{q}$ otherwise. Mirror ambiguity does not affect a boundary that works from either side.

At a fixed true distance d , $RMSE^2 = \text{Var}(\hat{d}) + [E(\hat{d}) - d]^2$. Standard deviation alone measures spread; RMSE also includes bias. Even unbiased range inputs can yield a biased distance estimate because the geometry is nonlinear and invalid samples are rejected. Measure range bias through calibration rather than assuming it is zero.

5.2 Limits of the first-order calculation

For an interior midpoint, $r = \sqrt{(L/2)^2 + d^2}$. If the two range errors and spacing error are independent, first-order propagation gives $\sigma_d^2 \approx r^2 \sigma_r^2 / (2d^2) + L^2 \sigma_L^2 / (16d^2)$. The symbols σ are standard deviations. This approximation assumes local linearity and omits input bias, it becomes unreliable near the line, where division by d magnifies the estimate. Correlated errors require covariance terms. [11]

We checked the full nonlinear estimator with 2,000,000 reproducible Gaussian trials per case: $d = 0.30$ m at the midpoint, $\sigma_r = 0.10$ m per range, and the spacing uncertainty shown below. A trial represents an independent static deployment; its spacing error is not redrawn for every update within a deployment.

Impossible geometry is rejected, not silently clamped to zero. The bias column adds the same fixed offset to both ranges. These distributions are assumptions, not measured DWM3000 performance. Monte Carlo is useful here because it propagates the nonlinear model directly. [12]

Table 9. Original strict estimator: nonlinear results versus first-order approximation.

L / σL (m)	Range bias (m)	Linear σd (m)	Valid std / bias (m)	Valid RMSE (m)	Rejected
2 / 0	0	0.246	0.146 / +0.071	0.162	26.6%
2 / 0.10	0	0.297	0.157 / +0.095	0.183	30.5%
4 / 0.10	0	0.582	0.214 / +0.219	0.306	39.8%
2 / 0.10	+0.10	0.297	0.163 / +0.250	0.298	4.8%
2 / 0.10	+0.20	0.297	0.143 / +0.427	0.450	0.2%

The TA's concern is confirmed: at $L = 2$ m with uncertain spacing, the accepted distance standard deviation is about 0.157 m, well below the linear estimate of 0.297 m. But about 31% of samples are rejected. A +0.20 m range bias gives an even smaller standard deviation while increasing RMSE to 0.450 m. Therefore neither standard deviation nor accepted-sample RMSE alone proves reliable operation.

The original strict-rejection estimator cannot meet availability on the line: with unbiased symmetric noise and exact spacing, roughly half the range pairs have $rA + rB < L$. Better precision reduces the size of that inconsistency, but not its probability at $d = 0$. The 0.3 m tone threshold and temporal stability therefore remain unverified.

5.3 Candidate refinement and feasibility

A proposed refinement, awaiting the team's choice, fits noisy ranges to the nearest feasible pair before calculating distance. Set $s = \max(rA + rB, L)$, $t = \text{clip}(rA - rB, -L, L)$, then $rA' = (s + t)/2$ and $rB' = (s - t)/2$. This minimizes equal-weight squared range corrections. Reject nonpositive inputs and any pair requiring more than 0.30 m correction to either range; log every correction. Stale data, packet errors and anchor faults still mute feedback.

We simulated the ten test positions with $\sigma_r = 0.10$ m, 200,000 independent samples per case, and fixed per-anchor biases of -0.05 , 0 or $+0.05$ m crossed with fixed spacing errors of -0.10 , 0 or $+0.10$ m. A ± 0.10 m spacing-error limit is not the same as $\sigma_L = 0.10$ m. These are assumed error budgets, not measured radio specifications. Results below summarize the sampled cases, not a continuous worst-case proof.

Table 10. Candidate estimator comparison over the sampled positions and offsets.

Scenario	Largest valid RMSE	Lowest geometry validity	Meets both targets?
Strict rejection; 2 m, zero bias / spacing error	0.342 m	49.91%	No
Proposed correction; 2 m, stated offset grid	0.456 m	99.61%	Yes, in simulation
Proposed correction; 4 m, stated offset grid	0.643 m	99.77%	No
Proposed correction; 2 m, $+0.20$ m bias on both ranges, exact spacing	0.665 m	$\sim 100\%$	No

The 2 m candidate meets the 0.5 m RMSE and 95% geometry-availability targets across the tested grid; the 4 m and large-bias cases show why calibration and spacing matter. Geometry validity excludes packet loss. With eight frames per cycle, independent 99.5% frame delivery would give about 95.7% usable cycles after geometry rejection; correlated losses must be measured. This analysis does not certify the 100 ms gap limit, 50 ms physical response or narrow-zone stability. Before adoption, measure LOS/NLOS bias, replay full time series and keep the existing acceptance limits.

6 Cost analysis

Costs below are rough USD replacement estimates for one collar, without tax or shipping. They are planning figures, not quotes. Shop stock must be confirmed. Order quantities include modest assembly spares; installed quantities define the design.

Table 11. Collar component and cost estimates.

Part / manufacturer and reference	Installed / obtain	Unit estimate	Installed cost
ESP32-WROOM-32E-N4, Espressif (U2) [2]	1 / 1	\$4.00	\$4.00
DWM3000, Qorvo (U3) [3]	1 / 1	\$25.00	\$25.00
AP2112K-3.3TRG1, Diodes Inc. (U1) [4]	1 / 2	\$0.50	\$0.50
MCP73831T-2ACI/OT, Microchip (U4) [5]	1 / 2	\$0.75	\$0.75
USB4125-GF-A-0190, GCT (J4) [6]	1 / 2	\$1.00	\$1.00
AO3400A, AOS (Q1/Q2)	2 / 4	\$0.25	\$0.50
SS14FL, onsemi (D1/D2)	2 / 4	\$0.20	\$0.40
SMF4L5.0A, Littelfuse (D5)	1 / 2	\$0.50	\$0.50
LTST-C171GKT, Lite-On (D3/D4)	2 / 4	\$0.15	\$0.30
CEM-1203(42), Same Sky (BZ1) [8]	1 / 2	\$1.50	\$1.50
Adafruit 805 SPDT (SW1) [10]	1 / 1	\$0.95	\$0.95
B2B-PH-K-S, JST (J1/J2)	2 / 3	\$0.35	\$0.70
1718560005, Molex (J3)	1 / 2	\$0.40	\$0.40
4-pin 2.54 mm SMD header (J5), match footprint	1 / 2	\$0.50	\$0.50
330 Ω RK73H2ATTD3300F, KOA (R8/R10)	2 / 5	\$0.05	\$0.10
1 k Ω RMCF0805JT1K00, Stackpole (R14/R16)	2 / 4	\$0.05	\$0.10
10 k Ω RMCF0805JG10K0, Stackpole (R12/R15)	2 / 4	\$0.05	\$0.10
100 k Ω RMCF0805JT100K, Stackpole (R2/R9/R11)	3 / 5	\$0.05	\$0.15
5.1 k Ω RMCF0805JT5K10, Stackpole (R17/R18)	2 / 4	\$0.05	\$0.10
2.2 Ω RC0805FR-072R2L, Yageo (R19)	1 / 3	\$0.05	\$0.05

Part / manufacturer and reference	Installed / obtain	Unit estimate	Installed cost
100 nF CC0805KRX7R9BB104, Yageo (C9/C11)	2 / 4	\$0.10	\$0.20
1 μ F CL21B105KBFNNNG, Samsung (C1/C4/C12)	3 / 5	\$0.15	\$0.45
10 μ F GRM21BR61H106ME43L, Murata (C7/C8/C10/C13/C14)	5 / 7	\$0.40	\$2.00
Protected 400 mAh pack, Adafruit 3898 candidate [7]	1 / 1	\$6.95	\$6.95
Coin motor, Adafruit 1201 candidate [16]	1 / 1	\$1.95	\$1.95
JST-PH motor pigtail; supplier to match J2	1 / 1	\$1.00	\$1.00
Collar electronics subtotal	—	—	\$50.15

Obtain the listed resistors except R19, capacitors, LDO and LEDs through the E-shop where stock is confirmed. The self-service drawers list SS14FL, CEM-1203(42) and the Molex header; verify the diode package. The paid store lists Adafruit 805. Other exact parts need external sourcing or a confirmed local match. J5 needs the surface-mount footprint-compatible header, not a standard through-hole substitute.

The collar BOM totals about \$50.15 installed, or \$58.80 at the listed order quantities. Allow \$25 for a small PCB batch/stencil, \$10 for the printed case, screws and strap, and \$15 for an external programmer: about \$110 total new materials before tax/shipping if supplies and cables are reused. These fabrication figures are allowances, not shop quotations; no paid machining is planned.

Three Makerfabs boards are already owned: two anchors and one development board, later spare. At an assumed replacement value of \$40 each, their \$120 cost is separate from the collar BOM. An optional fourth board adds about \$40. No additional anchor MCU or radio modules are counted. Reuse two 5 V USB power outputs, data cables, five programming jumpers and a USB-C charging cable; allow roughly \$15 if these are missing.

Labor estimate: each of three members contributes 15 h/week for 12 active weeks at an assumed \$45/h. Per person: $180 \times \$45 \times 2.5 = \$20,250$; total labor = \$60,750. Including order quantities, \$50 fabrication/programming allowances and \$120 owned-board replacement value gives an estimated project total of \$60,978.80, excluding optional equipment, tax and shipping.

7 Schedule

The schedule below assigns one task to each member for every remaining semester week. Peter leads firmware, Shi Xian leads power/PCB work, and Shi Yang leads feedback/mechanical integration. Course deadlines follow the official calendar; the team reviews integration results together.

Table 12. Weekly responsibilities for the remaining semester.

Week	Peter	Shi Xian	Shi Yang
6	Finalize two-anchor protocol and logging	Review v2 fabrication package; finalize orders	Trial-fit enclosure, pack and motor candidates
7	Implement DS-TWR on existing boards	Assemble/check power and charging	Verify motor and buzzer drivers
8	Implement geometry and invalid-data handling	Bring up MCU/UWB and programmer	Integrate enclosure and feedback
9	Implement zones, hysteresis and safety	Measure rail, current peaks and heating	Test dwell cutoff and default-off behavior
10	Collect range/bias data and refine calibration	Resolve hardware faults and document fixes	Run latency and mechanical-fit tests
11	Run LOS accuracy and update-availability tests	Support test setup and hardware rework	Run stationary hysteresis and dwell tests
12	Run NLOS tests and assess range bias	Repeat rail and charging checks after rework	Repeat latency and enclosure-fit tests

Week	Peter	Shi Xian	Shi Yang
13	Resolve integration faults; freeze demo candidate	Update schematics, BOM and assembly notes	Prepare demonstration fixture and figures
14	Repeat acceptance tests on frozen firmware	Review final hardware and costs	Rehearse the complete demonstration
15	Draft firmware and analysis sections of final report	Draft hardware and verification sections	Draft mechanical, safety and results sections
16	Verify release firmware and archive logs	Complete final hardware inspection	Run final demonstration and integration checks

8 Societal impact, standards, ethics and safety

A local boundary could reduce obstructions and avoid electric shock, while keeping location data off cloud services. Reusing development boards reduces cost and waste. It may still fail near reflections or body blockage, and sound or vibration can distress an animal. We will describe measured limitations honestly and will not present the prototype as reliable containment or a demonstrated training method.

Relevant standards include IEEE 802.15.4 UWB PHY features supported by the radio, USB Type-C requirements for the charge connector, and applicable FCC Part 15 UWB rules. Using modules does not certify the finished product. Follow vendor radio settings and review regulatory applicability before use outside supervised laboratory development. IEEE ethical principles support accurate reporting, disclosure of limits and protection of users. [3], [13], [14]

Demonstrate with a fixture, not a live animal. Any later animal testing requires discussion with course staff and applicable institutional approval. The safety gate, default-off drivers and 10 s timeout limit unintended output, but do not prove that any sound or vibration level is harmless.

Follow ECE 445 laboratory and battery-safety guidance. Before connecting the pack, verify polarity and inspect it for damage. Begin board bring-up on a current-limited supply. Charge only while switched off, removed from the collar wearer and under supervision in the approved charging area. Stop for swelling, damage or unusual heating. The switch disconnects the run supply; it cannot detect whether the device has

been removed from an animal. Disconnect programmer signals before OFF/CHARGE to avoid back-powering. [15]

Insulate the battery and cable joints, provide strain relief, secure the motor and cover solder joints and sharp edges. Keep conductive objects out of antenna areas and away from the pack. The prototype enclosure is not waterproof. Confirm mechanical fit and safe temperature before any wearable demonstration.

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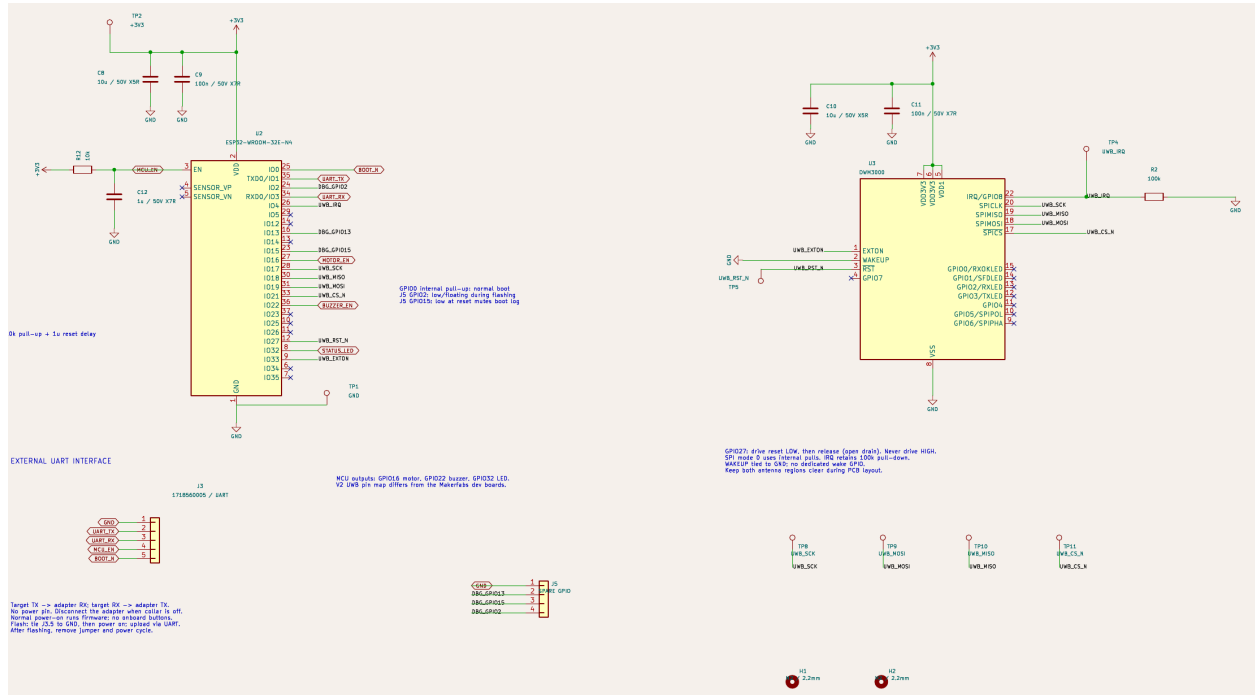
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Reproducible calculations are in `tools/design_document_analysis.py` (seed 20261002) and `tools/design_document_feasibility.py` (seed 20261003), with figures and results in `docs/design-review-assets/` in the project repository.

Appendix A — Current collar schematics

The following figures show the saved v2 schematic. Named nets connect across sheets. Use the linked vector PDF for pad labels and full-size inspection.

[Open the complete v2 schematic PDF](#)



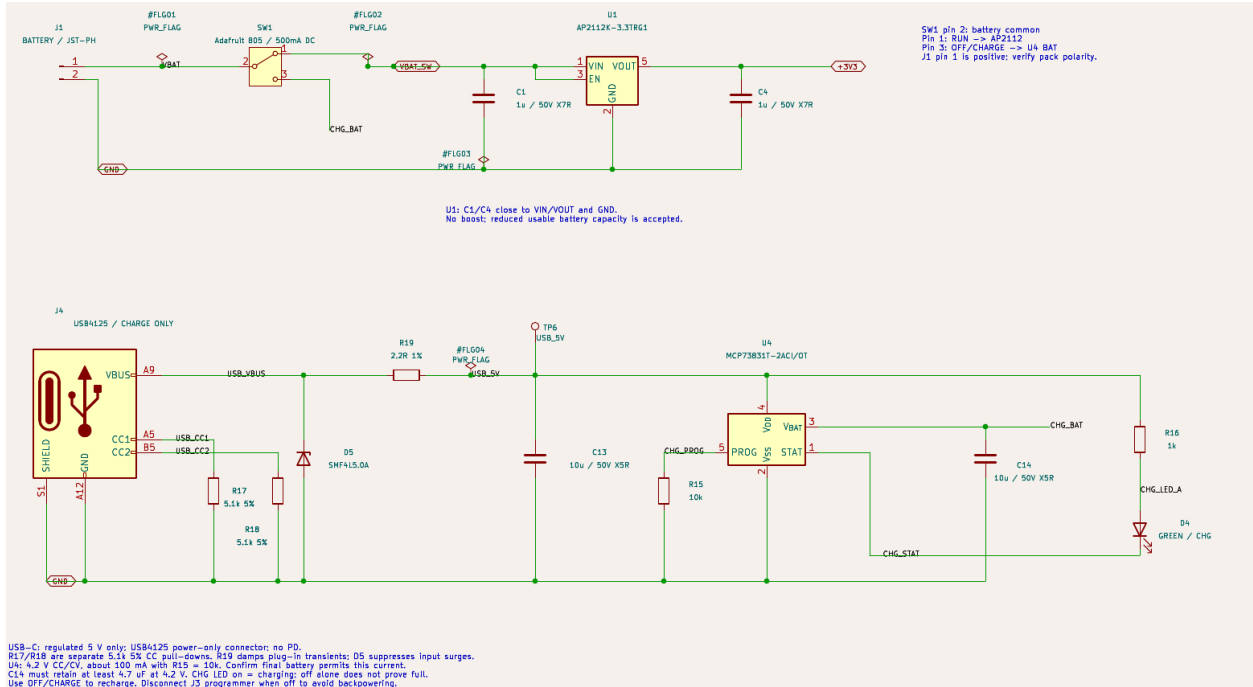


Figure A2. Run supply and off-only USB-C charging.

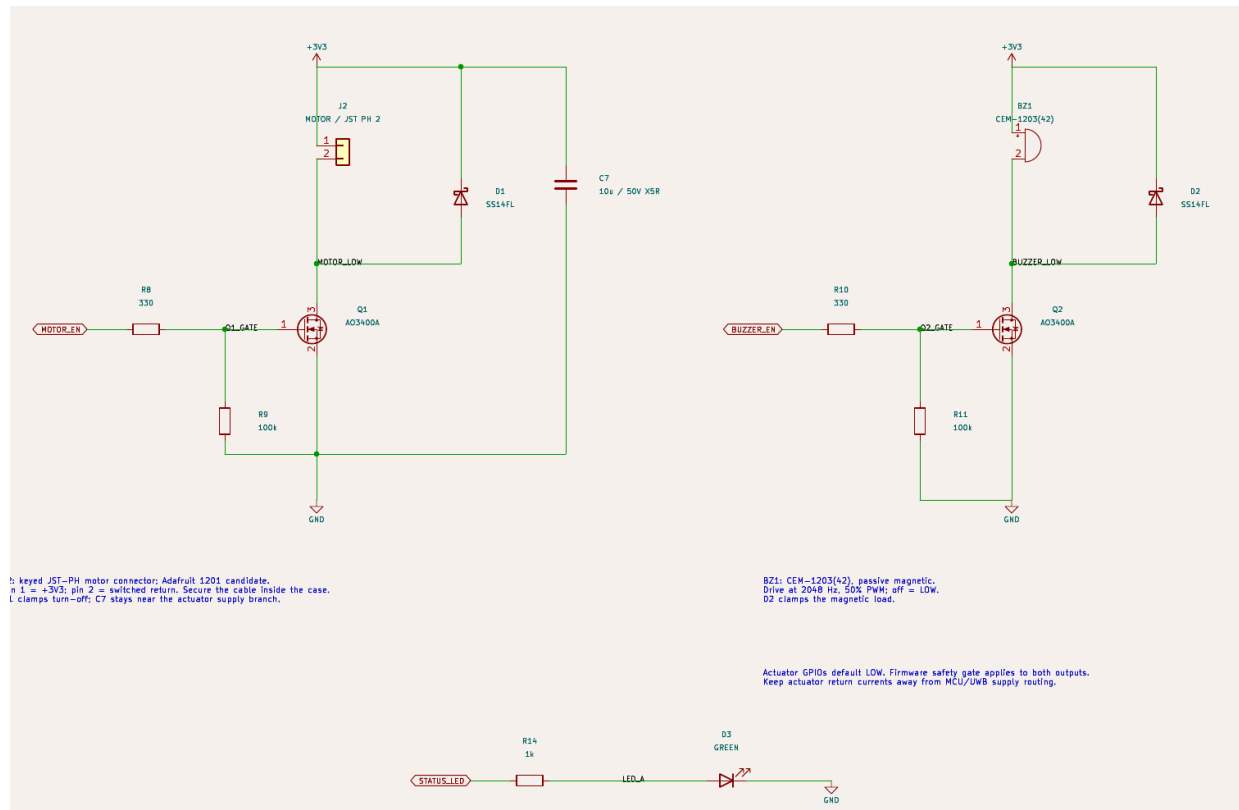


Figure A3. Motor, magnetic buzzer and status LED drivers.