

DIKI-DIKI Project Proposal

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Contents

1	Introduction	1
1.1	Problem	1
1.2	Solution and Visual Aid	2
1.3	High-level Requirements	2
2	Design	3
2.1	Block Diagram	3
2.2	Subsystem Overview	3
2.2.1	Input Filter	3
2.2.2	Primary Power Stage	3
2.2.3	Secondary Rectifier Stage	4
2.2.4	Output Filter	4
2.2.5	Control/Sensing	4
2.2.6	Telemetry	5
2.2.7	Signal Isolator	5
2.2.8	Isolated Gate Driver	5
2.2.9	Isolated Power	5
2.3	Subsystem Requirements	6
2.3.1	Input Filter	6
2.3.2	Primary Power Stage	6
2.3.3	Secondary Rectifier Stage	6
2.3.4	Output Filter	6
2.3.5	Control/Sensing	7
2.3.6	Telemetry	7
2.3.7	Signal Isolator	7
2.3.8	Isolated Gate Driver	7
2.3.9	Isolated Power	8
2.4	Tolerance Analysis	8
2.4.1	Project Risk	8
2.4.2	Signal Propagation Analysis	8
2.4.3	Initial Simulation	9
3	Impact and Standards	10
3.1	Ethics, Safety, Societal Impact, and Standards	10
	References	11

1 Introduction

1.1 Problem

As emissions regulations tighten across major markets, automakers have begun electrifying and hybridizing their vehicles. The electrification pathway delivers meaningful efficiency gains and emissions reductions, whether the platform retains a combustion engine or not. Such vehicles still need a 12V rail to power legacy safety-critical and comfort electronics, such as power steering assist modules, infotainment, lighting control, and in many platforms ADAS sensors. This means the isolated 48V-to-12V DC-DC converter is a mandatory subsystem present in a rapidly growing fraction of new vehicles.

Mild-hybrid systems recover energy that would otherwise be lost during braking and coasting, reducing total energy consumption by roughly 10-15% relative to combustion vehicles, a benefit that scales into a meaningful reduction in global emissions as adoption grows. But the isolated 12V rail itself is not specific to mild-hybrids. Every electrified platform, from 48V mild-hybrids to full high-voltage EVs, still needs to power the same legacy 12V loads. The DC-DC converter that does so doubles as a redundant supply if the low-voltage battery fails in a crash, a safety benefit that holds regardless of how electrified the platform is.

Despite this growing importance, many production 48V-to-12V converters still rely on analog control loops, specifically compensator ICs with fixed, hard-to-retune behavior and no native path for reporting fault conditions or system health back to the vehicle's diagnostic network. Modern automotive diagnostics increasingly depend on CAN-reportable fault codes for everything from routine maintenance flagging to safety-critical fault isolation after a collision, and an analog-only converter simply cannot participate in that diagnostic ecosystem without significant additional hardware. As vehicle power electronics continue moving toward higher voltages from 48V to 400V and above, the industry needs control and magnetics design approaches that are portable across voltage classes. The 48V-to-12V case is an immediate, tractable learning platform, but the digital control architecture and magnetics-design methodology are intended to generalize upward to higher-voltage isolated DC-DC stages, not to be a mild-hybrid-specific solution.

1.2 Solution and Visual Aid

We propose a digitally controlled isolated DC-DC converter using a half-bridge topology, demonstrating a control and magnetics design approach that scales toward higher-voltage (e.g., 400V-to-48V-class) automotive systems, implemented and validated at a reduced-voltage scale (48V-to-12V) for lab safety. By replacing the analog control loop with a fully digital implementation, the design directly addresses the diagnostic-reporting gap in existing solutions while preserving — and rigorously validating — the galvanic isolation barrier that automotive safety standards and basic public-safety considerations demand.

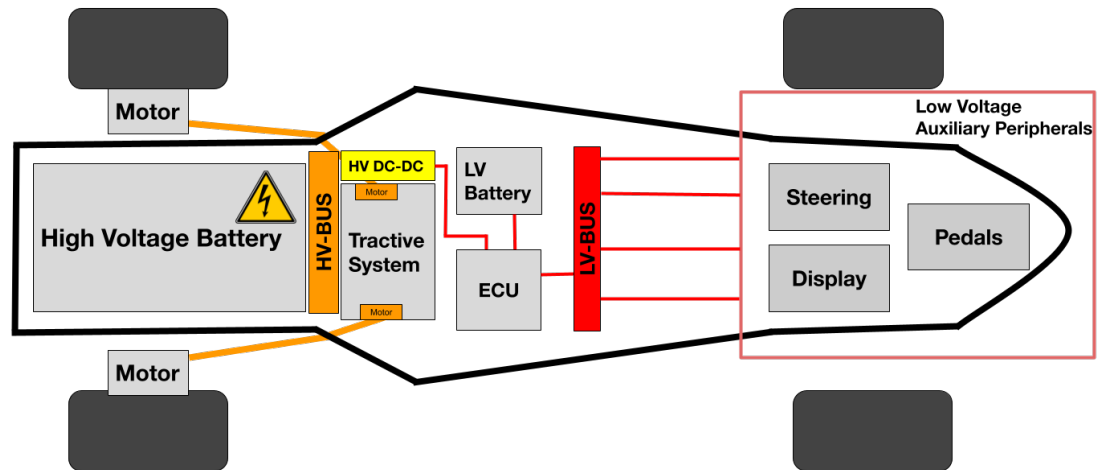


Figure 1. Application of Isolated DC-DC in Automotive EV Power Distribution

1.3 High-level Requirements

- The converter shall regulate a 12V DC output within $\pm 5\%$ across the full input voltage range of 20V to 60V.
- The converter shall deliver at least 125W of continuous output power while maintaining a minimum efficiency of 90%, measured at 48V input.
- The converter shall maintain a galvanic isolation resistance of at least 10 M Ω between the high-voltage and low-voltage domains.

2 Design

2.1 Block Diagram

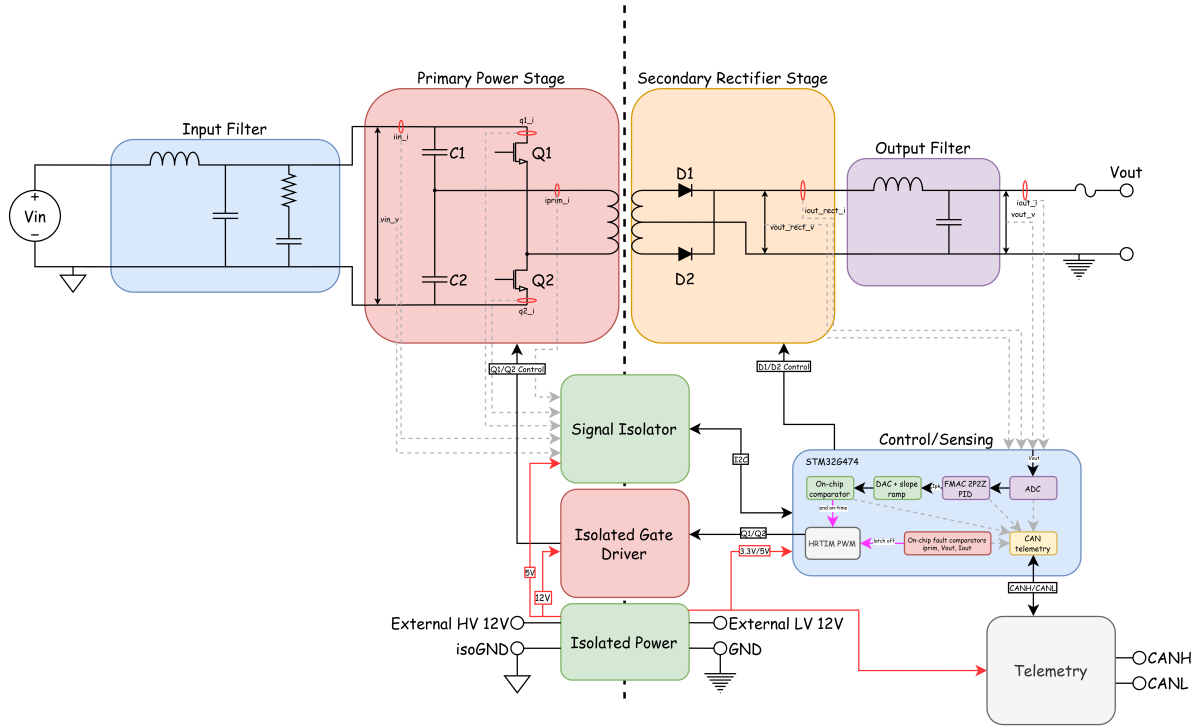


Figure 2. System block diagram of the isolated half-bridge DC-DC converter.

2.2 Subsystem Overview

2.2.1 Input Filter

The input filter is the entry point for high-voltage power into the DC-DC converter, attenuating conducted noise and switching-frequency disturbances before they reach downstream components. Its output feeds the primary power stage, presenting it with a clean, low-impedance source rather than the raw, noise-coupled input rail.

2.2.2 Primary Power Stage

The primary power stage converts the DC input voltage into an AC square wave to transfer power across the transformer. It does this using a half-bridge topology with two switches ($Q1, Q2$) and a pair of split-bus capacitors ($C1, C2$) that set the primary's return reference and block DC bias current from reaching the transformer.

2.2.3 Secondary Rectifier Stage

The secondary rectifier stage converts the AC waveform across the transformer secondary into a unidirectional waveform whose average value matches our V_{out} target. The initial implementation uses rectifier diodes; active switches will be added for synchronous rectification as a stretch goal to improve efficiency.

2.2.4 Output Filter

The output filter attenuates the switching-frequency ripple in the rectified output, producing a stable 12V DC rail. Using purely reactive elements (inductor and capacitor) rather than dissipative ones keeps this filtering ideally lossless.

2.2.5 Control/Sensing

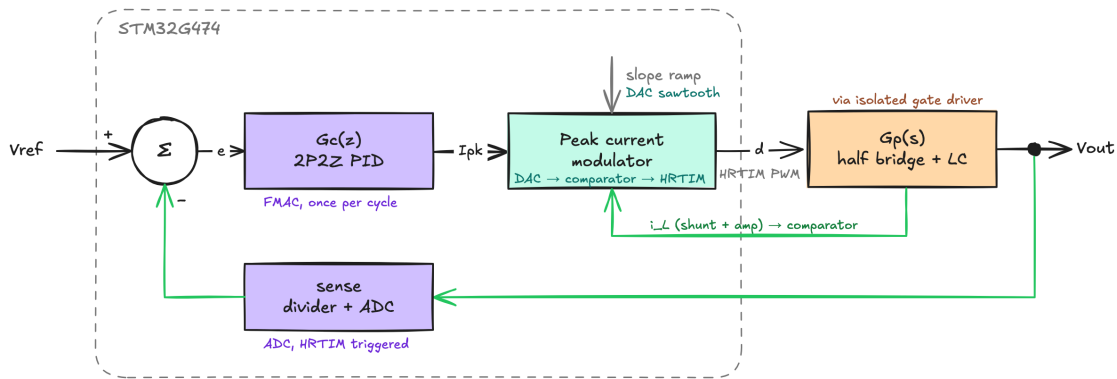


Figure 3. Control System Diagram.

The control/sensing subsystem regulates the output, enforces protection, and produces the data the telemetry subsystem reports. It is built on an STM32G474 referenced to the LV ground. The G474 was chosen because its peripheral set is designed for power applications. It has a high-resolution timer (HRTIM) for gate signal generation, on-chip analog comparators with internal DACs for fast current limiting and fault trips, a filter accelerator (FMAC) for running the compensator, and five independent ADCs [9].

Nine signals are sensed by the STM. Input voltage and current, Q1, Q2 and transformer primary currents, rectified voltage and current between the rectifier and output filter, and output voltage and current. All ADC sampling is triggered from the HRTIM so every measurement is taken at a fixed point in the switching cycle. Board temperature is also measured at several points, including the rectifier diodes, primary FETs and transformer, using digital temperature sensors on an I2C bus.

Because control is digital, the control mode is a firmware decision and can be changed later

without new hardware. The initial plan is peak current mode. A voltage loop runs in firmware every switching cycle, compares the output voltage to 12V, and runs a 2P2Z PID compensator whose output is a peak current command. That command is written to an internal DAC and sets the threshold of an on-chip comparator watching the output inductor current. When the current reaches the threshold, the comparator ends the active FET's on-time directly in hardware. The DAC threshold ramps down through each cycle for slope compensation, following the structure used in TI's digital peak current mode reference design [10]. Q1 and Q2 currents are also monitored to protect against flux imbalance causing a DC bias.

Three more on-chip comparators are used to watch primary current, output voltage and output current and shut off gate outputs in unsafe conditions. Undervoltage and overtemperature are handled in software. Any of the above faults latches the converter off and reports the cause over CAN, and the latch can only be cleared by a CAN command so the converter never restarts on its own.

2.2.6 Telemetry

The telemetry subsystem is the converter's interface to the vehicle diagnostic network. It consists of the G474's FDCAN peripheral and a CAN transceiver on the LV side, communicating per the ISO 11898 CAN standard [6, 7]. It publishes periodic status frames containing all nine sensed quantities, board temperatures, the peak current command, computed input, rectified and output power, efficiency, and controller state. When a fault occurs it publishes a fault frame identifying the cause and the sensed values at the moment of the trip. It also accepts commands to enable and disable the converter, clear a latched fault, and adjust the output setpoint within a bounded range.

2.2.7 Signal Isolator

To maintain galvanic isolation between the HV and LV domains, no conductive path may cross the barrier. The signal isolator transfers both analog and digital signals across this boundary using an internal transformer, preserving isolation while still passing the sensing/control signals the converter needs.

2.2.8 Isolated Gate Driver

The isolated gate driver maintains galvanic isolation across the primary-secondary boundary while sourcing and sinking the gate current needed to meet switching timing requirements, with desaturation and overshoot protection built in.

2.2.9 Isolated Power

The isolated power subsystem provides regulated supply rails to the analog sensing and gate drive circuitry on the primary side, while maintaining galvanic isolation from the LV domain that

sources that power. Since the gate driver and detection circuitry need to be active before the main converter is even regulating output, this bias supply has to come up independently and cannot rely on the converter's own output as a bootstrap source.

2.3 Subsystem Requirements

2.3.1 Input Filter

1. The device input should include reverse polarity protection to prevent hardware damage during an inverted input connection.
2. The device input filter should be able to withstand the inrush current during start-up conditions with the maximum load of 125 W and the lowest input voltage at 20 V.

2.3.2 Primary Power Stage

1. The primary power stage shall support continuous primary power transfer of at least 140 W.
2. The DC bias middle capacitors shall maintain a reference within 5% of $V_{in}/2$.
3. The primary power stage switches shall be able to withstand the maximum switch stress during periodic steady state conditions, which is defined by the peak switch stress product $S_S = V_{peak} \cdot \Delta I_{pk}$.

2.3.3 Secondary Rectifier Stage

1. The secondary rectifier stage shall have compatibility for both synchronous and asynchronous rectification.
2. The secondary rectifier stage shall be able to withstand a continuous current of 12A.
3. The secondary rectifier stage shall be able to withstand an over-current event of 15A for at-least 200ns.
4. The secondary rectifier stage shall be able to withstand no-load conditions.

2.3.4 Output Filter

1. The output filter must maintain a 5% output voltage ripple during all nominal modes of operation, including steady state load from 0-20 A.
2. the output filter must be able to withstand the inrush current during nominal starting conditions at maximum load.

2.3.5 Control/Sensing

1. Step response to a 50% load (5.2 A $\leftrightarrow$ 10.4 A) shows overshoot and undershoot below 5%, settling time to $\pm 2\%$ under 1 ms, and no sustained oscillation.
2. Voltage loop executes once per switching cycle in under 1.5 μ s.
3. Voltage measurements within $\pm 1\%$ and current measurements within $\pm 2\%$ after calibration.
4. Primary overcurrent (150% of rated peak), output overvoltage (above 14 V), and output overcurrent (above 15 A) shut off all gates within 500 ns.
5. Soft start reaches 12 V within 20 ms with inrush below 150% of rated.
6. Faults latch the converter off until a CAN clear command is received.

2.3.6 Telemetry

1. Status frame with all sensed quantities, temperatures, computed powers, efficiency, and controller state published at 100 Hz or faster.
2. Fault frame with cause and sensed values at the trip published within 10 ms of a latch.
3. Enable, disable, fault clear, and setpoint commands acted on within 10 ms. Setpoints outside 11–13 V are rejected.
4. Node recovers from bus-off within 1 s.
5. All frames decodable with the provided DBC file.

2.3.7 Signal Isolator

1. The signal isolator shall transmit all primary side feedback signals to the microcontroller.
2. The signal isolator shall transmit all signals with at least twice the bandwidth of the inner control loop.

2.3.8 Isolated Gate Driver

1. The Isolated Gate Drive subsystem must be capable of driving the primary side switches at a minimum of 100kHz switching frequency.
2. The Isolated Gate Drive subsystem should be capable of turning off MOSFET in the case of a shoot-through, or MOSFET failure event within 500ns.

2.3.9 Isolated Power

- The isolated power network shall supply $3.3\text{ V} \pm 2\%$ to provide stable power to the microcontroller and control circuitry
- The isolated power network shall supply $5\text{ V} \pm 2\%$ to provide stable power to the isolated gate driver and signal isolator
- The isolated power network shall be able to withstand the current budget of all control circuitry, including but not limited to, the microcontroller, communication transceivers, amplifiers, isolated gate driver, and signal isolator.

2.4 Tolerance Analysis

2.4.1 Project Risk

Given our hard-switched half-bridge topology, switching loss and component non-idealities pose the primary risk to hitting our efficiency target. Digital control at our target frequency range also compresses our available timing margin. The full signal path from sensing through the microcontroller to gate-drive output must complete well within a single switching period, leaving limited room for propagation delay before it begins to affect regulation accuracy and, at the extreme, loop stability.

2.4.2 Signal Propagation Analysis

Table 1. Voltage feedback path delay (Vout sense → PWM update)

Stage	Delay
ADC sample + convert (12-bit, 40 MHz)	$0.35\text{ }\mu\text{s}$
Interrupt entry latency ($\sim 10\text{--}20$ cycles)	$0.2\text{ }\mu\text{s}$
ADC read + compensator execution	$0.2\text{--}0.3\text{ }\mu\text{s}$
DAC register write	$0.1\text{ }\mu\text{s}$
DAC output settling	$0.5\text{--}1\text{ }\mu\text{s}$
Total (with margin)	$\sim 2.5\text{ }\mu\text{s}$

Table 2. Current sensing path delays

Signal	Delay
Primary current: CT	50 ns
Primary current: analog summer	$\sim 200\text{ ns}$
Primary current total	$\sim 250\text{ ns}$
Output inductor current: current-sense amp	$\sim 100\text{ ns}$

At 100 kHz , $T_{sw} = 10\text{ }\mu\text{s}$. The voltage feedback path's $\sim 2.5\text{ }\mu\text{s}$ delay consumes roughly 25% of the switching period, making it the dominant contributor to overall loop delay. The current-

sensing paths (~ 250 ns for primary current, ~ 100 ns for output inductor current) are an order of magnitude smaller by comparison, confirming that digital signal-path delay—not analog sensing—is the limiting factor and primary consumer of available timing margin in this design. This analysis emphasizes the importance of peak current detection through the analog comparator, as that variable will drive the T_{on} of the half bridge switches. It is worth noting that this propagation timing analysis assumes a full-scale (0 to maximum) DAC step, whereas in practice the control loop will not command such large step changes, meaning the actual available timing margin is greater than this calculated worst case.

2.4.3 Initial Simulation

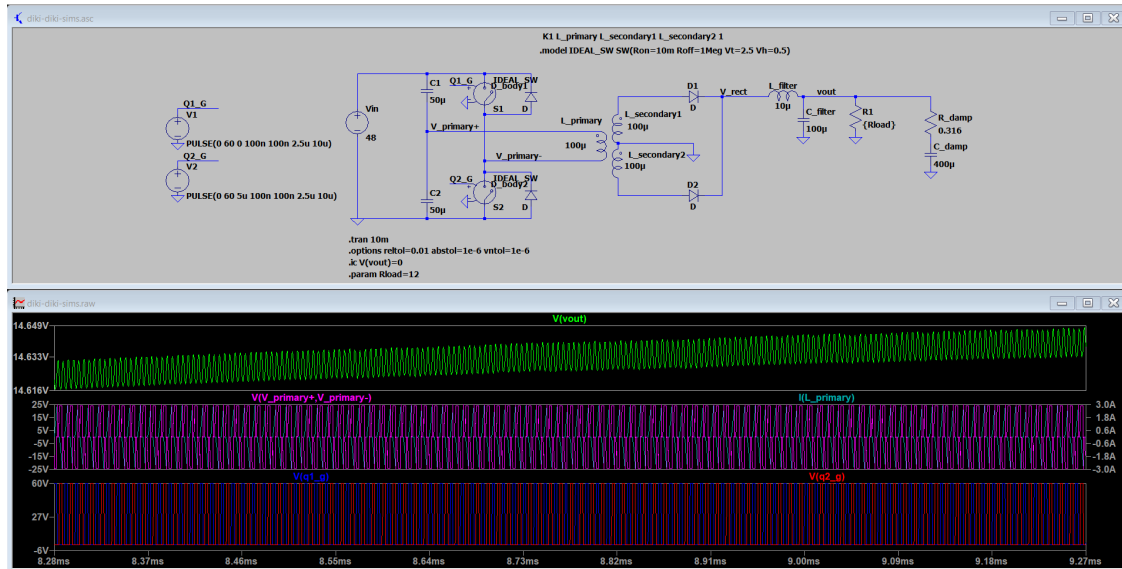


Figure 4. Initial LTspice simulations with open-loop control.

3 Impact and Standards

3.1 Ethics, Safety, Societal Impact, and Standards

The 48V to 12V converter is one of the components that makes mild-hybrid vehicles cheaper than full hybrids, which is the reason the architecture is spreading fastest in markets where a full EV is too costly. A converter that reports its own health over CAN also supports repair rather than replacement, since a fault code pointing to a specific stage lets a technician fix pinpoint issues rather than swap symptomatic modules. Digital control also opens the door for detailed fault response algorithms that improves safety and reliability. The trade is that a digital control brings new difficulties in compute and control requirements, as well as the potential for code bugs. We treat that as a design obligation to keep the hard protection paths in hardware, independent of software, so a firmware bug cannot cause a hazardous output.

The IEEE Code of Ethics asks engineers to hold safety standards and to be honest in stating claims based on available data [1]. Two places in this project call for care. First, we are validating at 48V and arguing the approach scales to higher voltage classes. We will report only what we measure and state clearly which conclusions are demonstrated and which are extrapolated. Second, efficiency figures are easy to inflate through selective test conditions. We will report efficiency across the full load range and input range, including the worst case, not only the peak.

The 48V input sits below the 60V DC threshold that IEC 61140 treats as hazardous live [2], which is the reason 48V was chosen as the lab scale for this project. A 48V bus with several amps available can sustain a DC arc, damage a probe tip or heat a ring or tool shorted across it. The input and output capacitors hold enough charge to spark when shorted after power is removed. The rectifier diodes will dissipate several watts at full load and can run hot enough to burn on contact. Our mitigations are a bench supply with current limit for all early testing, a discharge procedure, a simple enclosure or standoff keeping exposed copper away from hands, insulated probes, and the hardware over-current, over-voltage and over-temperature trips. The converter latches off on any fault and does not restart without an explicit command, so a fault cannot cycle unattended. Isolation between the HV and LV domains is verified with an insulation resistance test. ANSI/AAMI ES1-1993, the safe current limits standard used by the ECE 445 course, caps the risk current that may flow from an exposed conductive surface to ground at 100 μA under normal conditions and 500 μA under a single fault [3]. With a 48 V bus and the 10 M Ω isolation resistance required in Section 1.3, the leakage across the barrier is below 5 μA , so a person touching the LV side while the HV side is energized is well inside these limits.

The design targets the operating voltage range of ISO 21780, which defines the 48V electrical system for road vehicles [4], and the electrical load and transient conditions of ISO 16750-2 [5]. The CAN interface follows ISO 11898-1 for the data link layer and ISO 11898-2 for the physical layer [6, 7]. Isolation and protection against electric shock follow the principles of IEC 61140 [2], and the ISO 6469-3 requirements for electrical safety in electrically propelled road vehicles inform the isolation resistance requirement in Section 1.3 [8].

References

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