

Adaptive Power Factor Correction Device

Proposal:

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Introduction:

Problem:

Power factor (PF) correction is an important process in commercial electrical systems because many common loads, such as motors and transformers, are inductive. A poor power factor causes a system to draw more current and apparent power for the same amount of real power, increasing system losses, reducing available electrical capacity, and potentially increasing equipment and utility costs. Power factor correction, also known as reactive power compensation, improves power factor toward unity by supplying compensating reactive power. Because most commercial loads are inductive, this is commonly accomplished using capacitor banks.

Existing power factor correction solutions are often either non-adaptive or designed for large-scale commercial and industrial applications. Systems such as commercial automatic capacitor banks can be expensive and oversized for smaller commercial tenants, making them impractical for installation at the individual tenant-panel level.

There is therefore a need for a low-cost, adaptive power factor correction device that can be implemented at the tenant-panel level.

Solution:

Our project aims to establish the groundwork for an adaptive power factor correction system that could eventually be scaled to a commercial 480 Volt (V) electrical panel. The system will dynamically adjust reactive power compensation as load conditions change, helping reduce unnecessary current draw, electrical losses, equipment requirements, and potential utility costs.

To accomplish this, we are designing and implementing a single phase adaptive power factor correction prototype operating from a 15 V AC source. This allows the system to demonstrate the same sensing, computation, and capacitor-switching concepts at a voltage that is manageable for laboratory development and testing.

The system has four main subsystems:

1. **Sensing** – Measures the Alternating Current (AC) voltage and current waveforms and conditions them into signals that can be safely sampled by the microcontroller.
2. **Microcontroller Unit (MCU)** – Samples the voltage and current signals, computes root mean squared values (RMS) voltage and current, real power, apparent power, reactive power, and power factor, and determines the required capacitive compensation.
3. **Capacitive Switching** – Uses controlled triode for alternating currents (TRIAC) switching to connect or disconnect discrete capacitor stages in parallel with the load based on commands from the microcontroller.
4. **AC-to-DC Power Conversion** – Converts the 15 V AC input into approximately 3.3 V Direct Current (DC) to provide the low-voltage power supply required by the microcontroller and supporting electronics.

During operation, the microcontroller continuously samples the voltage and current waveforms and calculates the current power factor. The controller evaluates whether compensation changes are required at approximately 10-second intervals. To prevent unnecessary switching caused by small fluctuations or measurement noise, the controller will only modify the connected capacitor stages if the measured power factor changes by more than a predefined threshold, initially expected to be approximately 0.04.

If an adjustment is required, the controller determines the amount of reactive power compensation needed and selects the appropriate combination of discrete capacitor stages. Capacitors are then switched into or out of the circuit using isolated gate drivers and power TRIACs. Switching is synchronized with the AC waveform to reduce switching transients and inrush current, while bleeder resistors allow disconnected capacitors to discharge safely.

The final prototype will demonstrate adaptive power factor correction using a variable inductive load supplied from 15 V AC. As the load changes, the system will detect the resulting change in power factor and, when the change exceeds the defined threshold, automatically adjust the connected capacitance to maintain the power factor near the desired target of approximately 0.95. To reasonably meet this goal with a manageable amount of capacitors we will have a target range for PF of 0.93 - 0.97.

Visual Aid:

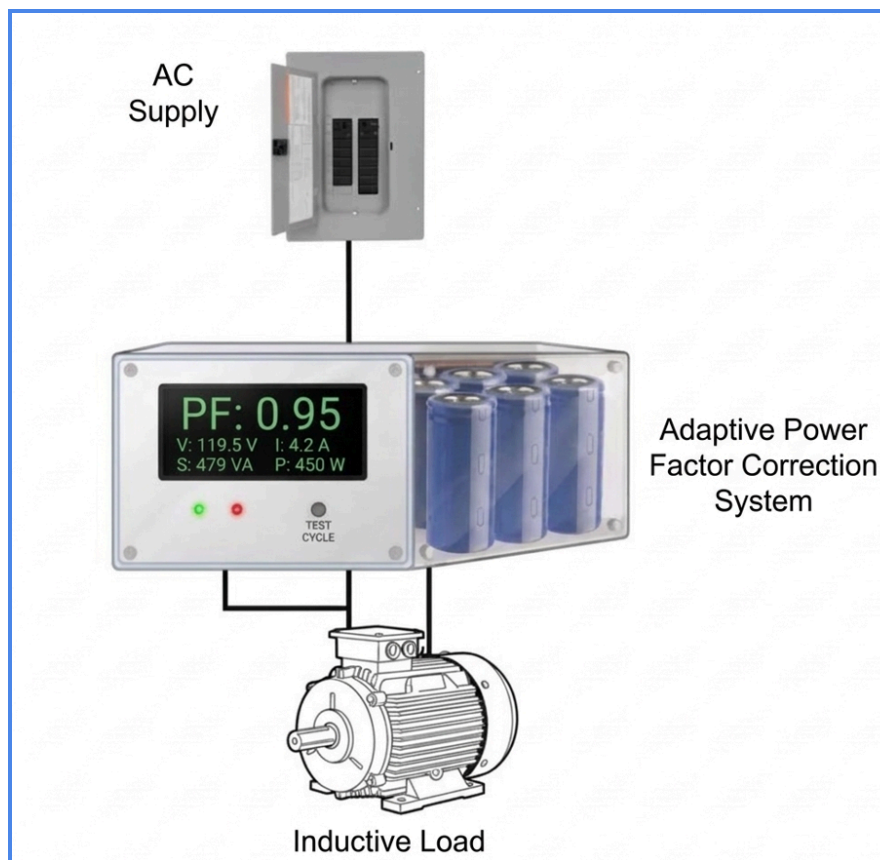


Figure 1: Visual Aid

High Level Requirements:

1. The system will measure AC voltage and current waveforms at 60 Hz with enough information to compute power factor with an accuracy of ± 0.05 compared to a reference measurement.
2. The system will sample the voltage and current waveforms at a rate of 5-10 kHz with consistent timing for accurate waveform reconstruction, phase detection, and power factor computation.
3. The system will improve the power factor to between 0.93-0.97 using adaptive capacitor switching under steady-state conditions. This will occur only when the current power factor is outside of this range.

Design:

Block Diagram:

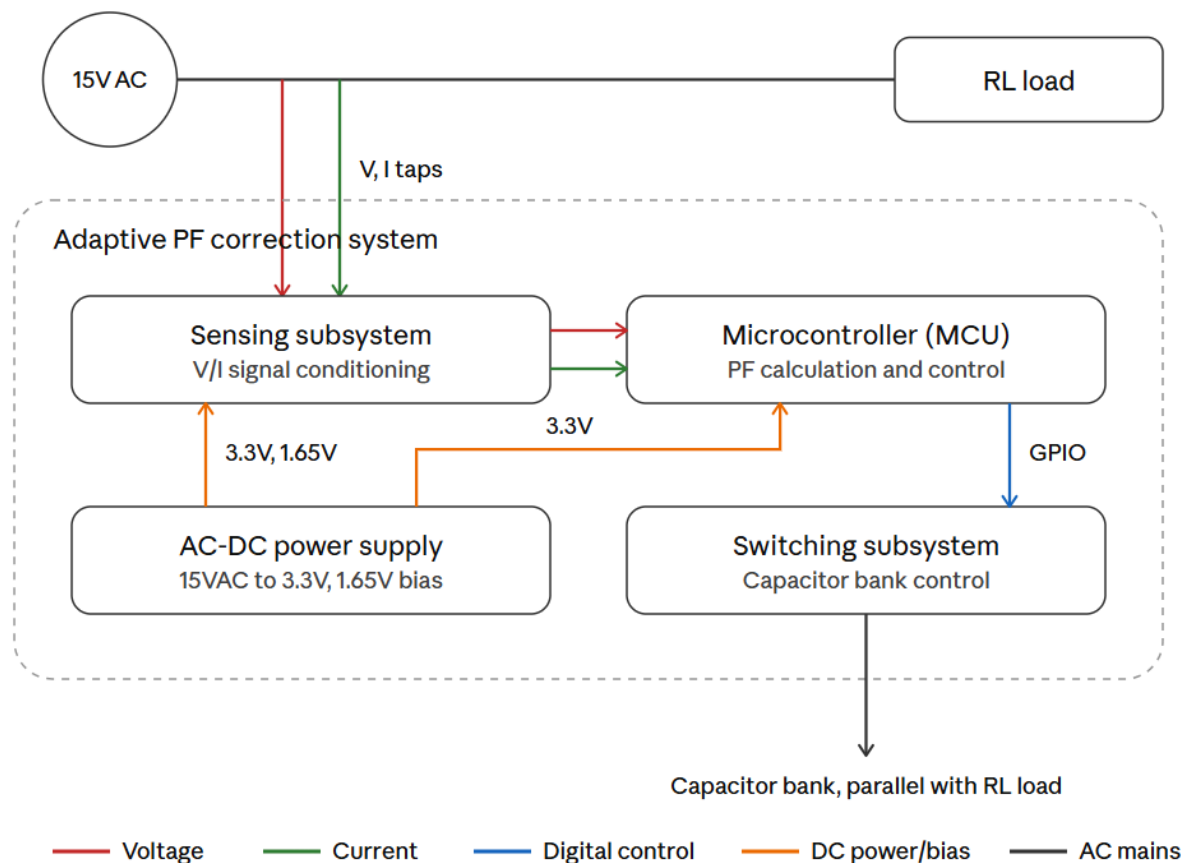


Figure 2: High Level Block Diagram

Sensing Subsystem:

Overview:

The sensing subsystem measures the AC voltage and current of the load and converts them into analog signals that are adjusted for the microcontroller's analog to digital converter (ADC) inputs. This subsystem directly interacts with the AC load and provides real-time waveform data to the MCU subsystem for power factor computation and control decisions.

The voltage sensing block uses a resistive voltage divider and a biasing network that shifts the scaled AC waveform into the appropriate input range of the ADC. The current sensing block uses a current transformer to scale the current and produce a proportional signal, which is also biased to match the ADC input parameters.

Both sensing blocks will rely on a reference voltage that is provided by the DC Power Supply subsystem so that the AC waveforms stay within the 0–3.3 V ADC range. The outputs will be continuous-time analog signals that represent the original voltage and current waveforms with accurate amplitude and phase information so the MCU subsystem can accurately reconstruct the signals and perform power factor calculations.

The key design considerations for this subsystem include input signal integrity, minimizing phase difference errors (for accurate PF calculations), and ensuring that all signals remain within safe voltage limits for the ADC. Filtering may be added to reduce high-frequency noise without significantly distorting the waveform or introducing phase shift.

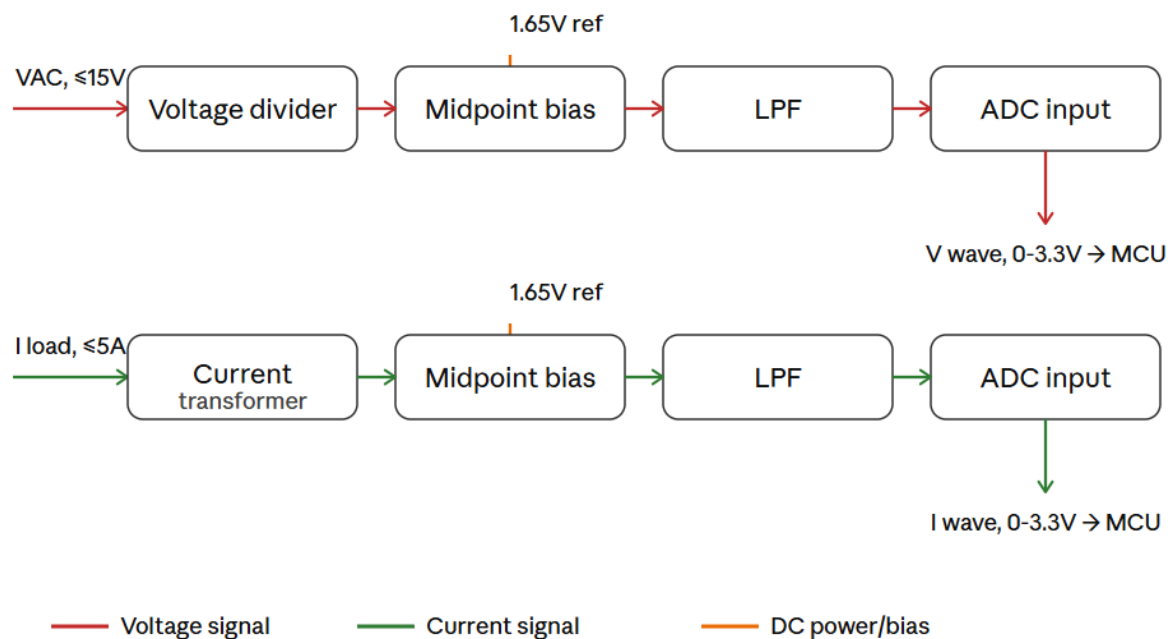


Figure 3: Sensing System Block Diagram

Requirements:

1. Safe Signal Outputs:

The subsystem will scale and bias the input voltage and current signals so that all of the outputs remain within the ADC input range of 0-3.3 V at all times. Signals going into the microcontroller should not exceed these limits.

2. Waveform and Phase Preservation:

The subsystem will preserve the shape and phase relationship of the voltage and current waveforms with minimal distortion. The total phase error from sensing inconsistencies should be <2%, ensuring accurate power factor calculation.

3. Measurement Ranges:

The subsystem will support measurement of:

- AC voltage up to 15 V RMS (≈ 21.2 V peak)
- AC current up to 5 A RMS

The output signals will target 1 V peak amplitudes that are centered at mid-supply to maximize measurement resolution.

4. Bias Stability:

The subsystem will operate with a stable bias voltage of $1.65 \text{ V} \pm 0.05 \text{ V}$, provided by the DC Power Supply subsystem.

5. Sampling Compatibility:

The subsystem output will support reliable ADC sampling at rates between 5-10 kHz, with enough bandwidth to capture the 60 Hz fundamental and relevant harmonics up to at least 1 kHz.

DC Power Supply Subsystem:

Overview:

The DC power supply subsystem converts the 15 V AC input into regulated DC voltages used to power the microcontroller and supporting electronics, while also generating a stable reference voltage for signal biasing in the sensing subsystem. This subsystem interfaces with all other subsystems by supplying the primary power rails, a common ground reference, and the mid-supply bias voltage used for ADC signal conditioning.

The power conversion path is as follows:

AC Input $\rightarrow$ Rectifier $\rightarrow$ Filter $\rightarrow$ Voltage Regulator $\rightarrow$ Bias Generation

The AC input is first rectified to produce a pulsating DC signal, which is smoothed out using a filtering stage (bulk capacitor) to reduce ripple. The resulting DC voltage is regulated down to a stable 3.3 V supply for the microcontroller and associated circuitry. A mid-supply reference voltage of $\sim 1.65 \text{ V}$ is taken from the regulated rail and used by the sensing subsystem to bias AC signals into the ADC input range.

The key design considerations for this subsystem include maintaining voltage regulation accuracy, minimizing ripple and noise, sufficient current delivery, and providing a stable ground reference. Bias voltage stability is especially important, since fluctuations directly impact measurement accuracy in the sensing subsystem.

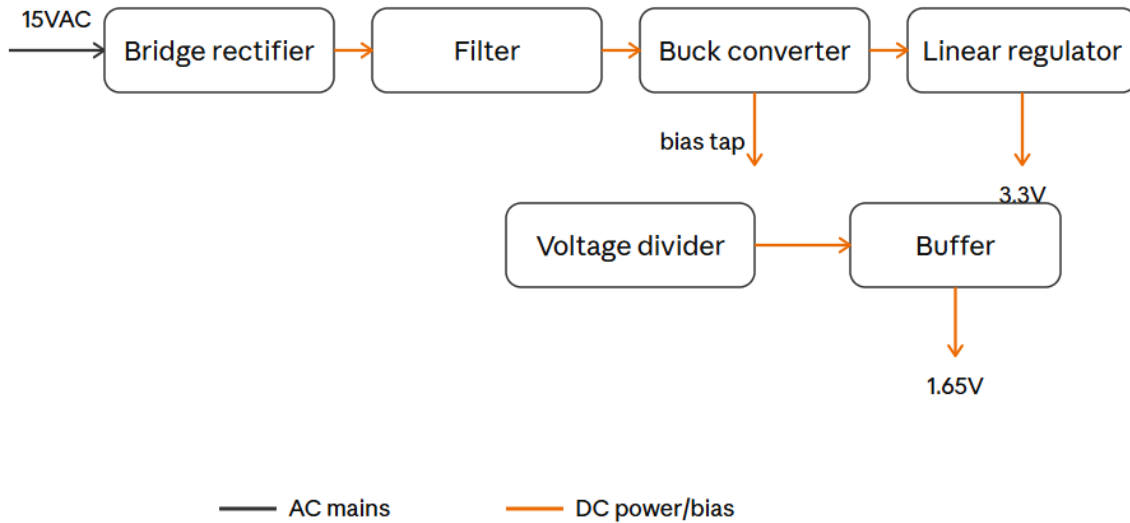


Figure 4: DC Power Supply Block Diagram

Requirements:

1. AC-to-DC Power Conversion:

The subsystem will convert a 15 V AC 60 Hz input into a DC voltage for regulation. The rectification and filtering stages will produce a DC output with enough smoothing to support stable regulation.

2. Stable Voltage Regulation:

The subsystem will provide a regulated 3.3 V supply within ± 0.05 V to power the microcontroller and other circuits when powered.

3. Current Supply Capability:

The subsystem will be able to supply at least 300 mA of continuous current to support the MCU, sensing circuits, and switching components.

4. Stable Bias Reference:

The subsystem will generate a mid-supply reference voltage of $1.65 \text{ V} \pm 0.02 \text{ V}$ for signal biasing. This reference must remain stable under varying load and noise conditions.

5. Common Ground Reference:

The subsystem will provide a stable and low-impedance common ground reference shared across the microcontroller, sensing subsystem, and switching control circuits.

6. Low Noise Operation:

The power supply will have an output voltage ripple of <50 mV peak-to-peak to prevent inaccurate ADC measurements. The bias reference will have minimal noise to avoid error in the sensed waveforms.

Microcontroller Subsystem:

Overview

The microcontroller subsystem is the computational core of the adaptive power factor correction system. It samples the conditioned voltage and current signals from the sensing subsystem, computes real-time power factor, and determines the reactive power compensation needed to bring the system into the target operating window.

MCU Selection: The subsystem will use a microcontroller for three key features: (1) dual, hardware-synchronizable ADC channels, allowing simultaneous sampling of voltage and current so that phase information is preserved; (2) a hardware timer capable of triggering ADC conversions at a fixed rate without CPU intervention, ensuring consistent sample spacing; and (3) an onboard hardware floating-point unit (FPU), which allows the RMS, power, and power factor calculations to be performed efficiently in real time.

A hardware timer is configured to trigger simultaneous ADC conversions on the voltage and current channels at 5–10 kHz. Samples are transferred via DMA (Direct Memory Access) directly into memory buffers, avoiding CPU-induced timing jitter that would otherwise distort the phase relationship between the two signals. Each buffer captures multiple full AC cycles to support averaged, cycle-aligned calculations.

Because the sensing subsystem biases both waveforms to sit within the ADC's input range, the MCU first removes this DC offset from each sample to recover the original zero-centered waveform, then scales the result using the known voltage-divider and current-transformer ratios to obtain true voltage and current values.

Power and Power Factor Calculation

Using the reconstructed waveforms, the MCU computes the root-mean-square (RMS) voltage and current:

$$V_{rms} = \sqrt{[1/N] \sum v(t)^2} \quad (1)$$

$$I_{rms} = \sqrt{[1/N] \sum i(t)^2} \quad (2)$$

The apparent power is calculated as:

$$S = V_{rms} \times I_{rms} \quad (3)$$

Real power is calculated by averaging the instantaneous power over an integer number of AC cycles:

$$P = (1/N) \sum v(t_n) \times i(t_n) \quad (4)$$

The power factor is calculated as:

$$PF = P/S \quad (5)$$

For the predominantly inductive, sinusoidal load, reactive power is calculated as:

$$Q = \sqrt{S^2 - P^2} \quad (6)$$

Where:

V_{rms} = RMS voltage (V)

I_{rms} = RMS current (A)

$v(t_n)$ = instantaneous voltage at sample n (V)

$i(t_n)$ = instantaneous current at sample n (A)

N = number of samples over an integer number of AC cycles

P = real power (W)

S = apparent power (VA)

PF = power factor (dimensionless)

Q = reactive power (VAR)

The conditioned voltage signal is passed through a comparator circuit that produces a clean digital pulse at each zero crossing. This pulse is routed to an MCU General Purpose Input Output (GPIO) pin configured as an external interrupt (EXTI). On each interrupt, the MCU timestamps the crossing using a free-running hardware timer. This timing information serves two purposes: aligning the RMS/power calculation window to whole AC cycles, and synchronizing capacitor-switching commands to the switching subsystem.

Approximately every 10 seconds, the MCU compares the current power factor against the value at the last compensation update. If the difference exceeds a defined threshold (~ 0.04), the MCU calculates the additional reactive power compensation required to bring the system PF into the target window (0.93–0.97), then selects the combination of discrete, binary-weighted capacitor stages (1x, 2x, 4x, 8x...) that best approximates the required capacitance. This threshold-gated, periodic evaluation prevents unnecessary switching from measurement noise or momentary load fluctuations.

Once a capacitor stage combination is selected, the MCU sets the corresponding GPIO outputs to command the switching subsystem. GPIO transitions are timed to occur at the next detected zero-crossing (rather than immediately) to minimize inrush current and switching transients in the downstream TRIAC-based switching stage.

The MCU will output live measurements (PF, P, Q, S, and active capacitor stages) via UART to a connected display or terminal, supporting the project's requirement that power factor correction be visibly verifiable during the demo.

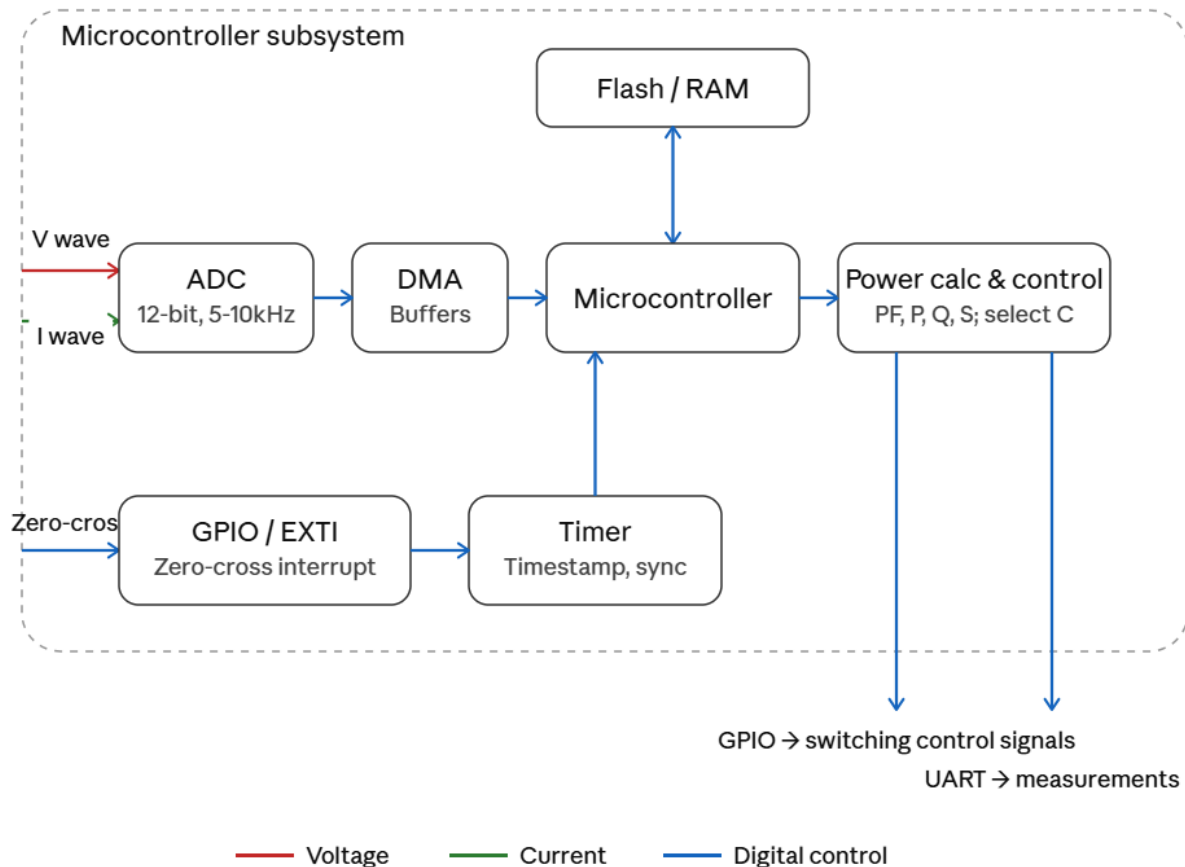


Figure 5: Switching System Block Diagram

Requirements

1. **Synchronized Real-Time Sampling:** The MCU shall sample the conditioned voltage and current signals simultaneously (or with negligible relative delay) at a rate of at least 5 kHz using timer-triggered, DMA-based ADC acquisition, to preserve the phase relationship between the two signals.
2. **Accurate Power Computation:** The MCU shall compute RMS voltage, RMS current, real power, apparent power, and power factor from the sampled waveforms with an accuracy within $\pm 2\%$ of a reference measurement device, evaluated over an integer number of AC cycles.
3. **Zero-Cross Detection and Synchronization:** The MCU shall detect AC zero-crossings via an external interrupt driven by a comparator circuit and shall use this timing reference to align power calculations to full AC cycles and to time capacitor-switching commands.
4. **Threshold-Based Switching Control:** The MCU shall re-evaluate power factor at approximately 10-second intervals and shall command a change in capacitor configuration only when the measured PF deviates from the previously commanded value by more than a defined threshold (~ 0.04), to prevent excessive or unstable switching.
5. **Capacitance Selection:** The MCU shall correctly calculate the reactive power compensation required to bring the system power factor into the target window of 0.93–0.97 and select the appropriate combination of discrete capacitor stages to achieve this, given the available binary-weighted capacitor bank.
6. **Switching Command Output:** The MCU shall output GPIO signals to the capacitive switching subsystem to enable or disable individual capacitor stages, with transitions timed to the nearest zero-crossing to minimize inrush current.
7. **Status Reporting:** The MCU shall output live system measurements (power factor, real/apparent/reactive power, and active capacitor stage configuration) via a serial or display interface for verification during testing and demonstration.

Switching Subsystem:

Overview:

The capacitive switching subsystem dynamically connects and disconnects capacitor stages in parallel with the load to provide reactive power compensation and improve the system power factor. The subsystem receives GPIO control signals from the microcontroller and translates them into isolated switching commands for the AC-side power electronics.

The proposed switching path for each capacitor stage is:

GPIO Output → Opto-Isolated Gate Driver → Power TRIAC → Inrush-Limiting Resistor → Capacitor Stage

The optocoupler-based gate driver provides electrical isolation between the low-voltage microcontroller and the AC switching circuitry while supplying the gate-trigger signal required by the power TRIAC. The TRIAC functions as the primary solid-state AC switch used to connect or disconnect each capacitor stage from the load.

Two primary design considerations for this subsystem are switching synchronization and capacitor inrush current. Switching commands will be coordinated with zero-cross information provided by the sensing subsystem so that capacitor stages can be connected at controlled points in the AC waveform. An inrush-limiting resistor will initially be placed in series with each capacitor stage to reduce transient current during connection.

A potential secondary switching path may be used to bypass the inrush-limiting resistor after the capacitor has been safely energized. This would allow the capacitor to operate with minimal added series resistance during normal power factor correction. The necessity of this bypass circuit and its timing will be determined through circuit analysis, simulation, and prototype testing.

A bleeder resistor will be connected in parallel with each capacitor stage to provide a controlled discharge path after the capacitor is disconnected. The bleeder resistance will be selected to provide an acceptable discharge time while drawing sufficiently low real power so that its effect on the overall power factor correction is minimal.

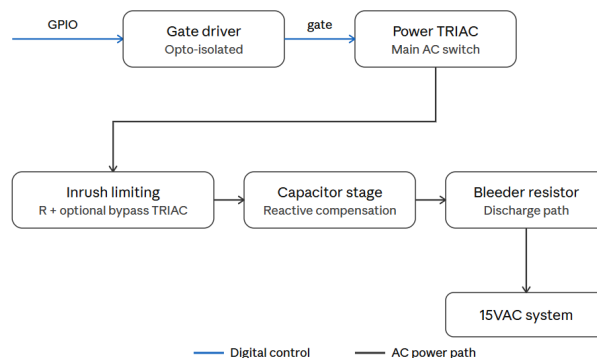


Figure 6: Switching System Block Diagram

Requirements:

1. **Safe Dynamic Capacitor Switching:**

The subsystem shall safely connect and disconnect capacitor stages while the AC system is energized. Switching shall be coordinated with the AC waveform, capacitor inrush current shall be limited during connection, and disconnected capacitors shall be provided with a controlled discharge path.

2. **Power Factor Correction Capability:**

The capacitor bank shall provide sufficient capacitance range and resolution to allow the controller to correct the system power factor into a target operating window of 0.93 to 0.97 for loads within the designed operating range.

3. **Multiple Compensation Levels:**

The subsystem shall contain multiple independently switchable capacitor stages so that different combinations of capacitance can be selected to provide multiple discrete levels of reactive power compensation.

Tolerance Analysis:

Sensing Subsystem - Bias Error:

An important tolerance that would lead to error is not having the correct bias voltage. If the intended bias of 1.65 V deviates by 50 mV, this represents a 5% offset relative to a ~1 V peak signal. This introduces a DC offset in the reconstructed waveform after sampling, which affects the real power calculation and by extension, the power factor calculation. To mitigate this, the system will calculate the average of sampled values in software and then remove the bias. This way, bias-related errors will be significantly reduced.

DC Power Supply Subsystem - Rectifier Ripple and Filtering:

One thing to look out for in the power supply is the ripple introduced by the AC-to-DC conversion stage, which must be reduced to avoid affecting the downstream regulation. For a 15 V_{RMS} input assuming a full-wave rectifier and a load current of 0.3 A, the ripple voltage is approximately 2.5 V with a 1000 microfarad capacitor. This level of ripple is too large for direct use, but it is reduced by the voltage regulation stage (buck converter and/or LDO), which provides a stable 3.3 V output. Increasing the bulk capacitance or using additional filtering further reduces ripple, which would allow for proper regulator operation.

TRIAC Inrush Current at Capacitor Switch:

Inrush current is a factor that needs to be analyzed for tolerance in the switching subsystem, since an uncharged capacitor looks like a near short circuit at the instant a TRIAC connects it to the AC line, and excessive peak current could damage the TRIAC or the capacitor. Using a 100 microfarad capacitor stage, a 10 ohm inrush-limiting resistor, and a 15 V RMS (about 21.2 V peak) source, the resulting peak inrush current comes out to about 2.1 A, decaying within roughly 1 millisecond, well inside the 8.33 millisecond AC half-cycle. A standard low-power TRIAC typically has a one-cycle surge current rating of 10 to 15 A, giving plenty of margin over this peak. This shows that with reasonable component values, the inrush-limiting approach easily meets tolerance, and the same analysis will be re-run with the actual sized values once the capacitor bank is finalized during design and testing.

MCU Timing and Sampling:

Accurate power factor calculations require synchronized voltage and current sampling. At a 5 kHz sampling rate, the sampling interval is 200 μ s. For a 60 Hz AC source, a 10 μ s timing mismatch introduces a phase error of approximately 0.216°, resulting in a power factor error of approximately 0.0012 at PF = 0.95. Hardware-timed sampling and direct memory access (DMA) will minimize timing errors. Synchronization will be verified using an oscilloscope, and power factor accuracy will be checked against a reference measurement device to meet the $\pm 2\%$ requirement.

Ethics, Safety, and Societal Impact

Ethics

The primary ethical consideration for this project is ensuring that the 15 V AC prototype operates safely and that its capabilities are represented accurately, both to instructors during evaluation and to any future audience of the design. This aligns with the IEEE Code of Ethics commitment "to hold paramount the safety, health, and welfare of the public" and "to be honest and realistic in stating claims or estimates based on available data" [2]. In practice, this means the design incorporates isolation, controlled capacitor switching, inrush limiting, and capacitor discharge protection to reduce risk to users, technicians and equipment, and the team will clearly distinguish between the demonstrated 15 V AC system and the broader concept of scaling the same architecture to higher-voltage, 480 V commercial applications. Any commercial implementation would require additional component ratings, protection, and regulatory compliance appropriate to the higher operating voltage, and the team will avoid overstating the prototype's readiness for such deployment.

Safety

Although the 15 V AC laboratory prototype falls outside the practical scope of most NEC installation requirements, the design is intended as a scalable proof of concept, so relevant requirements of NEC Article 460, which addresses capacitor installations used for applications such as power factor correction, are considered in the design [1].

- NEC 460.3 — Enclosing and Guarding: Capacitor terminals and other energized components must be protected from accidental contact. This design addresses that requirement through physical separation of the MCU and AC circuitry, optical isolation between the microcontroller and switching hardware, and protection of energized components during operation [1].
- NEC 460.6 — Discharge of Stored Energy: Capacitors must have a means of automatically discharging stored energy after being disconnected. This design uses a bleeder resistor across each capacitor stage to provide this discharge path [1].

Societal Impact

As electrical power demand continues to increase, improving the efficiency and utilization of existing electrical infrastructure becomes increasingly important. Power factor correction reduces unnecessary reactive current, which can lower system losses and free capacity in conductors, transformers, and other distribution equipment. An automated power-factor-correction system can therefore help facilities use electrical infrastructure more efficiently while supporting reliable grid operation as demand grows, with broader economic and environmental benefits from reduced generation and transmission losses.

References

[1] National Fire Protection Association, *NFPA 70: National Electrical Code*, Quincy, MA: National Fire Protection Association, 2023.

[2] IEEE, "IEEE Code of Ethics." Available:
<https://www.ieee.org/about/corporate/governance/p7-8.html>