SINGLE-PHASE AC POWER ANALYZER DESIGN DOCUMENT

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Contents

1. Introduction

1.1 Problem

Basic voltage and current measurements do not provide insight into how power is being consumed by an AC load. Relevant quantities such as real power and power factor require time-synchronized measurements of voltage and current, which are typically only available from commercial power analyzers. These commercial analyzers are expensive and unnecessary for small-scale laboratory or educational purposes.

1.2 Solution

Design and build a microcontroller-based, single-phase AC power analyzer that measures voltage and current supplied to a load using isolated sensing circuits. The microcontroller will sample both signals at the same time and compute RMS values, real power, and power factor in real time. Measurement data will be transmitted to a computer over USB for display and analysis. Example use cases include comparing real power and power factor across common loads (incandescent lamp vs. fan motor vs phone charger), observing changes in RMS voltage, current, and power during load startup, and identifying inefficient or abnormal load behavior in educational lab experiments. It provides students with hands-on exposure to AC power measurements without needing expensive commercial equipment. The final system will provide a low-cost, embedded tool for monitoring and analyzing AC power behavior in laboratory and educational environments.

1.3 Visual Aid

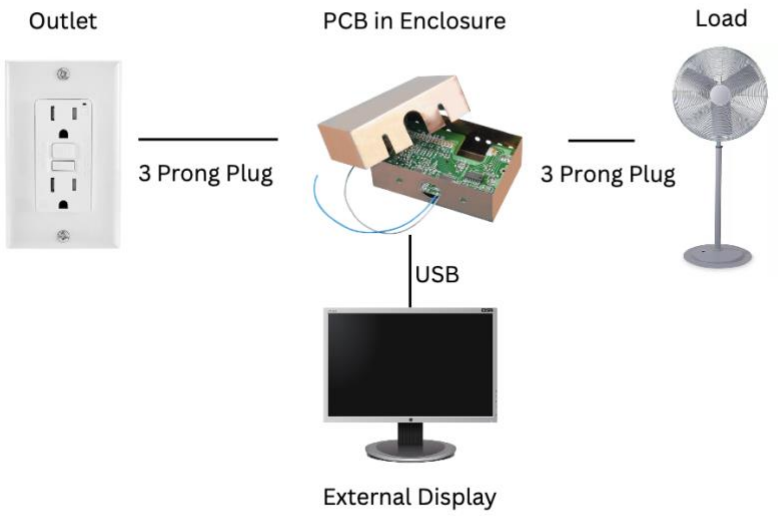


Figure 1 Pictorial representation of project

1.4 High Level Requirements

1.4.1 Measurement Accuracy

The analyzer shall measure RMS voltage, RMS current, real power, and power factor of a single-phase 120 VAC load with accuracy within ±5% for RMS voltage, ±10% for RMS current, ±10% for real power, and ±0.10 for power factor when compared against a calibrated commercial power analyzer for steady state loads up to 5 A RMS.

1.4.2 Time-Synchronized Sampling

The analyzer shall acquire voltage and current measurements using time-synchronized sampling at a minimum sampling rate of 3kHz, such that computed values of real power and power factor remain within the accuracy limits specified above.

1.4.3 Real-Time Reporting

The analyzer shall compute and transmit RMS voltage, RMS current, power (P), and power factor (PF) to a host computer at a minimum update rate of 5 Hz, where values are displayed to the user in real time.

2. Design

2.1 Block Diagram

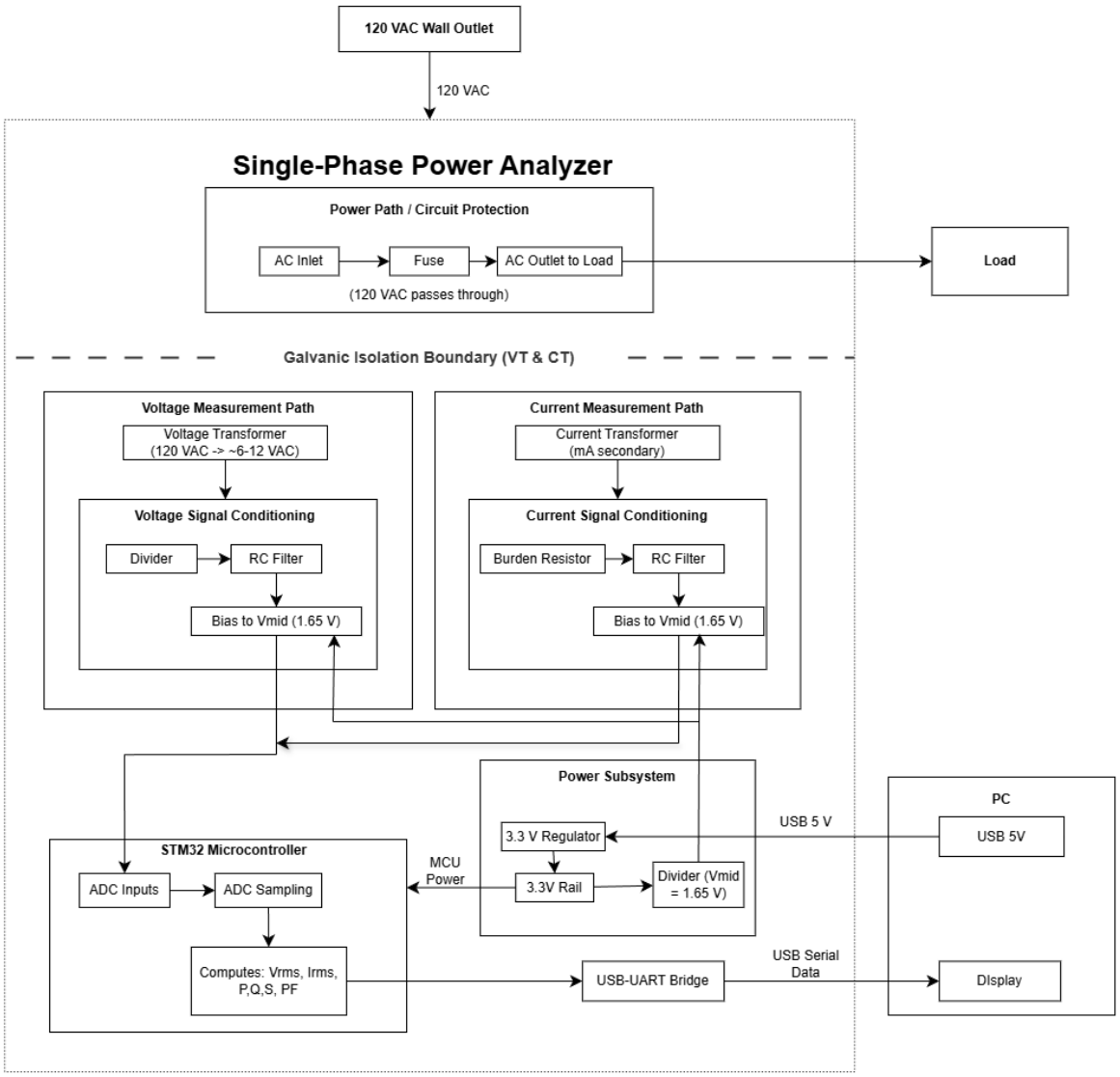


Figure 2 Block Diagram with each subsystem

2.2 Power Path / Circuit Protection Subsystem

The power path subsystem design ensures a secure connection between the AC inlet and the load. It will also maintain electrical isolation of high and low voltage. In case of a load short circuit or internal wiring failure, we will place a series fuse on the hot line to prevent overcurrent conditions. This fuse will be placed inside of the AC inlet receptacle. Since our PQA is designed for a max of 5A RMS we will use a 6.3A slow blow fuse. It's important to use a slow blow fuse with a slightly higher current rating in case a

load has a high start up current. For the AC inlet we will use an IEC 320 C14 receptacle with a built-in fuse on the line. For the load outlet we will use the standard NEMA 5-15R outlet. We will use screw terminals and quick connects for the connections. The enclosure for the entire design will be 3D printed to ensure compatibility with our design and safety concerns. The ground will be unified throughout the entire design.

2.2.1 Power Path / Circuit Protection Subsystem Requirements

The power path/circuit protection subsystem shall satisfy the following requirements:

- Secure connection between the load and inlet.
- Maintain electrical and physical isolation of high and low voltage.
- Provide protection in case of a fault in the design or the load.

Requirements	Verification Method	Verification
Secure connection between the load and inlet.	Use a DMM to ensure continuity from the outlet to inlet for line, neutral, and ground.	Secure connection
Maintain electrical and physical isolation of high and low voltage.	Visually check that there is physical connection and measure low voltage side with a DMM.	Separation of voltages
Provide protection in case of a fault in the design or the load.	Load our fuse with 150% rated current.	See if fuse blows as intended.

Failure to meet these requirements would result in safety hazards and no power flow.

2.3 Voltage Measurement Subsystem

The voltage measurement subsystem is responsible for taking accurate, isolated voltage readings from the line to neutral. To do this, we need to use a step-down transformer to convert the high voltage to low voltage. We will need to consider accuracy tolerances and rating of our transformer to ensure accurate RMS voltage readings. This transformer will be a PCB mounted transformer, so we will have to ensure that there is enough creepage between the high voltage side and the low voltage side on the PCB. To further ensure separation, we will have the transformer on a separate PCB than the low voltage side. We will use 2 terminal screw blocks to connect the secondary terminals to the other PCB.

2.3.1 Voltage Measurement Subsystem

The voltage measurement subsystem shall satisfy the following requirements:

- Isolate high voltage from low voltage.
- Does not affect the load input.
- Accurately describes input RMS voltage.
- Steps voltage down from 120VAC to 6-12VAC, 6VA.
- Transformer creepage of at least 5mm on PCB.

Requirements	Verification Method	Verification
Isolate high voltage from low voltage.	Measure voltage on the secondary side of the transformer using a DMM.	Ensure voltage separation
Does not affect the load input.	We will measure the input current of the transformer using a DMM.	Draws no more than 1% of load current
Accurately describes load RMS voltage.	Measure the load voltage with a known and accurate DMM.	Compare with our values and ensure its within 10% margin.
Steps voltage down from 120VAC to 6-12VAC, 6VA.	Input 120VAC on the primary and measure the secondary using a DMM.	See if 8VAC is on secondary side
Transformer creepage of at least 5mm on PCB.	We will design this into our board and measure it with a micrometer once it is received.	Ensure creepage

2.4 Current Measurement Subsystem

The current measurement subsystem is responsible for taking accurate, isolated current readings from the line. We will do this by using an isolated current transformer and a burden resistor to turn the current into a readable voltage waveform. We will need to consider how the tolerance of the resistor and CT affects our RMS current readings. The current transformer will be a solid core with a turn ratio of 500:1 and a maximum current rating of 5A. The wire leads from the CT will go into a screw two terminal block on the PCB.

2.4.1 Current Measurement Subsystem Requirements

The current measurement subsystem shall satisfy the following requirements:

- Make isolated current measurements.
- Does not affect the load input.
- Accurately describes input RMS current.

- 5A to 5mA Current Transformer.
- Current from CT is turned into a voltage waveform.
- Burden resistor tolerance

Requirements	Verification Method	Verification
Make isolated current measurements that does not affect the load input.	Measure the current before and after the CT using a known CT probe.	Ensure minimal current drop
Accurately describes load RMS current.	We will reference our values with values from a known and accurate CT probe.	Accurate RMS current readings
500:1 5A:1V Current Transformer.	Measure the voltage across the burden resistor.	Ensure our expected voltage of 0-1V
Burden resistor tolerance $\pm$1%.	We will compare the actual resistance with the ideal resistance using a DMM.	Burden resistor tolerance of $\pm$1%

2.5 Analog Signal Conditioning Subsystem

The analog signal conditioning subsystem scales, filters, protects, and level-shifts the voltage and current sensing signals to meet the input requirements of the 0–3.3 V ADC while maintaining waveform integrity for accurate RMS current/voltage, real power, and power factor calculations.

For the voltage conditioning, we will be using the transformers secondary as an input to a voltage divider, into a series capacitor, into a DC bias circuit, into an RC low-pass filter, then finally outputs to the ADC input. In Figure 2.5.1 below we see the voltage sensing circuit with the previously listed components. The voltage source is made to simulate the maximum rated voltage of 8V RMS at 60Hz for simulation purposes.

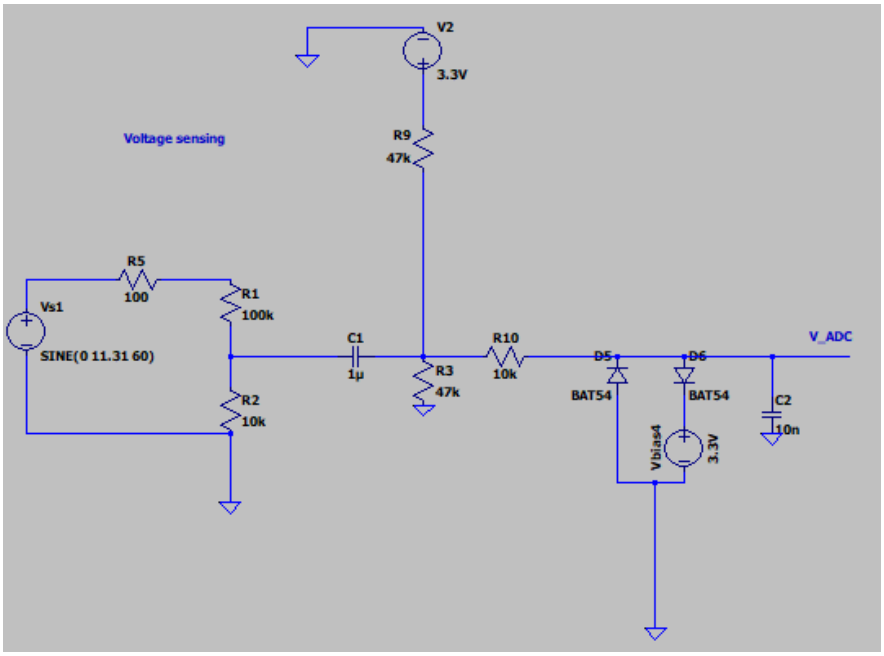


Figure 2.5.1 LTspice Schematic of voltage sensing circuit for simulation.

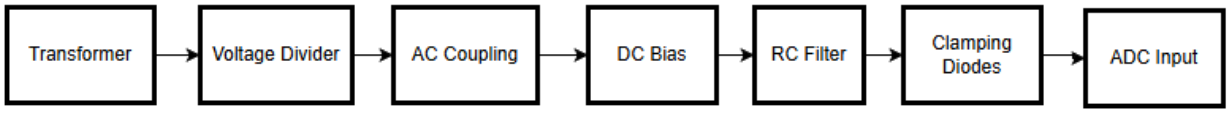


Figure 2.5.2 Block diagram for voltage sensing circuit.

Transformer: Steps down voltage from 120VAC to 8VAC. Isolated from the load.

Voltage Divider: Sets peak signal near 70-80% of ADC range, 1% tolerant resistors for accuracy, high resistance values (100k) to reduce the loading of the transformer and minimize power loss.

AC Coupling (Series Capacitor): Removes any DC component before applying Vmid bias. The cut-off frequency must be well below 60Hz to avoid phase shift.

DC Bias: Centers signal at 1.65V for ADC 0-3.3V range.

RC Filter: Prevents high-frequency switching noise from corrupting measurements.

Clamping Diodes: Protects the ADC input from transient overvoltage.

For the current conditioning, we will be using the CT + burden resistor as an input to a series capacitor, into DC bias circuit, into a clamp diode protection circuit, into an RC filter, then finally outputs to the ADC input. In Figure 2.5.3 below we see the current sensing circuit with the previously listed components. The current source is made to simulate the maximum rated current of 10mA at 60Hz for simulation purposes.

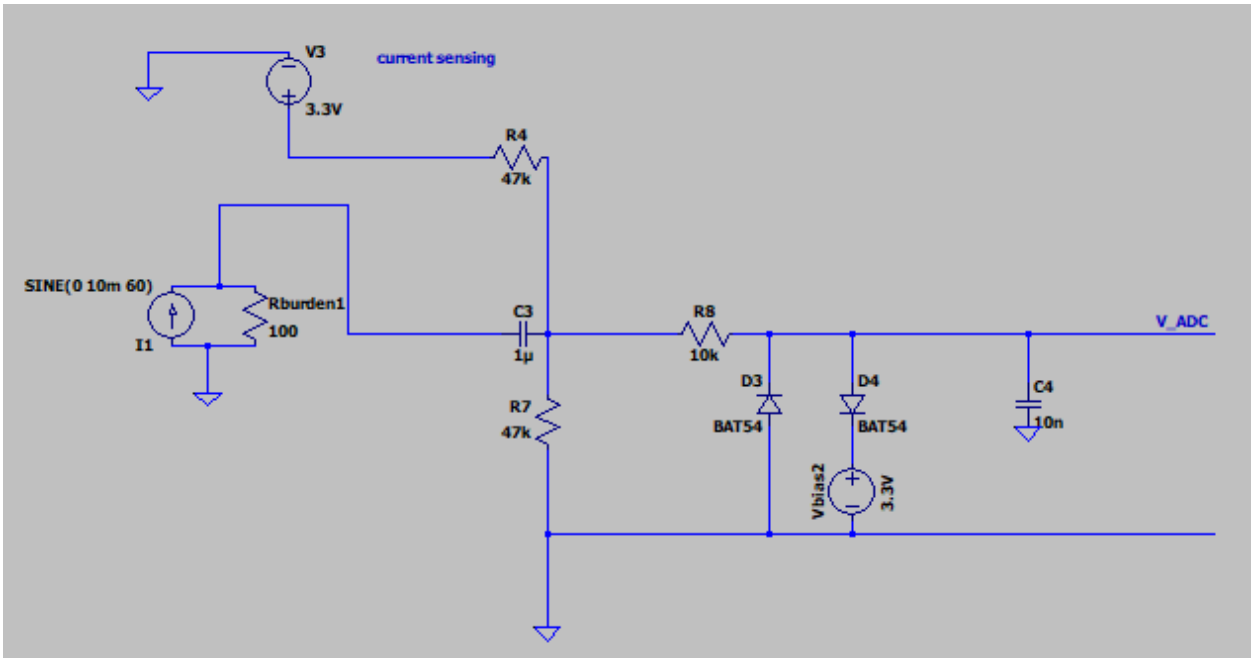


Figure 2.5.4 LTspice Schematic of current sensing circuit for simulation.

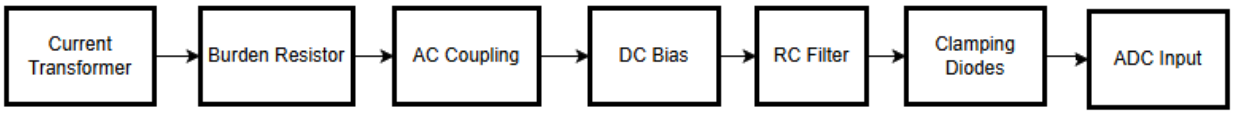
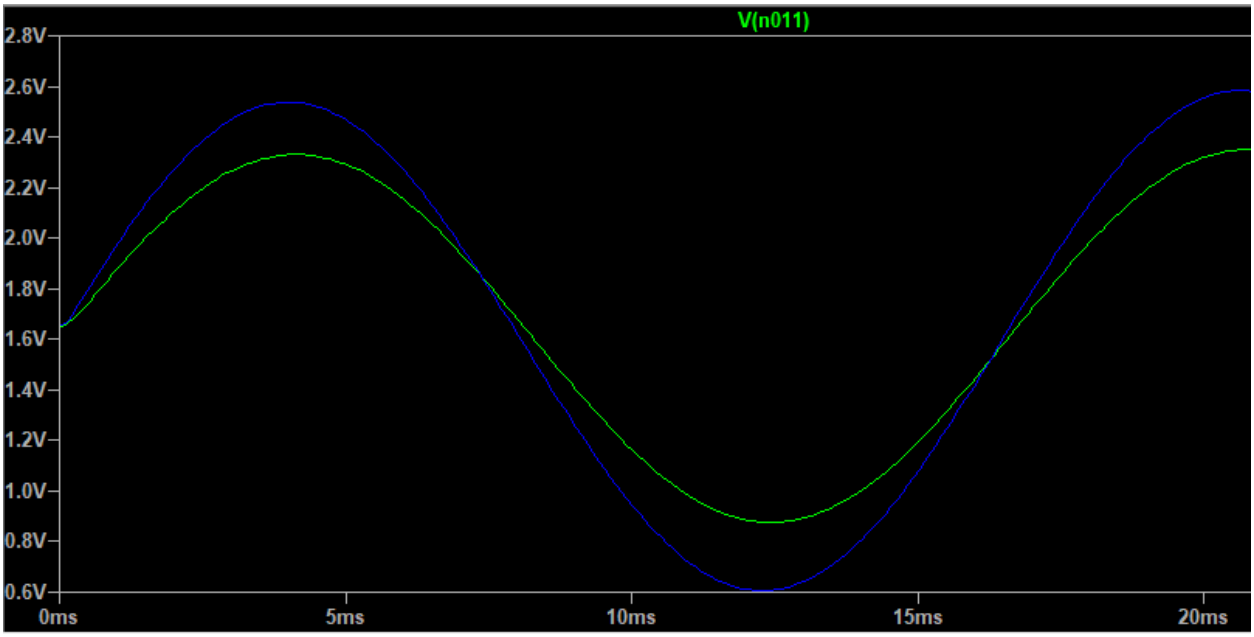


Figure 2.5.5 Block diagram for current sensing circuit.

Current Transformer: Takes isolated voltage measurement and outputs a small second current of at most 10mA.

Burden Resistor: This turns the secondary current into a voltage to be read by the ADC. For the max 10mA current, we will see 1V giving us the desired 0-1V swing to be conditioned into the 70-80% of 0-3.3V, centered at 1.65V.

Analyzing the waveform from LTspice, the voltage(Green) and current(blue) sensing circuits we see that they are within our desired 80-90% of 0-3.3V swing, centered at 1.65V, and have a relative phase shift of 0.57 degrees. We assume that this will be different in practice since LTspice is an ideal circuit but we are well within range of our requirements.



2.5.1 Analog Signal Conditioning Subsystem Requirements

The analog signal conditioning subsystem shall satisfy the following requirements:

- Both outputs referenced at Vmid = 1.65 V.
- Minimize relative phase shift between voltage and current channels.
- Use 70-80% of the ADC range(0-3.3V) to prevent clipping.
- Limit bandwidth using low-pass filters to prevent aliasing during sampling.
- Provide input protection using series resistance and clamping diodes to prevent overvoltage at the ADC inputs.

Requirements	Verification Method	Verification
Both outputs referenced at Vmid = 1.65 V. Minimize relative phase shift between voltage and current signals. Use 70-80% of the ADC range(0-3.3V) to prevent clipping. Limit bandwidth using low-pass filters to prevent aliasing during sampling.	Oscilloscope measurements on the output of the sensing circuits.	Vmid=1.65, minimal phase shift, no clipping, limited bandwidth
Provide input protection using series resistance and clamping diodes to prevent overvoltage at the ADC inputs.		

2.6 Embedded Processing Subsystem

The Embedded Processing Subsystem is responsible for acquiring time-synchronized voltage and current measurements and computing electrical quantities in real time. This subsystem will be implemented using an STM32F303 microcontroller operating from a regulated 3.3 V supply.

This subsystem receives two analog input signals from the Voltage and Current Signal Conditioning subsystems. These signals are scaled and biased to fall within the 0-3.3 V ADC input range and are centered around a reference voltage (Vmid = 1.65 V). The microcontroller samples both channels using timer-triggered dual ADC hardware to ensure consistent sampling intervals.

Time-synchronized sampling is achieved using timer-triggered dual ADC operation. A hardware timer generates periodic trigger events that initiate conversions on both ADC channels simultaneously, ensuring deterministic sampling intervals and limiting channel-to-channel skew.

The system samples both channels at approximately 6 kHz, providing 100 samples per cycle of the 60 Hz waveform. This sampling rate reduces numerical integration error and provides sufficient bandwidth margin relative to the analog anti-alias filtering.

ADC conversions are transferred into memory via DMA using fixed length buffers corresponding to multiple waveform cycles. DMA eliminates sampling jitter and allows signal processing to occur without interfering with data acquisition.

Prior to computation, the firmware removes DC bias by subtracting the measured mean of each buffer, accounting for the Vmid bias and preventing calculation errors.

Samples are collected over a fixed-duration window corresponding to multiple cycles of the 60 Hz waveform. For each window, the firmware computes RMS voltage (Vrms), RMS current (Irms), real power (P), and power factor (PF). Calibration constants are applied to convert ADC counting into physical voltage and current units.

Computed values are passed to the Communication Subsystem for transmission to the host PC.

2.6.1 Embedded Processing Subsystem Requirements

The Embedded Processing Subsystem shall satisfy the following quantitative requirements:

- The subsystem shall sample voltage and current channels at a minimum sample rate of 3 kHz to ensure adequate resolution of 60 Hz waveforms.
- Voltage and current samples shall be acquired using time-synchronized sampling with channel-to-channel timing difference less than 10 µs.
- The ADC input range shall be limited to 0-3.3 V.
- The subsystem shall compute Vrms, Irms, P, and PF over a window of at least 5 cycles of the 60 Hz waveform.
- The subsystem shall update computed measurement values at a minimum rate of 5 Hz.

- The subsystem shall apply calibration scaling factors to convert ADC counts into physical voltage and current units.
- The subsystem shall maintain computational error contributions below the levels specified in the high-level requirements.

Failure to meet these requirements would prevent accurate power measurement and the device will fail to meet overall system objectives.

The requirements listed above are verified using the procedures summarized in the table below.

Requirements	Verification Method	Verification
Time-synchronized sampling	Apply identical sinusoidal signal to both ADC channels and compare sampled waveforms	No measurable phase offset between channels
Samling rate ≥ 3kHz	Timer configuration measurement	≥ 3kHz confirmed
ADC input within 0-3.3 V	Oscilloscope measurement of conditioned ADC signals during operation	No clipping observed
RMS and power calculation	Comparison with reference meter	Error within high-level accuracy requirements
Measurement update ≥ 5 Hz	Log PC display update timestamps	≥ 5 updates per second
Calibration scaling applied	Measure known resistive load and compare computed physical units	Correct physical units

Failure to meet these requirements would prevent accurate power measurement and the device will fail to meet overall system objectives.

2.7 Communication Subsystem

The Communication Subsystem provides real-time transmission of computed electrical measurements to a host PC. A CP2102N USB-to-UART bridge converts UART signals from the microcontroller into USB serial data that can be received by standard host PC software.

The Communication Subsystem interfaces with the Embedded Processing Subsystem via buffered measurement values and requires that computation completes prior to transmission. On the hardware side, the subsystem interfaces with the CP2102N USB-UART bridge through standard UART TX/RX lines operating at 3.3 V logic levels.

The subsystem receives computed measurement values including RMS voltage, RMS current, real power, and power factor from the Embedded Processing Subsystem and packages them into formatted serial messages. These messages are transmitted periodically over UART to the USB bridge, which presents data as a virtual COM port to the host PC.

On the host side, a software application parses through the incoming data and displays Vrms, Irms, P, and PF numerically in real time. The communication link therefore provides visibility into system measurements without affecting data acquisition or computation.

UART transmission is executed using non-blocking methods to ensure that communication does not interfere with sampling or signal processing. Measurement values are transmitted at a minimum of 5 Hz, matching the update frequency of the Embedded Processing Subsystem.

The selected UART baud rate provides sufficient bandwidth to transmit all measurement values within each update interval while maintaining margin for protocol overhead. Loss of communication does not affect data acquisition or computation, as transmission is decoupled from the sampling pipeline.

This subsystem ensures that measured quantities are presented to the user in real time, satisfying the third high-level requirement.

2.7.1 Communication Subsystem Requirements

The Communication Subsystem shall satisfy the following quantitative requirements:

- The subsystem shall transmit computed measurement values to a host computer over USB using a UART-based serial protocol.
- The data transmission rate shall be sufficient to support a minimum update frequency of 5 Hz without data loss.
- UART communication shall operate at a baud rate sufficient to transmit all required values within each update interval.
- The subsystem shall ensure that the loss of communication does not affect measurement computation within the Embedded Processing Subsystem.

Requirements	Verification Method	Verification
Transmission of computed measurements over USB	Observe serial output using terminal software on host PC	Measurement values correctly received and displayed
Data rate sufficient for ≥ 5 Hz updates	Log timestamps of received measurement packets on PC	≥ 5 updates per second observed without data loss
UART baud rate sufficient for packet transmission	Calculate required data rate and compare with configured baud rate; verify continuous transmission	No buffer overflows or dropped packets observed
Communication loss does not affect computation	Close the PC serial application (no host reads) and observe MCU heartbeat or processing indicator LED	LED continues blinking at expected update rate

Failure to meet these requirements would prevent the real-time display of measurement data and compromise system functionality.

2.8 Board Power Subsystem

The Board Power Subsystem is responsible for converting raw USB 5V power into stable voltage that is used for onboard electronics as well as providing a mid-voltage reference at 1.65V.

Utilizing a USB interface, the system draws USB 5V power directly from a connected PC. Then, the onboard regulator steps down the 5V input to a stable 3.3V which will be provided to the STM32 microcontroller to be able to run its logic operations and code.

Next, a voltage divider will be used to create a mid-rail reference at 1.65V which would be able to offset AC signals into a positive range (0V to 3.3V) that the microcontroller's Analog-to-Digital Converter (ADC) can safely process.

Requirements	Verification Method	Verification
The main power regulator must provide an output voltage of 3.3V ± 5% (3.135V to 3.465V) for a current load ranging from 0mA to 500mA.	Using a bench power supply, output 5V to the USB power input pins on the regulator. Next, place a resistor/load across the output and ground.	Multimeter confirms the output voltage remains between 3.135V and 3.465V.
The voltage divider must use high precision resistors to ensure the 1.65V offset remains consistent.	Power the board via USB. Place a multimeter across the output of the voltage divider and ground.	Steady state voltage reads around 1.65V.
There must be sufficient current to power the MCU, isolated sensing circuits, and any peripheral displays.	Connect a load across the 3.3V regulator. Use a multimeter to monitor the current draw of the load.	Load draws a continuous amount of current without any drastic fluctuations.

2.9 Tolerance Analysis

The most critical performance requirement is accurate real power and power factor measurement. These quantities depend on time-aligned sampling of voltage and current. Any sampling delay introduces phase error, which directly affects computed real power and power factor.

The Embedded Processing Subsystem requires channel-to-channel sampling skew less than 10 µs. The resulting phase error at 60 Hz is:

$$\phi_{error} = 2\pi f \triangle t = 2\pi(60)(10 \times 10^{-6}) = 0.00377\ rad\ \approx 0.216°$$

Since power factor is the cosine of phase angle, a small phase error of 0.216° (0.00377 rad) produces at most a 0.0038 change in PF. This is much smaller than the allowed ±0.10 PF error. Therefore, channel timing skew is not expected to limit PF or real power accuracy.

The system will sample at a minimum rate of 3 kHz. For a 60 Hz waveform, this gives:

$$\frac{3000}{60} = 50\ samples\ per\ cycle$$

Using at least 5 cycles per computation window yields 250 samples per update. With 50 samples per cycle and averaging over multiple cycles, the discrete summation closely approximates the continuous RMS integral. For a smooth sinusoid, the numerical error at this sampling density is well below 1%, which is well below our allowed tolerance.

The microcontroller uses a 12-bit ADC over a 0-3.3 V input range. The least significant bit (LSB) size is:

$$LSB = \frac{3.3V}{2^{12}} = \frac{3.3}{4096} = 0.806\ mV$$

The maximum quantization error is $\pm\ \frac{1}{2}\ LSB$:

$$\epsilon_q = \pm\ 0.403\ mV$$

The conditioned voltage and current waveforms are designed to have peak amplitudes on the order of 1-1.5 V. Using the conservative lower bound of 1 V peak amplitude, the worst-case relative amplitude error due to quantization is:

$$\frac{0.000403}{1.0} = 0.000403 = 0.040\%$$

For a 1.5 V peak amplitude:

$$\frac{0.000403}{1.5} = 0.0000269 = 0.027\%$$

Thus, quantization contributes less than 0.05% relative error in amplitude, which is negligible compared to the required voltage and current accuracy specifications. Quantization error is therefore not expected to limit measurement performance.

Therefore, overall measurement accuracy is expected to be limited primarily by analog sensing tolerances (VT ratio error, CT ratio error, and resistor tolerances), rather than by embedded computation.

3. Cost and Schedule

3.1. Bill of Materials

Description:	Manufacturer Part #:	Manufacturer:	Quantity:	Price per unit:	Link:
6VA 115/8V PCB Mounted Transformer	FP16-375	TRIAD Magnetics	1	$12.06	link
5 A 500:1 Current Sense Transformer 50/60Hz Through Hole	CT-06-50	KEMET	1	$7.99	link
1 µF Film Capacitor 40V 63V Polyester, Polyethylene Terephthalate (PET), Metallized - Stacked Radial	B32529C0105J000	EPCOS - TDK Electronics	2	$0.58	link
10000 pF Film Capacitor 400V 630V Polypropylene (PP), Metallized - Stacked Radial	B32621A6103J000	EPCOS - TDK Electronics	2	$0.63	link
100 kOhms ±1% 0.25W, 1/4W Through Hole Resistor Axial Metal Film	MFR-25FRF52-100K	YAGEO	5	$0.10	link
10 kOhms ±1% 0.25W, 1/4W Through Hole Resistor Axial Metal Film	MFR-25FRF52-10K	YAGEO	3	$0.10	link
100 Ohms ±1% 0.25W, 1/4W Through Hole Resistor Axial Metal Film	MFR-25FRF52-100R	YAGEO	2	$0.10	link
47 kOhms ±5% 0.25W, 1/4W Through Hole Resistor Axial Automotive AEC-Q200 Carbon Film	CFR-25JR-52-47K	YAGEO	4	$0.10	link
DIODE ARR SCHOTT 30V 200MA SOT23	BAT5404E6327HTSA1	Infineon Technologies	2	$0.28	link
NEMA 5-15 Plug x IEC C13 Socket, 18 Wire Gauge, 3' Long, SVT	71535K41	McMaster-Carr	1	$5.91	link
FUSE CERAMIC 6.3A 250VAC 5X20MM	5HT 6.3-R	Bel Fuse Inc.	3	$0.44	link
PWR ENT MOD RCPT IEC320-C14 PNL	6200.23	SCHURTER Inc.	1	$4.44	link
Power Connector Receptacle, Female Sockets NEMA 5-15R Panel Mount, Snap-In	738W-X2/03	Qualtek	1	$1.30	link

2 Position Wire to Board Terminal Block Horizontal with Board 0.197" (5.00mm) Through Hole	691137710002	Würth Elektronik	4	$0.37	link
ARM® Cortex®-M4 STM32F3 Microcontroller IC 32-Bit 72MHz 512KB (512K x 8) FLASH 64-LQFP (10x10)	STM32F303RET6	STMicroelectronics	4	$9.84	link
IC USB TO UART BRIDGE QFN24	CP2102N-A02-GQFN24	Silicon Labs	5	$4.14	link
USB - micro B USB 2.0 Receptacle Connector 5 Position Surface Mount, Right Angle; Through Hole	1050170001	Molex	3	$0.92	link
Connector Header Through Hole 6 position 0.100" (2.54mm)	10129378-906001BLF	Amphenol ICC (FCI)	2	$0.14	link
22 Ohms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	RC0603FR-0722RL	YAGEO	4	$0.10	link
17V Clamp 5A (8/20µs) Ipp Tvs Diode Surface Mount SOT-666	USBLC6-2P6	STMicroelectronics	3	$0.44	link
Linear Voltage Regulator IC Positive Fixed 1 Output 600mA SOT-25	AP2112K-3.3TRG1	Diodes Incorporated	4	$0.22	link

3.2. Cost of Labor

In addition to parts, we must account for cost of labor. The starting salary for a UIUC Electrical Engineering graduate is about $90k or $43 an hour. We work an average of 10 hours a week for about 14 weeks.

Total cost of labor = $43/hr x 10hrs/week x 14 weeks x 3 persons = $18,060

This brings out total cost to:

Total cost = cost of labor + cost of parts = $18164.58

3.3. Schedule

Week	Task	Person
February 23rd – March 2nd	Order parts	Isaac/Jeffrey
	Design review sign-up/document	Everyone
	MCU pin assignments established	Isaac
	First Round PCB Orders Feb. 26th	Joseph
March 2nd – March 9th	Finalize PCB Design	Joseph

	Design review	Everyone
	Second Round PCB Orders March 5th	Joseph
	Breadboard implementation	Jeffrey
March 9th – March 16th	Breadboard demo	Jeffrey
	Teamwork Eval. 1	Everyone
	Third Round PCB Orders March 12th	
	Begin PCB assembly	
March 16th – March 23rd (Spring Break)		
March 23rd – March 30th	Final PCB Orders March 26th	Joseph
	Design/print enclosure	Jeffrey
	Finalize PCB assembly	
March 30th – April 6th	Individual Progress reports	Everyone
	Build full design	Jeffrey
April 13th – April 20th	Progress demo	Everyone
	Team contract assessment	Everyone
April 20th – May 27th	Mock demo/presentation	Everyone
	Prepare for final demo, finishing touches	Everyone
May 27th – May 4th	Final demo/presentation	Everyone
May 4th – May 11th	Final papers, lab notebook	Everyone

4. Ethics, safety and societal impact

4.1 Ethics

Regarding ethics, we will strive to adhere to the IEEE Code of Ethics [1]. Specifically for our project, it is imperative to ensure the safety of not only our group, but the users that will be using our power analyzer. We will ensure the implementation of specific safety hardware, including fuses and surge protection, to prevent catastrophic failure or fire hazards during operation, as well as disclose and warn about the high-voltage risks associated with 120V AC. Moreover, by designing a functional, low-cost tool, this project supports the IEEE goal of improving the understanding of technology, specifically by making power quality analysis more accessible for educational and laboratory environments.

4.2 Safety

Due to working with 120V AC mains provided by the wall outlet, it is essential to make sure that the high voltage portion of our project remains electrically isolated from the rest of the components and low voltage equipment such as the microcontroller. To alleviate the dangers associated with working with high voltage, we will make sure to test and simulate our ideas initially through LTSpice and calculations before physically implementing and working on them. Furthermore, to also make sure that the user is protected from touching any components or voltage, the entire system will be enclosed in a portable encasing that will prevent any possible exposure. Additionally, it is essential to make sure that this enclosure has proper soldering connections, insulation of wires, and galvanic isolation boundaries to prevent overheating, arcing from low to high voltage, and shock protection. We will make sure that each

component is UL recognized and or listed. We will ensure that each component will be within its rated specifications. Furthermore, due to working with high voltage, we will produce a safety manual which will be demonstrated at demo as well.

4.3 Societal Impact

The development of our project is to provide a low cost, but effective single phase AC power analyzer that would be able to fill the gap in both educational and personal use. Commercial power quality analyzers are expensive and are reserved for industry and specialized research institutions. Therefore, we hope to be able to provide a low cost-alternative that could be used in laboratory and teaching environments. Furthermore, we believe that tool could be utilized personally to, for example, check appliances or homemade projects to make sure that the correct amount of AC power is being provided. Overall, through this project, we hope to be able make a useful tool more accessible for everyone, while still being accurate and efficient.

5. Citations

[1] *IEEE Code of Ethics*, IEEE, 2020. [Online]. Available: https://www.ieee.org/about/corporate/governance/p7-8.html