OscilloSketch

Design Document

ECE 445 Spring 2026

Team 22

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1. Introduction

1.1 Problem

Oscilloscope XY mode enables visualization of two-dimensional signals and vector-style graphics by mapping two analog voltages to horizontal and vertical deflection. While powerful, interactive control of XY mode typically requires multiple laboratory instruments or improvised embedded setups. Many existing approaches are not portable, are not purpose-built, and do not emphasize safe output scaling and protection. Improper signal scaling, unstable update timing, and lack of output protection can reduce visualization quality and can create avoidable risk to oscilloscope inputs.

1.2 Solution

OscilloSketch is a handheld embedded device designed to generate safe and stable bipolar X and Y voltages for oscilloscope XY mode while providing intuitive user interaction. The device functions like an Etch a Sketch. Two rotary encoders control cursor position in real time, enabling continuous line drawing on an oscilloscope display. The system is powered entirely from a single USB-C connection and outputs analog X and Y signals through BNC connectors, enabling simple setup, portability, and seamless interfacing with standard laboratory oscilloscopes. The design emphasizes deterministic timing, predictable user input, clean mixed signal design, and protection at user accessible connectors.

Base functionality focuses on interactive drawing. Future revisions may add Z blanking for beam intensity control and a demo mode that renders preprogrammed vector shapes.

1.3 Visual Aid

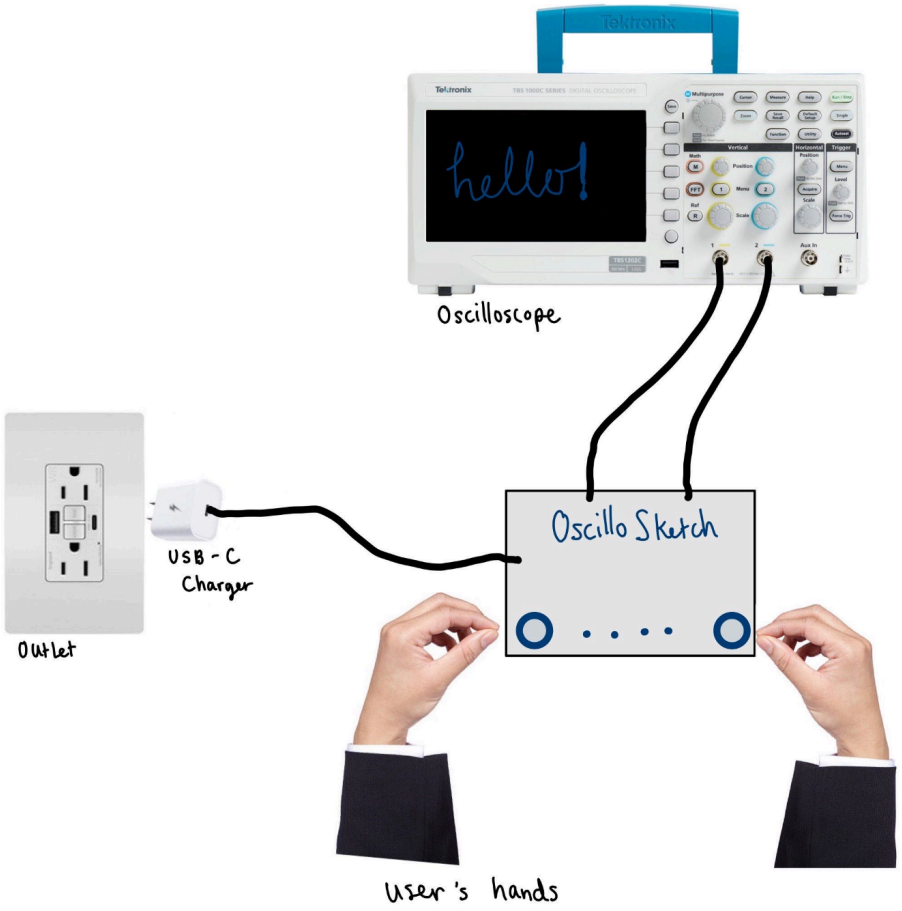

Figure 1. Application diagram. A user using an OscilloSketch

As shown in Figure 1, the OscilloSketch consists of two control knobs and four buttons that can be powered through a USB-C port. Typically, to supply enough current, it is recommended to power the OscilloSketch through a USB wall charger. The device generates two independent analog voltage outputs corresponding to the X- and Y-axis position signals. These outputs are transmitted through coaxial BNC cables to the oscilloscope's CH1 and CH2 inputs, respectively. When the oscilloscope is configured in XY mode, CH1 drives the horizontal position, and CH2 drives the vertical position, enabling real-time two-dimensional vector rendering of user-controlled waveforms on the display.

The user interacts with the system through two primary rotary control knobs, one assigned to each axis, allowing independent and continuous adjustment of the horizontal and vertical position signals. By turning these knobs with both hands, the user can smoothly trace curves,

corners, and complex shapes directly onto the oscilloscope screen. Several push buttons located along the center of the device provide additional control, such as switching between operating modes and enabling free draw or constrained motion. This combination of rotary inputs and simple button controls creates an intuitive and responsive interface that transforms the oscilloscope into an interactive drawing tool.

Figure 2. Concept inspiration. Traditional Etch-a-Sketch toy

Figure 2 illustrates the conceptual inspiration behind the OscilloSketch. The traditional Etch A Sketch toy uses two mechanical knobs to independently control the horizontal and vertical motion of a drawing stylus, allowing users to create images through coordinated two-axis movement and continuous line tracing. This simple yet engaging control scheme directly influenced the design of the OscilloSketch. By mapping each rotary knob to an independent X- and Y-axis voltage output, the system recreates the familiar two-handed drawing experience in an electronic form while enabling smooth, continuous drawing on the display. Instead of mechanically moving a stylus across a screen, the OscilloSketch generates corresponding analog voltage signals that continuously position the trace on an oscilloscope.

1.4 High-Level Requirements

The project is considered successful only if the system meets all of the following.

- **The system shall generate two independent continuous analog output voltages with at least 12-bit resolution and an output range near plus and minus 5 V suitable for oscilloscope XY mode.**
- **The system shall operate entirely from a single 5 V USB-C connection and shall draw less than or equal to 500 mA while supporting both device power and firmware programming.**
- **The system shall provide real-time Etch a Sketch style control, where two rotary encoders continuously control the X and Y cursor position with input to output latency less than or equal to 20 ms, and where motion appears smooth on the oscilloscope during normal use. The design target is an output update rate of at least 10,000 coordinated X-Y points per second.**

2 Design

2.1 Physical Design

The enclosure will be 3D printed and designed to provide structural support and proper alignment of all external interfaces, as shown in Figure 3. The PCB, approximately 98.5mm × 83mm, will be secured inside the enclosure using four corner mounting holes and standoffs to ensure mechanical rigidity and prevent board flex. Cutouts in the top surface allow the rotary encoders and four pushbuttons to extend through the enclosure for easy user interaction. The two BNC connectors for the X and Y outputs pass through the side wall of the enclosure and are mechanically fastened to the enclosure panel. This panel mounting provides strain relief and prevents mechanical stress from being transferred directly to the PCB during cable insertion or removal. A dedicated opening provides access to the USB-C connector for power and programming.

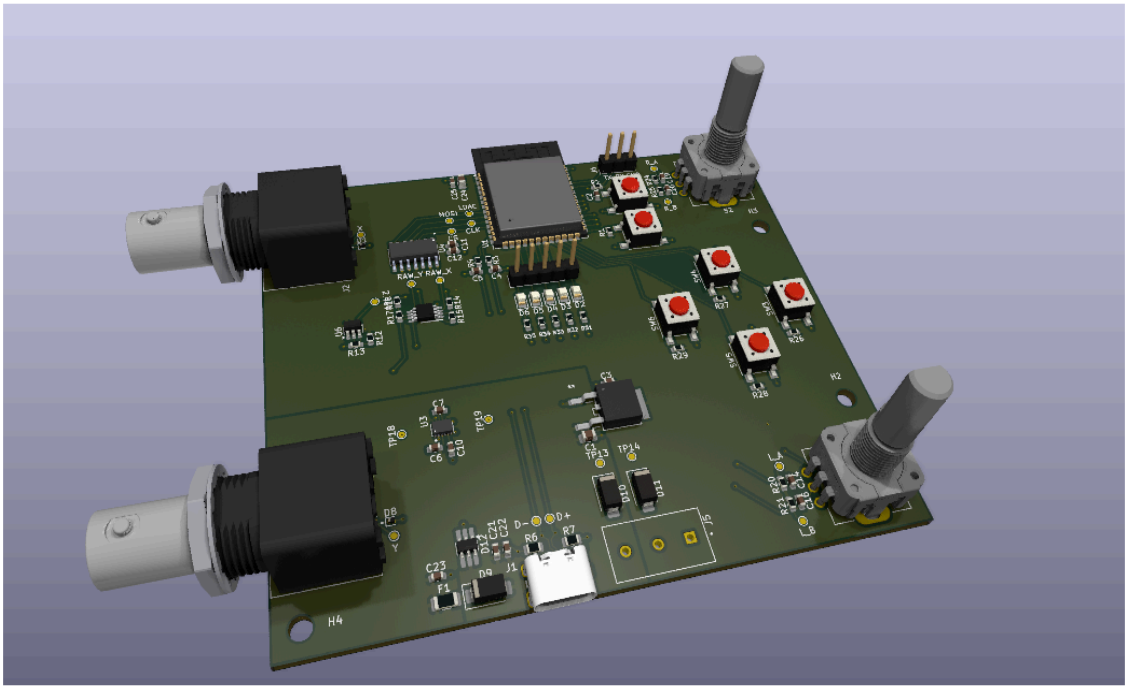

Figure 3. Physical layout concept for OscilloSketch.

2.2 Block Diagram

USB-C provides 5 V power to the Power Subsystem and USB D+ and D- for programming the ESP32-S3. The Power Subsystem generates a regulated 3.3 V digital rail and regulated plus 5 V and minus 5 V analog rails. The UI Subsystem provides quadrature encoder signals and pushbutton inputs to the MCU. The MCU processes user inputs and updates a dual 12-bit DAC over SPI, using LDAC to synchronize X and Y updates. The DAC outputs are mapped to bipolar signals by the analog output stage and routed through output impedance and clamp protection to the BNC X and BNC Y connectors for oscilloscope XY mode.

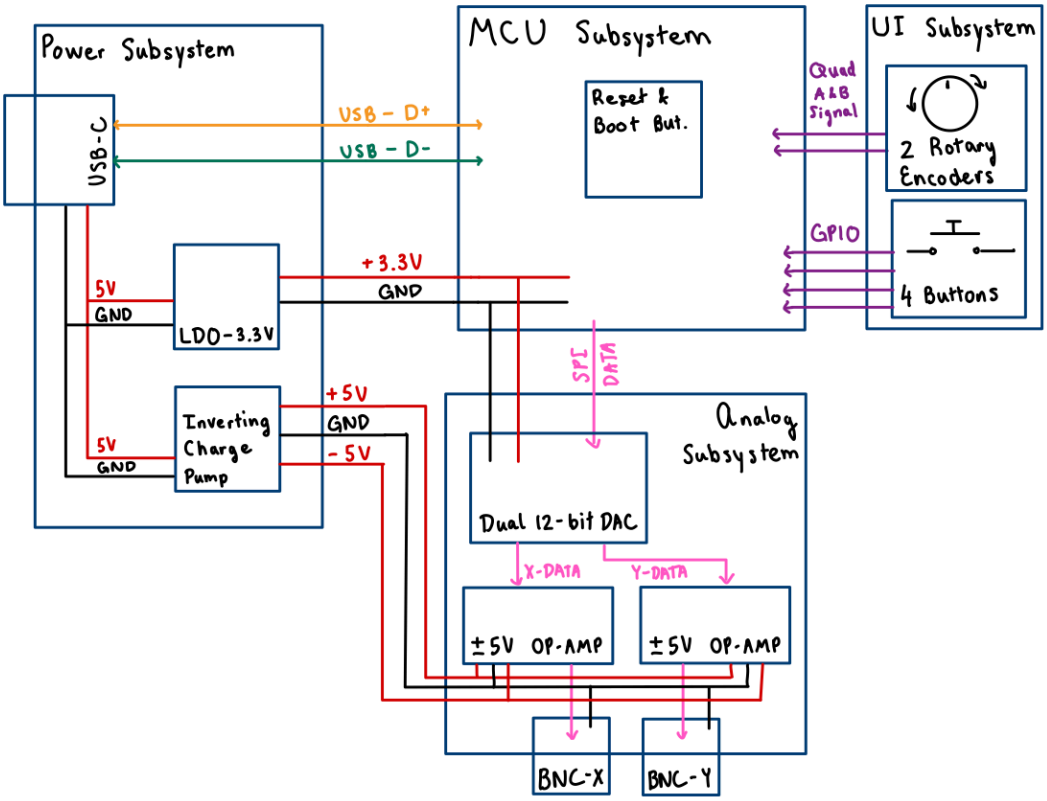

Figure 4. Block diagram of OscilloSketch.

2.3 Functional Overview and Block Diagram Requirements

This section defines subsystem behavior and quantitative requirements needed to meet the high-level goals. Each subsystem includes a requirements and verification table.

2.3.1 Power Subsystem

The power subsystem accepts 5 V from USB-C and generates regulated 3.3 V for digital circuitry and +5 V and -5 V for the analog output stage. This subsystem supports a stable output swing and prevents glitches caused by rail sag. Key design choices include the AZ1117C 3.3 V LDO for digital power and the LM27762 charge pump for regulated bipolar analog rails.

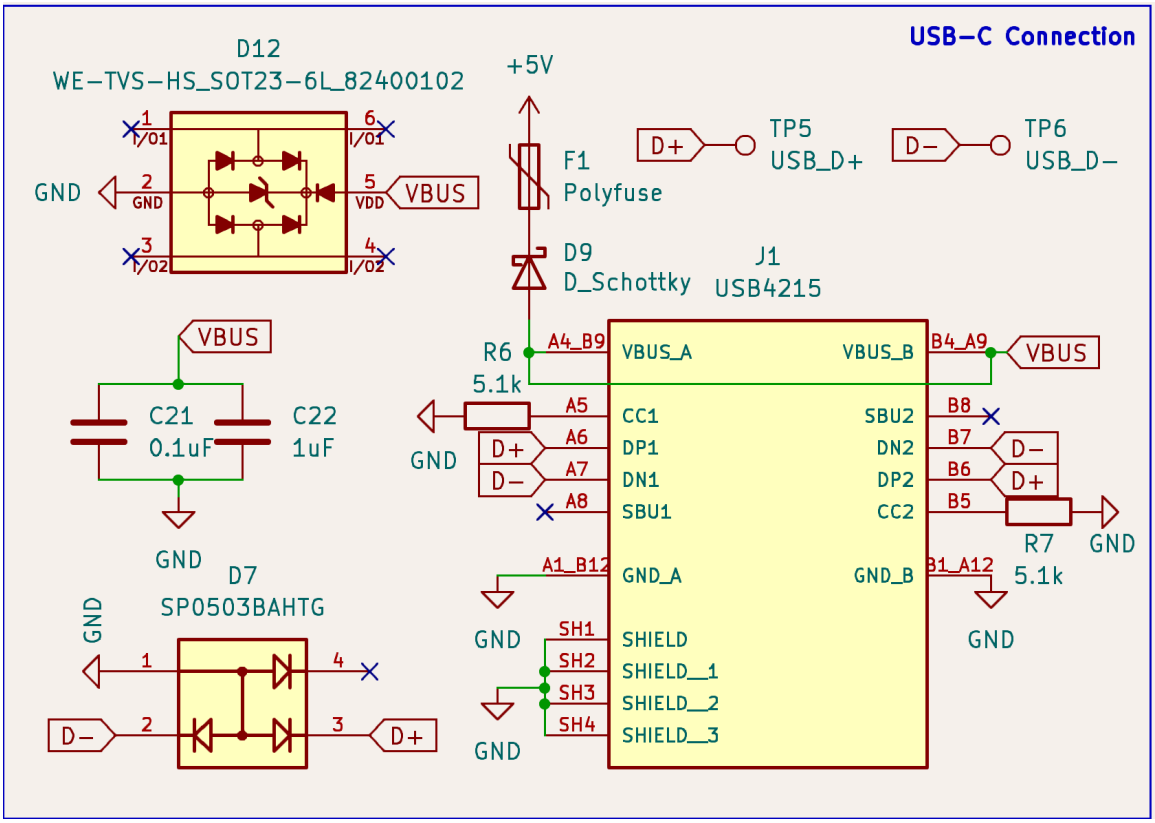

Figure 5.1 Schematic of USB-C Connection with Protection.

Figure 5.1 shows the USB-C input stage and associated protection circuitry for the Power Subsystem. The USB-C connector (J1) provides 5 V VBUS for system power and USB D+ and D− lines for programming the ESP32-S3. The CC1 and CC2 pins are each connected to 5.1 kΩ pull-down resistors (R6 and R7), which advertise the device as a sink and enable proper 5 V negotiation from a standard USB-C source.

To protect against electrostatic discharge (ESD) and cable transients, transient voltage suppression (TVS) devices are placed on both the VBUS line and the USB data lines. The VBUS rail is protected by D12 (Würth Elektronik 82400102), a 5 V working voltage (VRWM) TVS diode. This device clamps high-energy surges on VBUS to a safe level (approximately 7-8 V clamp region depending on surge current), preventing overvoltage stress on downstream regulators and power circuitry during plug-in events or ESD strikes.

The USB data lines (D+ and D−) are protected by D7 (onsemi SP0503BAHTG), a low-capacitance ESD protection array specifically designed for high-speed data interfaces. The device has a typical line capacitance of approximately 30 pF per channel, minimizing signal distortion and preserving USB full-speed signal integrity. The SP0503BAHTG provides IEC 61000-4-2 ESD protection while introducing negligible loading to the differential pair.

A resettable polymer fuse (F1, 0ZCJ0100FF2E) is placed in series with VBUS to provide overcurrent protection. This device is a 1206 footprint PPTC fuse with a hold current of approximately 1.0 A and low series resistance under normal operation. In the event of a downstream short or fault condition, the fuse transitions to a high resistance state, limiting current drawn from the USB source and preventing damage to the host port or on-board circuitry. Once the fault is removed and the device cools, the fuse automatically resets, eliminating the need for replacement.

A series Schottky diode, D9 (CDBA540-HF, 5 A, 40 V, DO-214AC/SMA package), provides reverse current protection on the VBUS path. The CDBA540-HF has a low forward voltage drop and fast response, allowing normal USB power delivery while preventing backfeeding into the USB source if external voltage is present elsewhere on the board. In fault conditions, the diode blocks reverse conduction and protects the host port from unintended current injection.

Local bulk and high-frequency decoupling capacitors (C21 = 0.1 µF and C22 = 1 µF) are placed directly on VBUS to stabilize the 5 V rail. These capacitors reduce voltage droop during cable insertion and transient load events, improving supply stability and preventing regulator or microcontroller brownout conditions.

Lastly, the test points (TP5, TP6) are included on the USB data lines to facilitate debugging and signal validation during development. Together, this is the front end that ensures safe power

delivery to form a protected and stable 5 V input for the downstream ±5 V analog rail generation and 3.3V regulator.

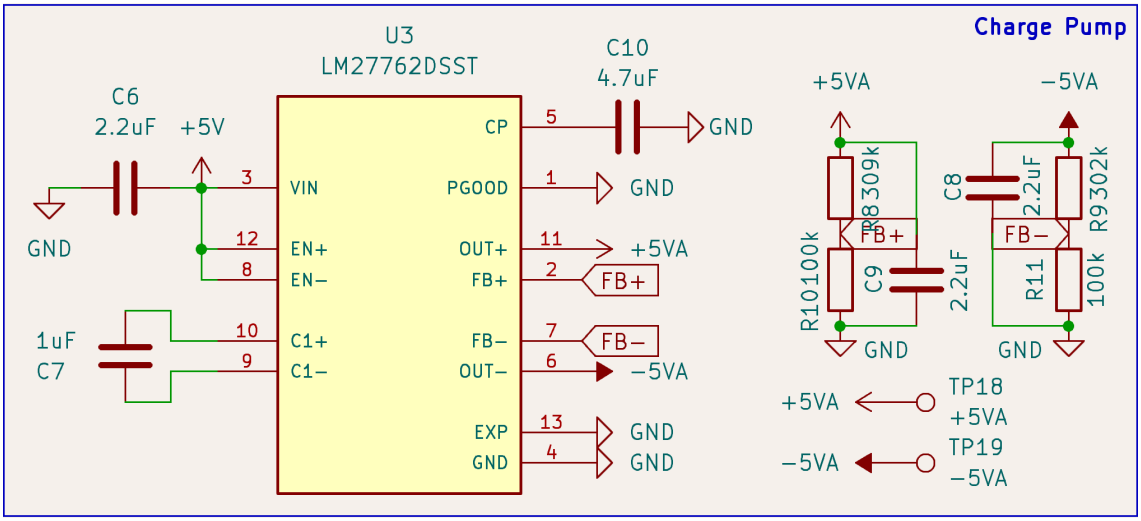

Figure 5.2 Schematic diagram of the Charge Pump IC and Circuit.

Figure 5.2 shows the ±5 V rail generation stage using the LM27762 regulated charge pump. This device converts the incoming 5 V rail into regulated +5VA and -5VA supplies required for the bipolar analog output stage. A charge pump architecture is selected to generate a negative rail without requiring an inductor, reducing board area and electromagnetic interference compared to a switching converter.

Input capacitor C6 provides local decoupling for the 5 V supply to minimize input ripple and support transient current demands. The flying capacitor (C7) connected between C1+ and C1− enables the internal charge transfer process that inverts and regulates the output. Capacitor C10 connected to the CP pin supports internal pump operation and stabilizes switching behavior.

The feedback networks (R8, R10, C9 for +5VA and R9, R11, C8 for -5VA) set the regulated output voltages according to the LM27762 feedback equations. The device regulates each output by maintaining its FB pin at an internal reference voltage of approximately 1.2 V for the positive rail and −1.22 V for the negative rail. Using the equation $Vout = (1 + \frac{Rtop}{Rbot})$, the selected values R8 = 316 kΩ and R10 = 100 kΩ yield +5 V rail voltage of 4.99 V, while R9 = 309 kΩ and R11 = 100 kΩ yield -5 V rail voltage of -4.98 V. These ratios produce nearly symmetric

±5 V rails while satisfying the datasheet requirement that the lower feedback resistor be at least 50 kΩ and having a tolerance of only ±1% to ensure a nominal voltage. The capacitors in the feedback networks provide filtering to improve stability and reduce switching ripple. Output capacitors further reduce ripple and enhance transient response under dynamic load conditions.

Test points TP18 and TP19 are included to allow measurement and validation of the +5 VA and −5 VA rails during development and verification. This IC and circuit enable the true bipolar output capability for the op-amp stage, ensuring symmetric signal swing about ground and preventing clipping when driving the oscilloscope in XY mode.

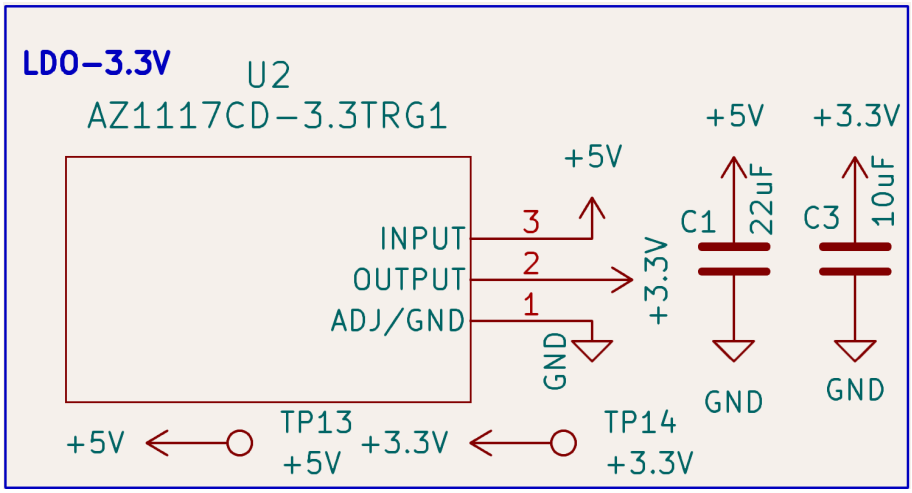

Figure 5.2 Schematic of LDO from 5 V to 3.3 V

Figure 5.2 shows the 3.3 V regulation stage using the AZ1117CD-3.3 LDO (U2), which converts the 5 V USB rail into a stable 3.3 V supply for the ESP32-S3, DAC digital interface, and other logic level circuitry. An LDO is used to provide a low noise, well-regulated digital rail and to reduce sensitivity to USB transients or supply ripple. Input capacitor C1 (22 µF) provides local bulk decoupling to support sudden load current changes and prevent the regulator input from sagging, while output capacitor C3 (10 µF) ensures loop stability and reduces output ripple as required by the LDO's datasheet. Test points TP13 (+5 V) and TP14 (+3.3 V) are included to allow straightforward verification of the input and regulated rails during debugging.

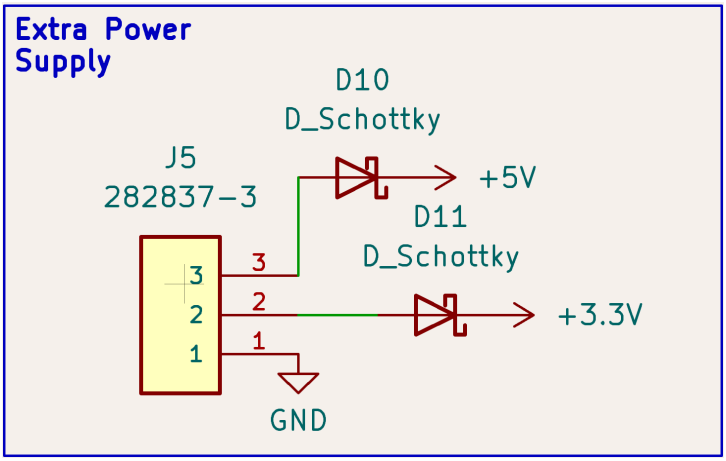

Figure 5.3 Schematic of Connector for External Power Supply.

Figure 5.3 shows an optional external power input connector (J5) that allows the system to be powered from an off-board supply during testing. The connector provides GND and separate +5 V and +3.3 V inputs, each routed through series Schottky diodes (D10 and D11, CDBA540-HF, DO-214AC). These diodes provide reverse current isolation and prevent backfeeding between the external supply and the on-board rails, protecting both the USB-C source and the external supply if multiple power sources are connected simultaneously.

Requirement	Verification Procedure
With USB input from 4.75 V to 5.25 V, the 3.3 V rail shall remain between 3.20 V and 3.40 V while supplying up to 150 mA load current.	Equipment: bench supply, DMM. Steps: power the board from a bench supply at 4.75 V then 5.25 V. Measure 3.3 V at the 3.3 V test point. Record min and max.
The plus 5 V and minus 5 V analog rails shall be within plus or minus 0.30 V of nominal during normal operation.	Equipment: DMM. Steps: power the board from USB. Measure plus 5 V and minus 5 V at rail test points at idle and while drawing. Record values.

USB input protection shall limit sustained current during a hard short on the 5 V rail using a resettable polyfuse.	**Equipment: bench supply with current limit. Steps: set supply current limit to 1 A. Short 5 V to GND at a test jumper for less than 2 seconds. Confirm current is limited and the board recovers after removing the short.**

2.3.2 Microcontroller and Firmware Subsystem

Figure 6.1 shows the ESP32-S3-WROOM-1 microcontroller and its primary hardware interfaces to the rest of the system. The module is powered from the regulated 3.3 V rail and is locally decoupled with bulk and high frequency capacitors (C24 = 22 µF and C25 = 0.1 µF) to reduce supply droop and noise during high transient load events. USB D+ and D− are routed directly to the ESP32-S3 for native USB programming, with 22 Ω series resistors (R3, R4) included for signal integrity by damping edge ringing on the differential pair. The module also includes the standard boot and enable circuitry required for reliable startup and flashing: CHIP_PU (EN) is pulled up to 3.3 V through R2 (10 kΩ) with a capacitor (C2 = 1 µF) to provide a power on reset delay, while the BOOT signal is pulled up through R1 (10 kΩ) and can be asserted low with a pushbutton (SW1) to enter the ROM bootloader.

User interface signals are connected to dedicated GPIO pins, including quadrature inputs for the left and right rotary encoders (LEFT_A/LEFT_B and RIGHT_A/RIGHT_B) and pushbutton inputs (LEFT_Button, RIGHT_Button, B1, B2, B3, and B4). The DAC interface uses an SPI bus (SPI_CLK and SPI_MOSI) with a chip select line (SPI_CS) and a dedicated LDAC control line to allow synchronized X/Y output updates. Test points (TP9-TP12) are provided on the SPI and LDAC nets to support debugging and timing verification during bring up. A 3-pin header (J6) exposes UART TX/RX for optional serial logging and recovery if USB debugging is unavailable.

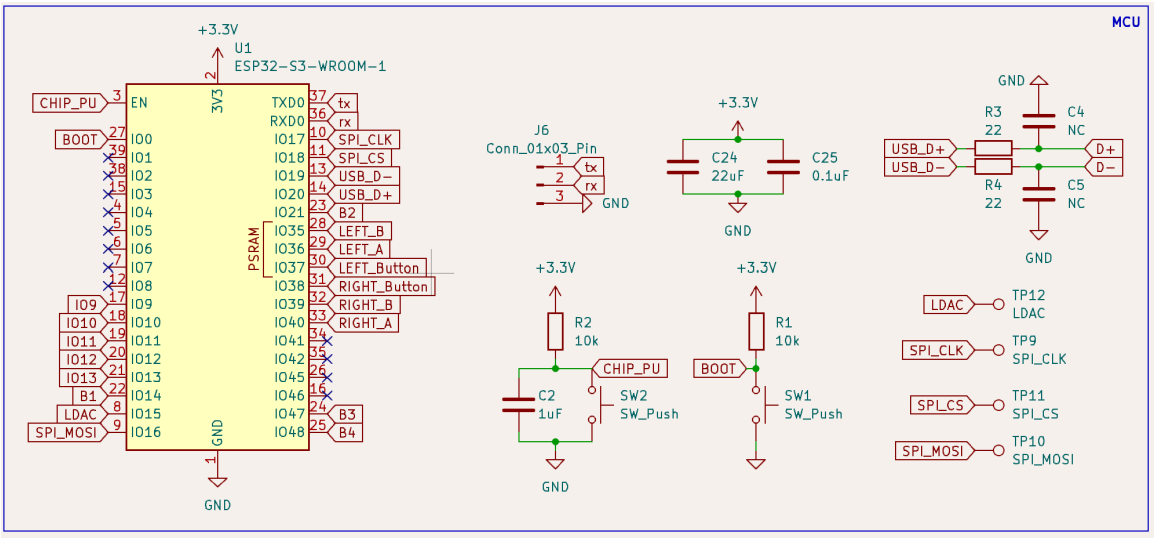

Figure 6.1 Schematic of the ESP32-S3-WROOM-1 and its connections

Figure 6.2 illustrates the firmware timing architecture of the OscilloSketch. The ESP32-S3 operates around a 10 kHz hardware timer interrupt that establishes a deterministic 100 µs update period to meet the 10,000 coordinated X-Y points per second requirement. As shown in the flow chart, each timer tick advances a buffer index, retrieves the next stored X-Y coordinate pair, transmits both 12-bit values to the dual DAC over SPI, and then pulses LDAC to synchronize the simultaneous update of both output channels.

To ensure that drawings remain visible on oscilloscopes without built-in display persistence, generated X-Y positions are stored in a circular buffer during operation. Each point consists of two 12-bit DAC values stored as 16-bit integers, resulting in 4 bytes per point. For example, a buffer of 20,000 points requires approximately 80 kB of RAM, which is well within the available memory of the ESP32-S3. As depicted in Figure 6.2, the 10 kHz loop continuously steps through this buffer and wraps back to the beginning when the end is reached, effectively replaying the entire drawing path in a continuous cycle while new points are appended during active drawing.

Encoder inputs are captured asynchronously through interrupt-based quadrature decoding or dedicated hardware peripherals, allowing position changes to be recorded without disrupting the real time update sequence. Pushbutton inputs are debounced in software and influence

the coordinate generation logic shown in the flow chart, such as enforcing axis constraints or selecting preset behaviors. SPI communication is configured at a clock frequency significantly higher than the 10 kHz update rate, ensuring both DAC writes complete comfortably within the 100 µs timing window. This separation between asynchronous input handling and deterministic timer-driven output ensures consistent timing and minimal output jitter.

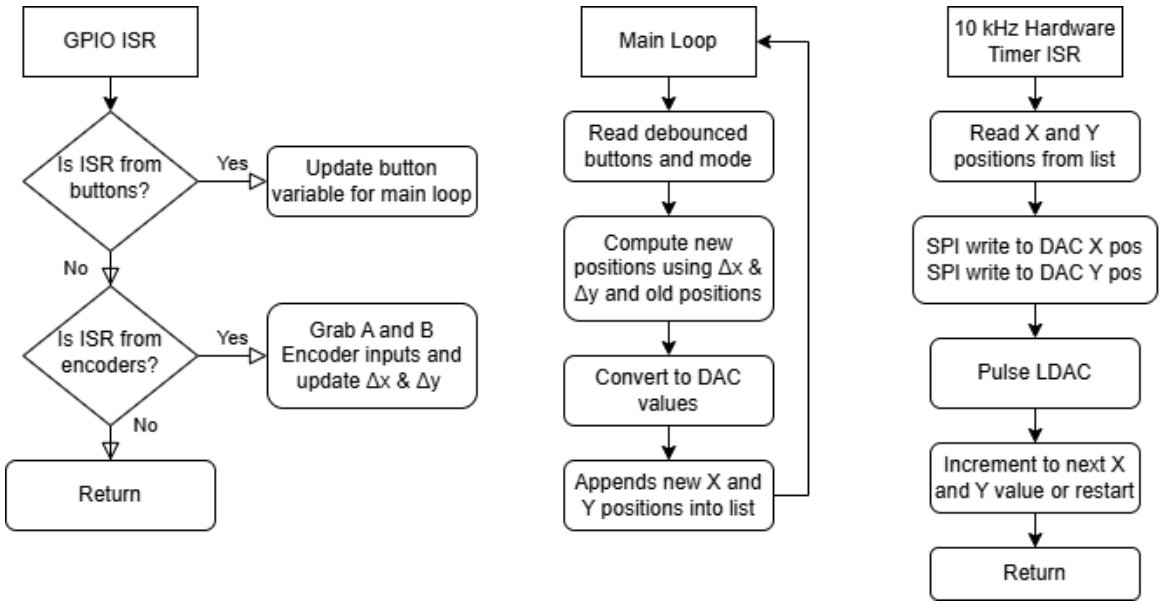

Figure 6.2 Firmware Timing Flow Chart

Requirement	Verification Procedure
The system shall update DAC outputs at a minimum of 10,000 coordinated points per second.	Equipment: oscilloscope. Steps: configure firmware to toggle a GPIO on every LDAC pulse. Measure toggle frequency on the scope and confirm at least 10 kHz. Save screenshot.
SPI shall run at 5 MHz and shall communicate without visible DAC update errors during continuous operation for 5 minutes.	Equipment: oscilloscope or logic analyzer. Steps: probe SCK and CS. Confirm SCK is 5 MHz. Run continuous output for 5 minutes and confirm no freezing or glitches.

Firmware shall initialize outputs to a safe state by setting X and Y near midscale before enabling continuous updates.	**Equipment: oscilloscope. Steps: power cycle the board while probing both BNC outputs. Confirm outputs settle near 0 V and do not jump to a rail during startup.**

2.3.3 User Input Subsystem

As shown in Figure 7 (right side), there are two PEC11R rotary encoders that provide quadrature A and B outputs along with integrated pushbutton switches. In Figure 7 (left side), there are four additional pushbuttons (B1-B4) that provide user functions such as clear and mode selection. All pushbuttons are implemented as active low inputs with 10 kΩ pull-up resistors to the 3.3 V rail. When pressed, the corresponding GPIO is pulled to ground. Debouncing is performed entirely in firmware using a short time based validation window within the main control loop, allowing debounce timing to be tuned during bring-up without requiring hardware changes.

The rotary encoder quadrature outputs (LEFT_A/LEFT_B and RIGHT_A/RIGHT_B) are pulled up to 3.3 V through 10 kΩ resistors and include 0.01 µF capacitors to ground, forming first order RC filters. These networks attenuate high-frequency noise and suppress fast transients caused by mechanical contact bounce while preserving sufficient edge sharpness for reliable interrupt detection. Final edge qualification, direction decoding, and incremental count accumulation are performed in firmware using GPIO interrupts, where the complementary channel state is sampled to determine rotation direction.

User input is designed to provide responsive and predictable incremental control rather than absolute position metrology. Encoder delta counts are mapped into DAC code increments using a configurable scaling factor (STEP = 8 codes per detent). This mapping defines the sensitivity of X/Y position updates and can be adjusted in firmware during system bring-up to refine user response without modifying the hardware.

Test points (TP1-TP4) are provided on the quadrature signal lines to support signal integrity verification, timing analysis, and debugging during bring-up. These access points allow

oscilloscope observation of encoder waveforms to confirm proper edge timing, noise suppression, and direction decoding behavior without disturbing normal system operation.

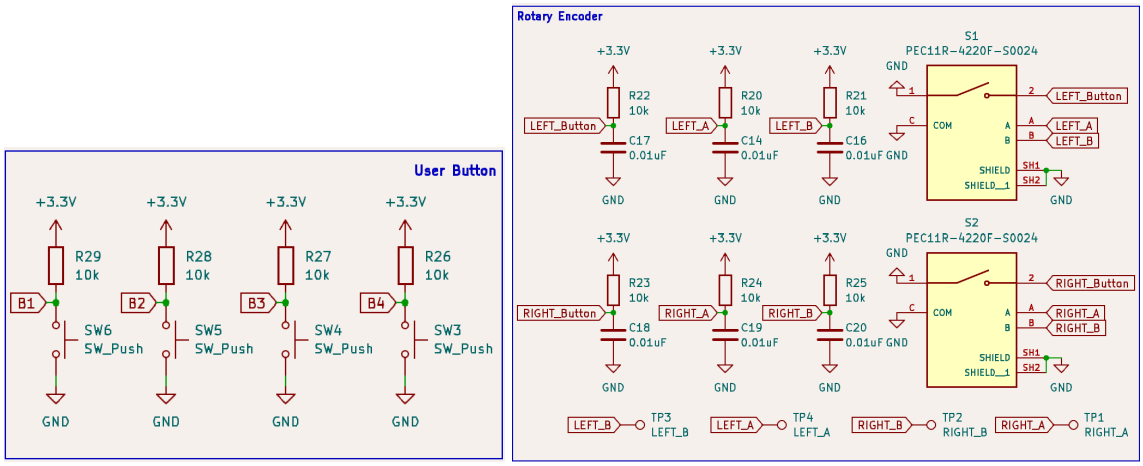

Figure 7. Schematic of four buttons (on left) and two rotary encoders (on right)

Requirement	Verification Procedure
Encoder rotation shall move the output in the correct direction for both axes under typical user rotation speeds.	Equipment: oscilloscope in XY mode. Steps: rotate each encoder clockwise then counterclockwise. Confirm motion direction matches the intended axis mapping.
For 20 detents of rotation, output change shall be within plus or minus 1 detent equivalent of the expected change using STEP = 8.	Equipment: DMM or oscilloscope. Steps: rotate exactly 20 detents. Expected code change is 160 codes. Expected voltage change is about 0.39 V. Measure and compare. Repeat at faster rotation.
Button press latency after debouncing shall be less than or equal to 20 ms.	Equipment: oscilloscope. Steps: toggle a GPIO when a button press is registered. Probe button line and GPIO. Measure time difference.

2.3.4 DAC Subsystem

Figure 8 shows the MCP4922 (U4) dual 12-bit DAC, which is powered from the regulated 3.3 V rail (VDD) and uses the same 3.3 V rail as the reference for both channels (VREFA and VREFB), producing full scale outputs from 0 to 3.3 V. The DAC is controlled over a 3-wire SPI interface consisting of SPI_CLK (SCK) and SPI_MOSI (SDI), with SPI_CS providing frame synchronization and chip selection. The SHDN pin is tied high to keep the DAC enabled during normal operation.

Both analog channels are routed as RAW_X (VOUTA) and RAW_Y (VOUTB). These outputs represent the unbuffered DAC voltages prior to any downstream amplification or filtering stages. Local decoupling capacitors (C11 = 0.1 µF and C12 = 10 µF) are placed at the DAC supply to reduce high-frequency supply noise and are recommended in the datasheets.

The LDAC control line is used to synchronize updates across both channels. New X/Y codes are first loaded through SPI, then LDAC is asserted to simultaneously transfer the buffered codes to the output latches, ensuring coordinated point updates and preventing intermediate states where one axis changes before the other. Test points (TP7 and TP8) are provided on RAW_X and RAW_Y to allow oscilloscope verification of output levels, settling behavior, and update timing during testing and debugging.

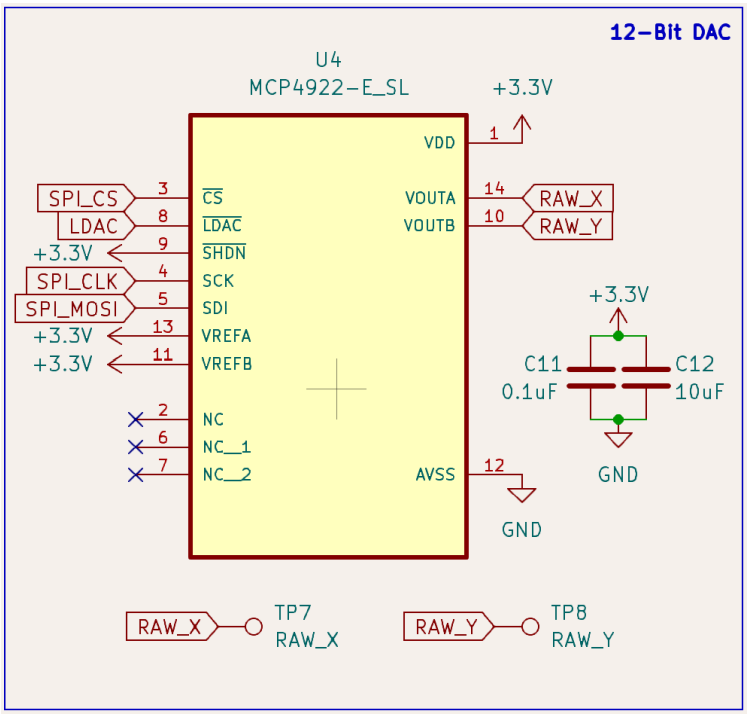

Figure 8. Schematic of the 12-Bit DAC

Requirement	Verification Procedure
RAW_X and RAW_Y shall span 0 V to 3.3 V nominal and shall be monotonic across full scale.	Equipment: DMM, oscilloscope. Steps: run a sweep from code 0 to 4095. Measure RAW test points. Confirm endpoints and monotonic behavior.
X and Y updates shall be coordinated using LDAC so both channels change at the same time within one update period.	Equipment: oscilloscope. Steps: output a pattern where both channels step at once. Probe RAW_X and RAW_Y. Confirm edge alignment.

2.3.5 Analog Output and Protection Subsystem

Figure 9 shows the analog output and protection stage used to translate the MCP4922 DAC outputs (RAW_X and RAW_Y) from a unipolar 0-3.3 V range into a bipolar signal of approximately ±5 V centered near 0 V. The OPA2192 is a dual channel precision op amp, with each channel configured as a level shifted non-inverting gain stage using a reference voltage (Vref). One amplifier processes the X channel and the other processes the Y channel, ensuring matched gain and offset characteristics between axes.

The reference voltage (Vref = 2.46 V) is generated locally using U6 (TLV9061xDBV) configured as a unity gain buffer. A resistive divider consisting of R12 = 3.4 kΩ (from +3.3 V to the divider node) and R13 = 10 kΩ (from the divider node to ground) establishes the nominal reference level. The divider produces:

$$Vref = 3.3V \cdot \frac{R13}{R13+R12} = 3.3V \cdot \frac{10k\Omega}{10k\Omega+3.4k\Omega} = 3.3V \cdot \frac{10}{13.4} = 2.46V$$

The divider node is filtered by C13 (0.1 µF) and C15 (10 µF) to reduce supply ripple and broadband noise before being buffered by U6. The TLV9061 operates as a voltage follower, providing a low-impedance, stable reference output labeled 2.46 V. Buffering is required because Vref directly participates in the transfer function of the OPA2192 gain stage, and so

any variation, droop, or noise on the reference would directly appear as output offset error on both the X and Y channels. The buffered reference, therefore, ensures consistent bipolar scaling and improved stability during supply transients and rapid DAC updates.

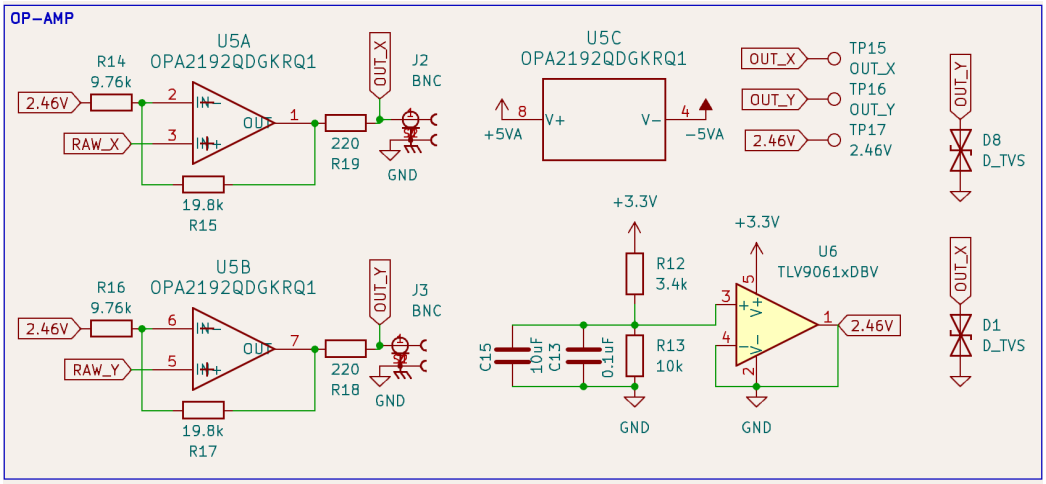

Figure 9. Schematic of the Analog Output and Protection

The output stage implements the following transfer function, where Vin (RAW_X or RAW_Y) is the unbuffered DAC outputs from the MCP4922 (0-3.3 V). The buffered reference voltage is Vref = 2.46 V, with Rf = 19.8 kΩ and Rref = 9.76 kΩ (both 1% tolerance resistors).

From a TI article, the transfer function of the level shifted non-inverting stage is:

$$Vout = (1 + \frac{Rf}{Rref}) \cdot Vin - (\frac{Rf}{Rref}) \cdot Vref = 3.0287 \cdot Vin - 4.996$$

This mapping converts the DAC's unipolar 0-3.3 V range into an approximately ±5 V bipolar output:

- **RAW_X or RAW_Y = 0 V → Vout ≈ −5.0**
- **RAW_X or RAW_Y = 1.65 V → Vout ≈ 0 V**
- **RAW_X or RAW_Y = 3.3 V → Vout ≈ +5.0 V**

The use of 1% tolerance resistors limits gain and offset variation between the X and Y channels, helping maintain axis symmetry and consistent scaling. Any residual mismatch primarily appears as a small gain or offset error rather than distortion.

Because the MCP4922 is a 12-bit DAC (4096 codes), the raw DAC step size is: 3.3 V / 4096 = 0.806 mV per code. Then, after amplification by a factor of 3.0287, the effective output resolution at the BNC connector becomes: 0.806 mV × 3.0287 ≈ 2.44 mV per code. This resolution provides smooth deflection on the oscilloscope while maintaining the full ±5 V output span.

To improve robustness during debugging and external connections, a series of output resistors (47-220 Ω) is placed near each BNC connector along with clamp protection devices. The intended oscilloscope load is a Tektronix 2225 with a 1 MΩ input impedance, so the series resistor has negligible impact on the displayed amplitude under normal operation. However, the added resistance improves fault tolerance by limiting output current if the channel is accidentally connected to a 50 Ω-terminated input or otherwise shorted.

Additional protection is provided by a bidirectional TVS diode (Littelfuse SP1005-01ETG) placed at each BNC output. This device provides low capacitance transient suppression and clamps positive and negative voltage spikes relative to ground, protecting the op-amp output from ESD events and cable hot plug transients. The bidirectional configuration is necessary because the analog output swings both above and below ground.

In the worst case, if the output is connected to a 50 Ω termination, the 220 Ω series resistor limits the current. With a 5 V output and total resistance of 270 Ω (220 Ω + 50 Ω), the current is approximately 18.5 mA. This is within the safe operating range of the OPA2192 and protects the output in the event of a 50 Ω load while maintaining normal performance under the intended 1 MΩ oscilloscope input.

Requirement	Verification Procedure
Each BNC output shall produce at least +4.5 V and at least -4.5 V when commanded to full scale codes, measured with a 1 Mohm oscilloscope input.	Equipment: oscilloscope, DMM. Steps: set code 0 and 4095. Measure DC output at BNC. Record min and max.

When the DAC code is midscale, each BNC output shall be within plus or minus 0.10 V of 0 V.	**Equipment: DMM, oscilloscope. Steps: set code 2048. Measure BNC output and record offset.**
The effective output step size shall be 2.44 mV per code with tolerance plus or minus 15 percent.	**Equipment: oscilloscope. Steps: step code by 1 at several starting points. Use averaging and measure delta. Record values.**
The output shall not show sustained oscillation when driving the intended coax cable into a 1 Mohm scope input.	**Equipment: oscilloscope. Steps: connect through the intended coax. Output a stepping pattern. Confirm no continuous oscillation and save a screenshot.**

2.4 Tolerance Analysis

The most challenging analog requirement is maintaining the output centered near 0 V at DAC midscale while preserving a full ±5 V swing. The mapping stage must simultaneously set the correct gain and the correct offset. Any mismatch in resistor ratios or reference voltage directly shifts the zero point or scales the output incorrectly.

As shown before, the transfer function of the mapper is:

$$Vout = (1 + r) \cdot Vin - (r \cdot Vref) = (3.0287) \cdot Vin - 4.996$$

Where r = 2.0287 and Vref = 2.46V. Therefore, when Vin is at midscale, Vin = 1.65, Vout should be very close to 0 V as shown below:

$$Vout = (3.0287) \cdot 1.65 - (4.996) = 0.00127\,V$$

However, there are two primary sources that contribute to midscale offset error. The first is variation in the gain ratio = r / Rref, which depends on the tolerance of the feedback and reference resistors. Any deviation in this ratio alters the effective scaling of both the input and reference terms in the transfer function. The second source is variation in the reference voltage Vref, which is established by a resistor divider and buffered by the TLV9061. Changes in

Vref directly shift the subtraction term in the mapping equation, resulting in a DC offset at the output.

With 1% tolerance resistors, the gain ratio r varies approximately from 1.9885 to 2.0697, while the buffered reference voltage Vref varies approximately from 2.450 V to 2.475 V. Because both r and Vref appear multiplicatively in the transfer function, the worst case midscale offset occurs when r and Vref deviate in opposite directions. Evaluating these extreme combinations at Vin = 1.65 V yields a maximum midscale output deviation on the order of ±60 mV.

This behavior can also be understood by rearranging the midscale condition as:

$$Vout = r \cdot (1.65 - Vref) + 1.65$$

Since 1.65 - Vref is approximately -0.81 V, the output is moderately sensitive to changes in r. This means that matching between Rf and Rref is slightly more critical than the absolute accuracy of the reference divider. Using 1% tolerance resistors keeps the gain ratio stable enough to meet the centering requirement without needing 0.1% precision components.

A ±60 mV offset corresponds to only about 1.2% of the ± 5 V full scale span. On the oscilloscope display, this appears as a very small vertical or horizontal shift of the drawing center point and does not materially affect visual symmetry. The ±60 mV worst case deviation remains within the ±100 mV specification, leaving approximately 40 mV of design margin. The additional error from the op-amp input offset voltage is small compared to the resistor induced error and does not significantly reduce this margin.

3. Cost and Schedule

3.1.1 Labor Cost Analysis

The primary cost associated with this project is engineering labor. A reasonable starting salary for a University of Illinois ECE graduate is approximately $80,000 per year. Assuming 2080 working hours per year, this corresponds to an hourly rate of $38.46 per hour. Per project guidelines, labor cost is calculated as ($/hour) × 2.5 × (hours worked). Assuming each partner contributed approximately 112 hours (estimated as 7 hours per week over a 16-week semester) to system design, PCB layout, firmware development, debugging, and validation, the labor cost per partner is $38.46/hour × 2.5 × 112 hours ≈ $10,769. For two partners, the total estimated labor cost is therefore: 2 × $10,769 ≈ $21,537.60. As expected for a prototype development effort, labor represents the dominant cost component of the project, significantly exceeding the material cost of the hardware itself.

3.1.2 Part Cost Analysis

The DigiKey cart total is $58.83, including shipping and applicable tariffs. This includes major components such as the MCP4922 DAC, OPA2192 op-amp, and PEC11R, protection devices, BNC connectors, and supporting passive components not available locally.

Reference	Value	Qty	Bought Qty	Location	Link	Total Cost
C6,C8,C9	2.2uF	3	10	Digikey	https://ww	$0.48
J1	USB4215-03-A_REVA	1	3	Digikey	https://ww	$1.73
R8	309k->316K	1	10	Digikey	https://ww	$0.06
R9	302k->309K	1	10	Digikey	https://ww	$0.06
R10,R11	100k	2	10	Digikey	https://ww	$0.06
R12	3.4k	1	10	Digikey	https://ww	$0.09
R14,R16	9.76k	2	10	Digikey	https://ww	$0.07
R15,R17	19.8k	2	10	Digikey	https://ww	$0.66
S1,S2	PEC11R-4220F-S0024	2	5	Digikey	https://ww	$9.45
U3	LM27762DSST	1	3	Digikey	https://ww	$7.26
U4	MCP4922-E_SL	1	3	Digikey	https://ww	$10.41
U5	OPA2192QDGKRQ1	1	2	Digikey	https://ww	$11.10
U6	TLV9061xDBV	1	3	Digikey	https://ww	$1.83
F1	PTC RESET FUSE 6V 1A	1	3	Digikey	https://ww	$0.87
D1, D8	TVS DIODE 6VWM 15.6V(	2	10	Digikey	https://ww	$1.17

Figure 10.1 Excel Sheet of ordered components from Digikey

Additional components are sourced from the ECEB Supply Center (eShop) and self-service laboratory inventory, which are provided to students at no direct cost for course projects. Based on the quantities shown in the bill of materials, the estimated retail value of components obtained from eShop, including passive components, pushbuttons, LEDs, regulators, protection devices, and the ESP32 module, is approximately $20-30. Self-service laboratory items, including BNC connectors and pin headers, have an estimated value of $8-14. While these parts do not incur direct out of pocket expense, their estimated value is included to reflect the true material cost of the project.

Reference	Value	Qty	Bought Qty	Location
C1,C24	22uF	2	6	Eshop
C2,C7	1uF	2	6	Eshop
C3,C12,C15	10uF	3	15	Eshop
C10	4.7uF	1	3	Eshop
C11,C13,C25	0.1uF	3	15	Eshop
C14,C16,C17	0.01uF	6	25	Eshop
D2,D3,D4,D5,	LED	5	15	Eshop
D7	SP0503BAHTG	1	3	Eshop
J2,J3	BNC	2	4	Self-Service
J4	Conn_01x05_Pin	1	3	Self-Service
J6	Conn_01x03_Pin	1	3	Self-Service
R1,R2,R13,R2	10k ohm	13	30	Eshop
R3,R4	22 ohm	2	6	Eshop
R6,R7	5.1k	2	6	Eshop
R18,R19	47 ohm	2	6	Eshop
R31,R32,R33,	330 ohm	5	15	Eshop
SW1,SW2,SW	SW_Push	6	12	Eshop
U1	ESP32-S3-WROOM-1	1	3	Eshop
U2	AZ1117CD-3.3TRG1	1	3	Eshop
D9, D10, D11	CDBA540-HF (DO214AC)	3	10	Eshop
D12	82400102 TVS 5VWM 7.7V(	1	3	Eshop

Figure 10.2 Excel Sheet of ordered components from the Eshop and Self-Service at the ECEB

Mechanical components, including any enclosure or mounting hardware, are fabricated using 3D printing filament. The estimated filament usage for the project is minimal (well under 0.5 kg), resulting in an approximate material cost of $5-10, depending on filament type and print density.

Laboratory equipment such as the Tektronix 2225 oscilloscope, bench power supplies, and standard BNC cables are existing ECE laboratory resources and are not included in the project's bill of materials. These items are required for testing and validation, but do not represent direct project expenses.

Overall, the total estimated hardware cost for the project remains under approximately $95-105, excluding laboratory equipment. This is calculated by adding all the estimated costs together: $58.83 + $25 + $10 + $7 = $100.38.

3.1.3 PCB Cost Analysis

The printed circuit board (PCB) was fabricated through JLCPCB. The board dimensions are less than 100 mm × 100 mm, qualifying for JLCPCB's standard low-cost prototype pricing tier. For a 2-layer FR-4 board with 1 oz copper and standard HASL finish, the base fabrication cost for a small batch (typically five boards) is approximately $5, with total cost including shipping generally in the range of $20-25, depending on shipping method.

Although PCB fabrication was covered by course resources and did not result in additional out-of-pocket expense, the estimated market cost is included here to reflect the true production value of the prototype. When distributed across the batch, the effective per-board fabrication cost is approximately $4-5 per PCB.

3.1.4 Grand Total

Total Estimated Project Value

Material Cost: = $100

PCB Value: = $25

Labor Cost: = $23,201

Grand Total Estimated Project Value: = $23,201

3.2 Schedule

Schedule aligns with the course calendar. Task ownership is shared unless noted.

Week	Task	Owner
Feb 23 to Mar 1	Finalize design document and design review preparation. Submit PCB order and place parts order. Begin firmware skeleton in Arduino.	Josh and Eric
Mar 2 to Mar 8	Design review. Apply feedback. Continue firmware on dev board. Validate SPI and encoder library behavior.	Josh and Eric
Mar 9 to Mar 15	Breadboard demo preparation. Prototype analog mapping if needed. Demonstrate encoder driven output update.	Josh and Eric
Mar 16 to Mar 22	Spring break. Continue firmware work as time allows.	Josh and Eric
Mar 23 to Mar 29	Assemble PCB. Bring up rails. Verify raw DAC outputs. Verify analog mapper outputs. Begin integration.	Josh and Eric

Mar 30 to Apr 5	**Complete base functionality and enclosure planning. Individual progress report.**	**Josh and Eric**
Apr 6 to Apr 12	**Progress demo preparation and testing. Verify R and V checklist items for base functionality.**	**Josh and Eric**
Apr 13 to Apr 19	**Refine firmware and button functions. Print enclosure and integrate.**	**Josh and Eric**
Apr 20 to Apr 26	**Mock demo and mock presentation. Complete verification and record results.**	**Josh and Eric**
Apr 27 to May 4	**Final demo and final presentation. Final report and notebook completion.**	**Josh and Eric**

4. Ethics, Standards, Societal Impact, and Safety

4.1 Societal impact

OscilloSketch improves the accessibility of oscilloscope XY visualization in educational and laboratory environments by providing a portable, purpose-built tool for interactive vector display. Traditional XY mode demonstrations often require signal generators or complex setups, which can limit experimentation. By integrating user input, DAC control, and analog scaling into a single device, the system lowers the barrier to exploring signal processing, coordinate systems, and vector-based visualization.

4.2 Engineering standards

Relevant standards and best practices include USB 2.0 interface practices, USB C connector Relevant engineering standards and best practices include USB 2.0 interface practices, USB-C connector wiring conventions, and ESD protection practices for user-accessible connectors. The design follows USB signal integrity recommendations, including controlled routing of D+ and D− differential pairs, series termination resistors for edge damping, and appropriate transient suppression.

Power-path protection follows established low-voltage design practices, including reverse-current isolation, resettable overcurrent protection (PPTC fuse), and TVS diode placement at connector interfaces. Component selection and layout practices are consistent with manufacturer datasheet recommendations for decoupling, grounding, and analog signal integrity.

4.3 Ethics

This project emphasizes safety, honesty in performance claims, and professional responsibility. Output performance is stated with tolerances and under specified load conditions (e.g., 1 MΩ oscilloscope input). Worst-case error analysis is included to quantify midscale offset and gain variation rather than relying solely on nominal calculations.

The design avoids overstating capabilities and clearly defines operating limits, including output current limits for 50 Ω loads. This approach aligns with the IEEE Code of Ethics by ensuring accurate reporting of system behavior and responsible engineering communication.

4.4 Safety

Electrical safety risks include ESD events at external connectors, accidental shorts at BNC outputs, and improper USB power connections. These risks are mitigated through input current limiting (PPTC fuse), reverse-current protection (Schottky diodes), transient voltage suppression (TVS arrays), output series resistance, and bidirectional clamp protection at user-accessible connectors.

The device operates entirely from low-voltage USB power (5 V input, 3.3 V regulated rails, and ±5 V analog generation) and does not interface directly with mains voltage, significantly reducing electrical hazard risk. All exposed connectors operate at low-voltage levels, minimizing shock risk under normal operating conditions.

5. References

[1] Espressif Systems, ESP32 S3 WROOM Datasheet.

[2] Microchip Technology, MCP4922 Dual 12 Bit DAC Datasheet.

[3] Texas Instruments, LM27762 Regulated Switched Capacitor Inverter Datasheet.

[4] Texas Instruments, OPA2192 Dual Precision Op Amp Datasheet.

[5] Texas Instruments, TLV9061 Op Amp Datasheet.

[6] Bourns, PEC11R Rotary Encoder Datasheet.

[7] Diodes Incorporated, AZ1117C 3.3 V LDO Datasheet.

[8] Tektronix, 2225 Oscilloscope Manual.

[9] IEEE Code of Ethics, IEEE.

[10] Texas Instruments, "Output Voltage Scaling Using Op Amps and Precision Resistors," SLOA097, Mar. 2010. [Online]. Available: https://www.ti.com/lit/an/sloa097/sloa097.pdf

[11] Texas Instruments, "USB Power Delivery Controller Solutions Technical Reference," SLYY228, 2021. [Online]. Available: https://www.ti.com/lit/eb/slyy228/slyy228.pdf