Acoustic Stimulation to Improve Sleep

ECE 445 Design Document - Spring 2026

Project #18
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1. Introduction

This project addresses the engineering challenge of designing a low-cost, wearable, closed-loop sleep enhancement system that reliably detects slow wave sleep using electroencephalography (EEG) and delivers precisely timed auditory stimulation to improve sleep quality. This system integrates an EEG headband, custom signal processing hardware, audio output circuitry, power management, and a user-facing application into a compact and comfortable form factor suitable for overnight use. The device performs real-time EEG acquisition and processing, identifies slow wave oscillations, and delivers short bursts of pink noise in phase with the detected brain activity, reinforcing the slow wave oscillations and sleep.

This report details the design, implementation, and verification of the proposed system. Chapter 2 details the overall system architecture and each subsystem, including the EEG front end, digital signal processing pipeline, audio output mechanism, power delivery circuitry, and user application. Chapter 3 analyzes the cost of components and labor. Finally, Chapter 4 summarizes the project's goals and discusses considerations further. Overall, the project demonstrates the feasibility of a practical and affordable closed-loop auditory stimulation device for sleep enhancement.

1.1 Problem

Poor sleep quality affects a large portion of the population, particularly older adults and individuals with sleep disorders, and is often associated with insufficient time spent in slow wave sleep (SWS). Slow waves are high-amplitude, low-frequency oscillations observed in cortical EEG activity that reflect synchronized neuronal firing and define the deepest stage of non-REM sleep. Adequate time spent in slow wave sleep is critical for memory consolidation, cognitive performance, and overall neurological health.

Prior research has demonstrated that closed-loop auditory stimulation can enhance slow wave sleep by reinforcing endogenous slow wave oscillations through precisely timed acoustic stimuli. However, existing research-grade and commercial systems capable of performing closed-loop EEG-based stimulation are typically expensive, bulky, or require clinical-grade hardware, limiting their accessibility for at-home and long-term use. This creates a need for a wearable, user-friendly system that can perform real-time EEG monitoring and stimulation without the cost and complexity of current solutions.

1.2 Solution

This project proposes a wearable, closed-loop sleep enhancement system that detects slow wave sleep using EEG and delivers phase-aligned auditory stimulation to reinforce slow wave activity. The system consists of an EEG headband connected to a custom printed circuit board (PCB) that performs the core functionality of a commercial EEG acquisition platform while also supporting real-time audio output. EEG signals are acquired through dry electrodes, amplified and digitized on-board, and processed in real time to detect slow wave oscillations.

When slow wave activity is detected, the system generates short bursts of pink noise timed to the phase of the oscillation to reinforce it and enhance slow wave sleep. In addition to stimulation, digitized EEG data are transmitted wirelessly to a mobile application, where users can view sleep metrics and historical trends. The system is designed as an integrated, compact, and comfortable device suitable for overnight use, enabling closed-loop sleep modulation outside of a clinical setting.

1.3 Visual Aid

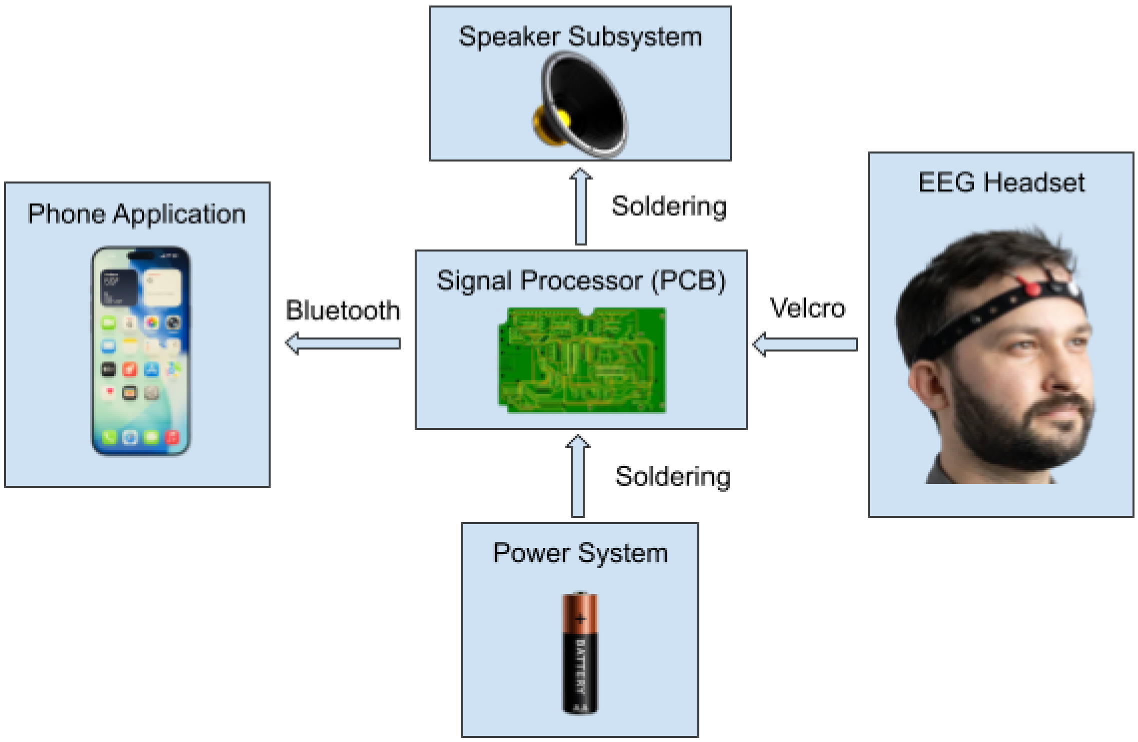

Figure 1. Pictorial representation of the acoustic stimulation system

1.4 High-Level Requirements List

The system shall detect slow wave activity in EEG signals in real time with sufficient robustness to noise - less than 10% signal artifact over an 8-hour night - and deliver phase-aligned auditory stimulation within 300ms of slow-wave detection and under 50dB.

The device shall operate continuously for a full night of sleep (at least 10 hours) while remaining comfortable and safe for overnight wear.

The system shall wirelessly transmit single-channel EEG-derived data to a mobile application, enabling users to view sleep stage information and historical sleep trends.

2 Design

2.1 Block Diagram

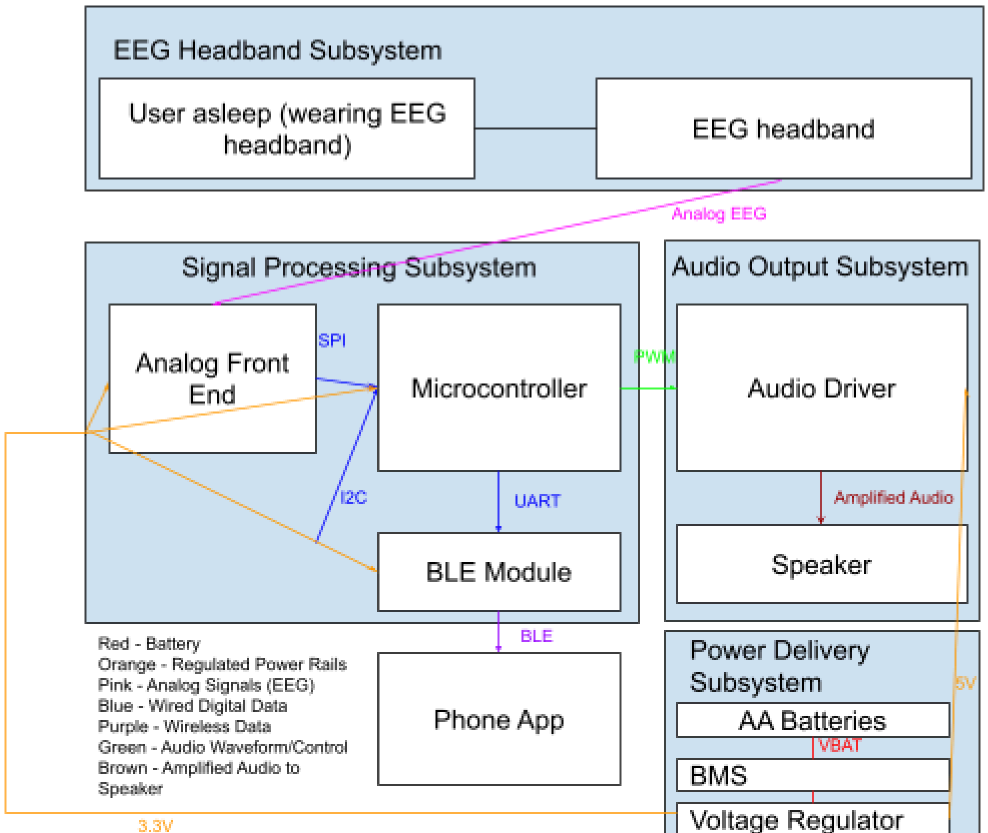

Figure 2. Block diagram of the system

2.2 Wearable Headband

2.2.1 EEG Headband

We will be using a commercially available EEG Headband, the OpenBCI EEG Headband Kit. This includes the headband, electrodes, and cables carrying the analog signal. It will be directly connected to the PCB which has the signal processor, audio system and power systems through velcro.

Table 1 - R&V for EEG Headband subsystem

Requirement	Verification Procedure	Equipment	Data / Presentation
User Comfort: At least 80% of test participants (≥8 out of 10) shall report that they would be willing to wear the headband for 30	1. Recruit a minimum of 10 participants. 2. Have each participant wear the full device (headband + attached PCB via Velcro) for 30 minutes while seated.	Printed or digital survey form, timer	Table of participant responses; calculated average comfort score and reuse

minutes and use it again, with an average comfort rating of ≥ 3.5 / 5 on a standardized Likert scale.	3. After use, administer a standardized survey including: (a) 1–5 comfort rating, (b) yes/no willingness to use again. 4. Compute average rating and percentage willing to reuse.		percentage
Signal Integrity After Integration: When connected to the PCB and secured via Velcro, the EEG signal amplitude shall remain within ±10% of baseline amplitude measured before PCB attachment during a 2-minute resting recording.	1. Record baseline EEG signal (eyes closed, seated) for 2 minutes using headband alone. 2. Attach PCB via Velcro and repeat 2-minute recording under identical conditions. 3. Compute RMS amplitude of signal in both cases. 4. Compare percentage difference.	EEG acquisition software (OpenBCI GUI), analysis software (MATLAB/Python)	Table of RMS amplitudes; calculated percent difference

2.2.2 Signal Processor

The Signal Processing Subsystem performs EEG acquisition, digitization, and real-time slow-wave detection, with the core architecture of the OpenBCI Cyton board serving as reference while reducing channel count to one and replacing the RFduino radio with an MDBT42Q-P192KV2 Bluetooth Low Energy (BLE) module. This subsystem directly satisfies the high-level requirement of detecting slow-wave activity and generating phase-aligned stimulation within 300 ms.

Differential EEG signals from the headband (1–100 microVolts) are routed to a Texas Instruments ADS1299 analog front end for amplification and digitization. Each channel of the ADS1299 includes a high-input-impedance differential programmable gain amplifier (gain set to 24), which amplifies the microvolt-level signal while suppressing environmental noise. The amplified signal is then converted using an integrated 24-bit delta-sigma ADC, which oversamples and digitally filters the signal to achieve low noise and high resolution suitable for biomedical signals. EEG data are sampled at 250 Hz for one active 24-bit channel and transmitted to the PIC32MX250F128B microcontroller over an SPI interface, with all unused ADS1299 channels powered down to reduce power consumption. The ADS1299's DRDY (data ready) signal is used as an interrupt source to ensure deterministic sampling intervals for the active EEG channel.

The PIC32 microcontroller performs digital filtering and feature extraction in real time. Firmware implements a 60 Hz notch filter to suppress power line interference and a 0.5-4 Hz bandpass filter to isolate slow-wave activity. Phase estimation and threshold-based slow-wave detection are executed on buffered EEG windows, producing a stimulation trigger signal with temporal resolution ≤10 ms.

Processed EEG samples are transmitted from the PIC32MX250F128B to the MDBT42Q-P192KV2 BLE module over an asynchronous UART interface configured for 8-N-1 framing at a validated baud rate (≥115200 bps). Because the design has been simplified to a single EEG channel sampled at 250 Hz with 24-bit resolution, the sustained raw data rate is then:

$$250\ samples/s \times 3\ bytes/sample \approx 750\ B/s$$

This is well within UART's conservative 11.5 kB/s estimate and BLE's conservative 10 kB/s estimate. Data is packetized into fixed-length binary frames to ensure clean parsing and loss detection. Each frame contains: (1) a protocol version byte, (2) a 16-bit monotonically increasing sequence number for drop detection, (3) a 32-bit millisecond timestamp derived from the ADS1299 data-ready interrupt count, (4) a block of N consecutive 24-bit signed samples for the single channel, and (5) an optional 16-bit CRC for UART-level integrity checking. The sequence number and timestamp allow the BLE module and mobile application to detect missing frames and reconstruct uniform sample timing independent of wireless packet boundaries. BLE is used strictly as a transport layer; application-level framing and timing are handled by this UART-defined data structure to maintain stream consistency and simplify debugging.

Table 2 - R&V for Signal Processing subsystem

Requirement	Verification Procedure	Equipment	Data / Presentation
A/D conversion: The signal processing subsystem shall digitize 1 EEG channel at 250 Hz producing 24-bit signed digital output samples.	1) Configure ADS1299 for 250 SPS and intended PGA gain. 2) Inject a known differential sine (ex. 1 Hz, 10 Hz) at varying amplitudes 1 mV, 10 mV, and 50 mV using a signal generator. 3) Log raw samples and check DRDY frequency and sample word length/format	Function generator (or DAC), resistor divider/attenuator, oscilloscope, PC logger (Python/MATLAB).	Table with measured DRDY frequency, plots of injected vs recorded waveform
Artifact Suppression: Over an 8-hour recording, the subsystem shall exhibit < 10% artifact-contaminated data. An artifact is defined as samples flagged by ADC saturation or lead-off detection.	1) Run an 8-hour overnight recording with the full system enabled. 2) Log raw EEG, lead-off status bit. 3) Compute artifact fraction = (time flagged artifact) / (total time). 4) Repeat for at least one additional trial if feasible.	Fully assembled device, PC/phone receiver + logging software, analysis script, optional accelerometer calibration jig.	Timeline plot showing artifact flags over 8 hours, excerpt plots (EEG segment before/during/after artifact).
SWS/NREM detection performance: Firmware	1) Use a fixed, pre-labeled dataset (ground truth NREM labels per epoch).	Pre-labeled dataset, PC	Confusion matrix +

shall classify >85% of NREM sleep epochs on pre-labeled data using 1 EEG channel sampled at 250 Hz, measured as accuracy ≥ 85% on a test set.	2) Run the exact embedded algorithm (or equivalent implementation) on the dataset. 3) Log predicted labels per epoch. 4) Compute accuracy, precision/recall for NREM.	Running evaluation script; firmware build or compiled reference implementation producing predictions.	Accuracy table, brief description of dataset split (train/validation /test) and number of epochs.
Closed-loop timing output to audio system: The subsystem shall output a detection event and stimulation timing signal such that the audio subsystem can begin modulation ≤ 300 ms after slow-wave detection.	1) Feed a synthetic slow-wave waveform (known phase landmarks) into the ADS1299 input. 2) Capture the detection output GPIO and the audio-enable GPIO (or UART event timestamp) on a logic analyzer.	Function generator/DAC, logic analyzer or oscilloscope, PC logger.	Histogram of measured latencies; GPIO timing showing event alignment.

2.2.3 Audio System

The audio output subsystem converts stimulation timing decisions from the microcontroller into precisely timed audible pink noise delivered through a speaker. The microcontroller produces a low-power digital audio waveform (PWM-encoded pink noise) at the desired phase. An audio driver/amplifier stage converts the low-power waveform into a speaker-level signal with sufficient current and voltage swing. This subsystem enables the closed-loop functionality of the system through auditory stimulation.

Table 3 - R&V for Audio Output Subsystem

Requirement	Verification Procedure	Equipment	Data / Presentation
Stimulation Latency: The time delay between the microcontroller trigger signal and the onset of audible output shall be ≤ 20 ms under nominal supply voltage (3.3 V ±5%) at 20–30°C.	1. Configure firmware to output a digital trigger pin simultaneously with PWM enable. 2. Connect oscilloscope Channel 1 to trigger pin and Channel 2 to amplified audio output (across 8 Ω load). 3. Measure time between trigger rising edge and first audio waveform exceeding 10% of peak amplitude. 4. Repeat for 10 trials.	Oscilloscope (≥100 MHz), 8 Ω dummy load	Oscilloscope screenshot with measured Δt; table of 10 delay measurements

Timing Jitter: The variation in stimulation onset timing shall be ≤ ±5 ms from the mean delay over 100 consecutive trigger events.	1. Generate 100 consecutive stimulation triggers. 2. Measure trigger-to-audio delay using oscilloscope persistence/storage mode. 3. Record all delays and compute mean and maximum deviation.	Oscilloscope (storage mode)	Table of delays; calculated mean and max deviation
Output Sound Pressure Level (SPL): The speaker shall produce 50 dB SPL ±2 dB measured at 10 cm distance in ambient noise <40 dB during continuous stimulation.	1. Place a calibrated SPL meter 10 cm directly in front of the speaker. 2. Enable continuous pink noise output. 3. Record SPL for 10 seconds and compute the average value. 4. Repeat 3 trials.	Calibrated SPL meter	Table of measured SPL values and average

2.2.4 Power system

The power subsystem is responsible for providing stable, safe, and efficient power to all system components, including the microcontroller, EEG acquisition circuitry, and audio output stage. The system is powered by four AAA batteries connected to the PCB.

The overall system is powered by four AA batteries, providing approximately 6 V DC, which is regulated down to the required 3.3 V digital supply and ±2.5 V analog rails, powering the ADS1299, the PIC32 microcontroller, and the wireless communication module. The regulator is selected to maintain output within ±5% under dynamic load conditions while minimizing output ripple to prevent noise coupling into the EEG front-end and audio circuitry.

Power integrity and safety are prioritized through the inclusion of output decoupling capacitors for transient suppression, and ideal component placement ensures effective dissipation of heat, ensuring that the PCB surface temperature remains within safe limits for wearable use.

Table 4 - R&V for Power subsystem

Requirement	Verification Procedure	Equipment	Data / Presentation
Regulated Output Voltage: The power system shall provide a regulated output of 5 V ±5% (3.3V for the digital supply) for load currents from 0–500 mA, with peak-to-peak ripple ≤ 50 mV under	1. Connect adjustable electronic load to 5 V (3.3 V for digital supply) rail. 2. Sweep load current from 0 mA to 500 mA in 100 mA increments. 3. Measure DC voltage using DMM at each step. 4. Measure ripple using oscilloscope (AC-coupled, bandwidth limit 20 MHz).	DC power supply (battery simulator), electronic load, DMM, oscilloscope	Table of Vout vs. load current; oscilloscope screenshot of ripple

nominal battery voltage (~6 V).			
Thermal Performance: During continuous system operation at maximum load (500 mA), PCB surface temperature shall not exceed 40°C ±2°C in ambient conditions of 20–25°C.	1. Operate the full system at maximum load for 30 minutes. 2. Measure hottest PCB location using IR thermometer or thermal camera. 3. Record ambient temperature.	IR thermometer or thermal camera, thermometer	Table of ambient temp and max PCB temperature

2.3 Data analysis

2.3.1 User-facing Application

To improve usability, the User-Facing Application will give the end user insights into their sleep. Specifically, we aim to analyze the user's slow-wave sleep and how the system is processing that data to output audio throughout the night.

We can use a React Native frontend for compatibility with Android and iOS. We can run lightweight ML models on-cloud to determine the state of sleep (using libraries like FFT and bandpower). For the backend, Firebase can be used to store our data, which will come in via Bluetooth.

To be more specific, the application will follow this implementation path:

1. Bluetooth data ingester (following defined data frame).
2. Store data to be used later.
3. Visualize the data (before or after processing).

The application will follow standard UI/UX practices common in 2026, prioritizing data visualizations for everyday users.

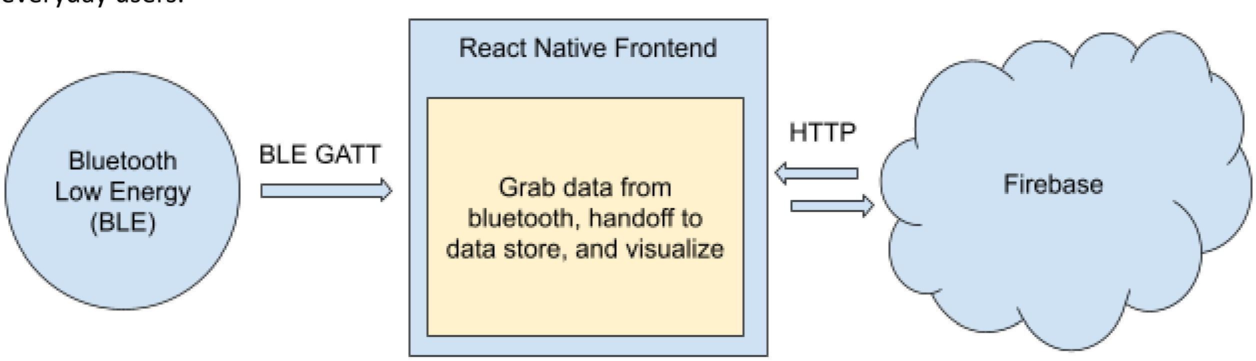

Figure 3. Block diagram of the mobile application.

Table 5 - R&V for User-Facing Application

Requirement	Verification Procedure	Equipment	Data / Presentation
Sleep Stage Classification Accuracy: The on-device sleep classification algorithm, using a single EEG channel, shall achieve ≥ 75% overall accuracy ±3% when compared against labeled reference sleep data over a minimum of 8 hours of recorded data. Accuracy is defined as (correct stage predictions / total predictions).	1. Obtain labeled sleep dataset (reference-labeled epochs). 2. Run implemented ML model on the same dataset. 3. Compare predicted sleep stages (Wake, REM, Light, Deep) to ground truth labels. 4. Compute overall accuracy and confusion matrix.	Laptop/PC, Python environment, labeled dataset	Table of predicted vs. actual labels; confusion matrix; calculated accuracy
Data Latency & Visualization Update: The application shall display updated sleep stage information within ≤ 5 seconds ±1 second of receiving EEG data via Bluetooth under normal operating conditions (WiFi/cellular available, stable BLE connection).	1. Transmit timestamped EEG packet from device. 2. Log reception time in the app. 3. Measure time until the updated sleep stage is visible in the UI. 4. Repeat for 20 transmissions.	Smartphone (Android/iOS), stopwatch or internal timestamp logging	Table of latency measurements; calculated mean and maximum latency

2.4 Tolerance Analysis

The effectiveness of closed-loop auditory stimulation depends on delivering pink noise bursts at a specific phase of the slow-wave oscillation. Variations in signal processing latency, sampling rate, and computational delay may result in phase errors that reduce stimulation efficacy.

Slow-wave sleep oscillations typically occur for a frequency of about 1 Hz. With that assumption:

$$T = 1/f = 1s$$

To maintain effective phase locking, the stimulus must be delivered within ±45° of the target phase, corresponding to a timing tolerance of:

$$\Delta t = 45°/360° \times T = 0.125s$$

The estimated latency consists of EEG sampling delay (~10ms), signal processing (~40ms), microcontroller processing (~20ms) and audio driver latency (~10ms). This is ~80ms in total meaning this requirement should be feasible to satisfy.

3. Cost and Schedule

3.1 Cost Analysis

3.1.1 Labor

Assuming a $50 hour wage and an average of 8 hours of work per week over 10 weeks, this is the sum of our labor costs:

$$\$50/hour\ x\ 2.5\ x\ 80\ hours\ x\ 3\ persons\ =\ \$30,000$$

3.1.2 Parts

Table 6 - Electronics Parts Costs

Part	Manufacturer	Retail Cost ($)	Bulk Purchase Cost ($)	Actual Cost ($)
OpenBCI EEG Headband Kit	OpenBCI	349.99	349.99	0
ADS1299 AFE	Texas Instruments	73.3	32	73.3
PIC32MX250F128B	Microchip	5.22	3.8	5.22
MDBT42Q-P192KV2 Bluetooth	Nordic Semiconductor	5.78	5.3	5.78
TL082CP Op-Amp	Texas Instruments	1.55	1.55	1.55
Resistor Pack (COM-10969)	SparkFun	9.95	9.95	2
Capacitor (75-562R5HKD10)	Vishay	2.47	0.89	2
Capacitors (330820)	Kemet	0.14	0.07	2
Speaker AST03008MRR	PUI Audio	3.67	1.86	3.67
MCP1700 Regulator	Microchip	0.51	0.48	0.51
AA Batteries	Energizer	0.62	0.34	0.62
On/Off Button (TBD)	--	2.85	2.1	2.85
MCP4822 DAC	Microchip	4.28	3.24	4.28
PAM8302 Audio Amplifier	Diodes Incorporated	0.5	0.23	0.5
Total		**460.83**	**411.8**	**104.28**

Table 7 - Software Components Costs

Part	Manufacturer	Retail Cost ($)	Bulk Purchase Cost ($)	Actual Cost ($)
React Native	Same Sky	0.00	0.00	0.00
Firebase	Google	0.00	0.00	0.00
FFT / ML Libraries	Open source	0.00	0.00	0.00
Total		**0.00**	**0.00**	**0.00**

3.1.3 Total

The total would thus be as follows:

$$\$30,000 \; + \; \$104.28 \; = \; \$30,104.28$$

3.2 Schedule

Table 8 - Tentative schedule of design project

Week	Task	Person
Feb 23 - 27	Write up the design document	Everyone
	Order parts for prototyping	John
Mar 2 - 6	Design the first iteration of the PCB and order it (EEG Headband + ADS1299 + PIC32 to just view brain signals).	Sid
	Attend Design Review	Everyone
	Use PCB prototype 1 to build and test just the power delivery subsystem	Everyone
Mar 9 - 13	Design the second iteration of the PCB and order it (EEG Headband + ADS1299 + PIC32 + Battery Power)	John
	Attend Breadboard Demo	Everyone
	Submit Teamwork evaluation I	Everyone
	Use PCB prototype 2 to build and test just the signal processing subsystem (independent of the power delivery subsystem)	Everyone
Mar 23 - 27	Design the third iteration of the PCB and order it (EEG Headband + ADS1299 + PIC32 + Battery Power + Audio System + Bluetooth module)	Everyone
	Write code to process digital signals and generate pink noise	Bakry
	Use PCB prototype 3 to build and test the audio driver subsystem	Everyone
Mar 30 - Apr 3	Submit Individual progress reports	Everyone
	Use final PCB prototype 4 to build the full system and test	Everyone
	Write code for the user-facing application and test	John
Apr 6 - 10	Submit Team Contract Assessment	Everyone

	Attend Progress Demo	Everyone
Apr 13 - 17	Debug, test and reiterate building as needed	Everyone
Apr 20 - 24	Demo working prototype to TA in mock Demo	Everyone
Apr 27 - May 1	Demo working final design in Final Demo	Everyone
May 4 - 8	Submit Final Papers	Everyone
	Checkout from Lab with TA	Everyone
	Finalize notebooks for submission	Everyone

4. Societal Impact, Engineering Standards, Ethics and Safety

4.1 Societal Impact

4.2 Engineering Standards

The design approach follows general IEEE and ACM codes of ethics by prioritizing user safety, honest reporting of results, protection of user data, and clear communication of limitations. Electrical design practices follow low-voltage wearable device norms and standard PCB safety practices to reduce risk of shock, overheating, or short circuits.

4.3 Ethics

This project involves a wearable EEG-based device that monitors brain activity and delivers auditory stimulation during sleep. Because it interacts with users' physiological signals and sleep behavior, ethical considerations related to safety, privacy, transparency, and responsible use are important.

4.3.1 Data Privacy and Security

The device collects EEG-derived data and sleep metrics, which qualify as sensitive biometric information. Ethical handling of this data requires minimizing collection to only what is necessary, using secure wireless transmission, and storing data in protected application storage. If cloud services are used, access controls and encryption should be enabled. Users should be informed what data is collected and how it is used. No data should be shared with third parties without explicit consent.

4.3.2 Transparency and Informed Use

Consistent with IEEE and ACM ethical principles, the system should be described accurately with no exaggerated claims about performance or health benefits. Users must be informed about limitations in sleep-stage detection accuracy and stimulation effectiveness. Known uncertainties and error rates should be disclosed so users can make informed decisions about use.

4.3.3 Bias and Performance Limitations

Sleep detection algorithms may perform differently across users due to physiological variability, electrode placement, or noise. Ethical deployment requires acknowledging that performance may not generalize equally to all users and avoiding claims of universal effectiveness. Future validation across diverse users is recommended.

4.4 Safety

The system is designed to be non-invasive and low-risk, using dry EEG electrodes and low-voltage battery-powered electronics. Audio stimulation levels are constrained to remain within safe listening thresholds to avoid hearing damage or negative sleep disturbance. The device is not intended to diagnose or treat medical conditions, and all documentation and user-facing materials will clearly state that it is a prototype research device and not a certified medical product. This avoids misleading users or encouraging unsafe medical reliance. Additionally, the system is designed in accordance with FCC Part 15 regulations for electromagnetic emissions and FCC OET Bulletin 65 guidelines for safe human exposure to radiofrequency energy [6], [7].

5. Citations

[1] OpenBCI, “OpenBCI EEG Headband Kit.” [Online]. Available: https://shop.openbci.com/products/openbci-eeg-headband-kit. [Accessed: Feb. 23, 2026].

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[6] Federal Communications Commission, *“Code of Federal Regulations, Title 47, Part 15 – Radio Frequency Devices.”* [Online]. Available: https://www.ecfr.gov/current/title-47/part-15. [Accessed: Feb. 24, 2026].

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