OscilloSketch

Handheld XY Etch-a-Sketch Signal Generator

for Oscilloscopes

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1. Introduction

1.1 Problem

Oscilloscope XY mode enables visualization of two-dimensional signals and vector-style graphics by mapping two analog voltages to horizontal and vertical deflection. While powerful, interactive control of XY mode typically requires multiple laboratory instruments or improvised embedded setups that are not portable, not purpose-built, and often electrically unsafe. Improper signal scaling, unstable timing, or lack of output protection can lead to poor visualization quality or potential damage to oscilloscope inputs.

There is currently no simple, handheld, dedicated controller designed specifically to generate safe, stable bipolar X/Y signals for oscilloscope XY mode while providing intuitive user interaction. Producing clean vector graphics requires careful mixed signal design, including digital to analog conversion, deterministic timing, bipolar analog output conditioning, and protection against misuse.

This project improves accessibility of XY visualization in educational and laboratory settings while emphasizing safe interfacing practices and robust mixed signal design.

1.2 Solution

We will design and fabricate a handheld embedded device that connects directly to an oscilloscope's CH1 and CH2 inputs and generates bipolar X and Y voltages for XY mode. The device functions like an Etch-a-Sketch, using two rotary encoders to control the cursor position, enabling continuous line drawing on the oscilloscope display. The system will be powered via USB-C and packaged in a compact, 3D-printed enclosure for portability and ease of use.

At a system level, a microcontroller will read user inputs and generate SPI signals that are converted into two synchronized analog voltages using a dual-channel DAC. These voltages will be conditioned by an analog output stage that level shifts and amplifies the signals to produce clean bipolar outputs suitable for oscilloscope XY mode operation. Dedicated power regulation circuitry will provide stable digital and analog supply rails, and output protection components will ensure safe connection to laboratory equipment. The design emphasizes signal integrity, deterministic timing, and low-noise analog performance to create a responsive and visually stable drawing experience.

The stretch goals would include a vector-rendered demo mode that would automatically draw preprogrammed shapes or animations by streaming X and Y coordinate paths to the DACs, showcasing analog output without user input. Optional Z-axis blanking would control the oscilloscope's intensity input to turn the beam off while repositioning, preventing unwanted connecting lines.

1.3 Visual Aid

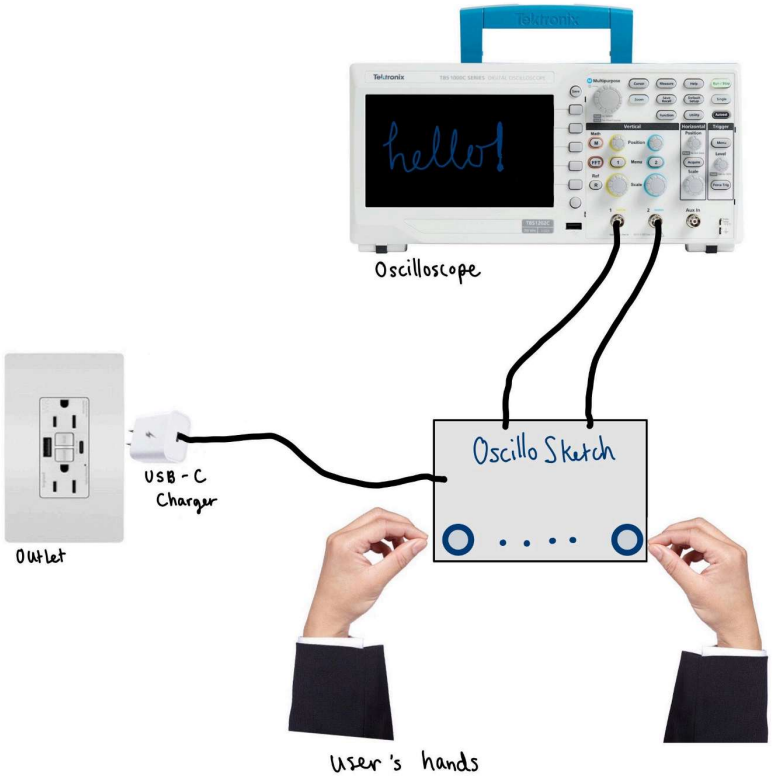

Figure 1. Application of the OscilloSketch device. The system is powered via USB-C and outputs analog X and Y voltages to an oscilloscope operating in XY mode. The user controls the position using the 2 rotary encoders.

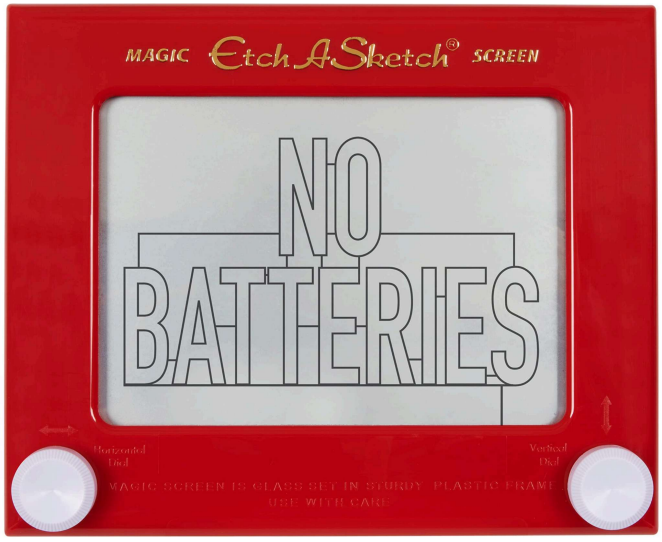

Figure 2. Traditional Etch-a-Sketch toy. This children's drawing device inspired the OscilloSketch concept, where two knobs control horizontal and vertical motion to create continuous line drawings.

1.4 High-level requirements

1. The system shall generate two independent, continuous analog output voltages with a minimum resolution of 12 bits and a voltage range of about ±5 V, for visualization in oscilloscope XY mode.

2. The system shall operate entirely from a single 5 V USB-C connection, consuming no more than 500 mA while supporting both device power and firmware programming.

3. The system shall update both DAC channels at a minimum of 10,000 coordinated X–Y points per second while continuously reading the rotary encoders, so cursor motion appears smooth and free of visible stepping on the oscilloscope.

2. Design

2.1 Block Diagram

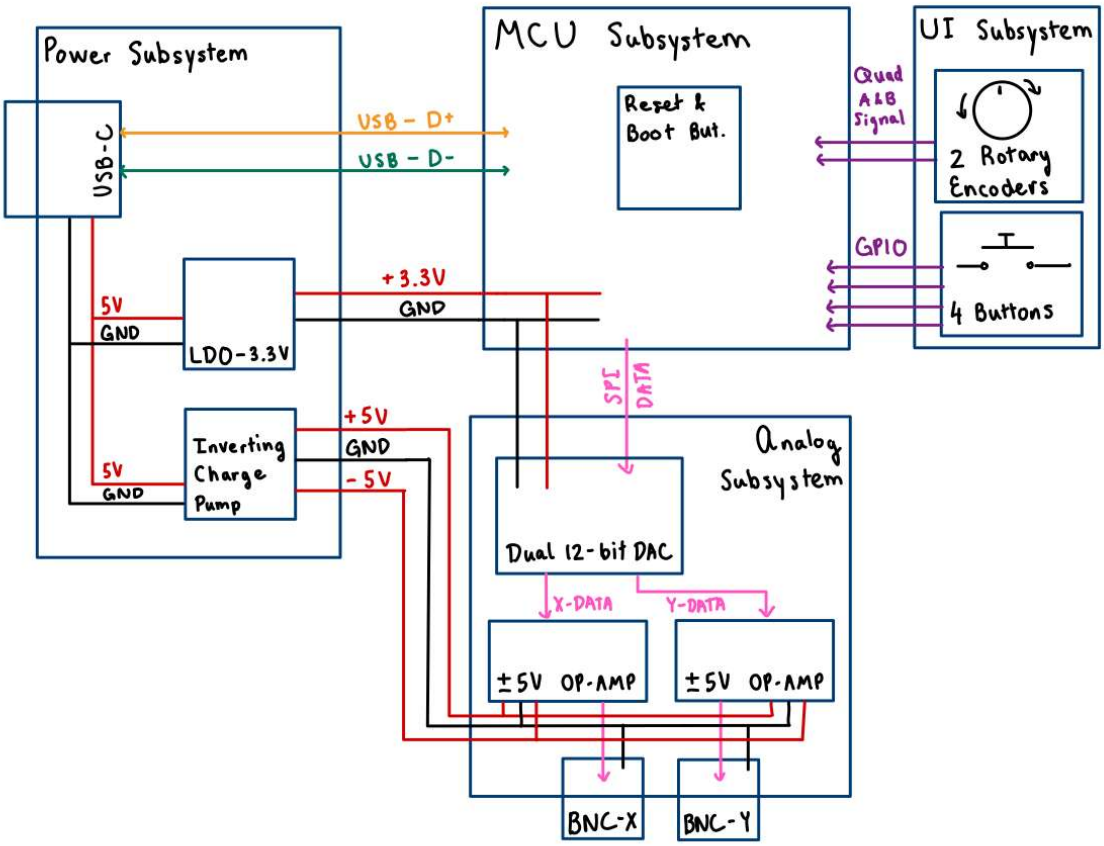

Figure 3. High-level subsystem architecture of the OscilloSketch, illustrating the Power, MCU, UI, and Analog subsystems and their interconnections.

2.2 Subsystem Overview

Subsystem A — User Input / UI

Two incremental rotary encoders provide quadrature PWM A/B signals and push-switch inputs to the ESP32-S3 for X and Y position control. Two dedicated pushbuttons support core functions such as mode selection and clear screen. Two additional buttons are reserved for extended features like demo mode activation or Z-blanking. All signals operate at 3.3 V logic levels and interface directly with MCU GPIO inputs.

Subsystem B — Microcontroller + Firmware

The ESP32-S3 decodes quadrature inputs, debounces switches, maintains X and Y state variables, and updates the dual-channel DAC over SPI. A hardware timer generates periodic interrupts to drive DAC

updates at a fixed rate of at least 10 kS/s per channel, ensuring deterministic output independent of UI processing. The ESP32-S3 is powered from the board's regulated 3.3 V rail provided by an LDO from the USB-C 5 V input, and it is flashed/programmed directly over USB using the ESP32-S3's native USB interface.

Subsystem C — DAC & Analog Output

The MCP4922 dual 12-bit DAC receives SPI commands from the ESP32-S3 and produces two analog output voltages (X and Y). The DAC reference is derived from the regulated 3.3 V rail, so each channel spans 0 to 3.3 V with a resolution of 3.3 V / 4096 = 0.806 mV per LSB. The analog output stage subsequently level-shifts and amplifies this range into a bipolar output suitable for oscilloscope inputs.

The OPA2192 dual op-amp performs both level shifting and amplification of the DAC outputs. It subtracts the midscale voltage (approximately 1.65 V) to center the signal around 0 V, then applies a gain of about 3.0 to convert the internal ±1.65 V span into an output of approximately ±4.95 V suitable for oscilloscope inputs.

Each channel includes a series output resistor sized to enforce current limiting and ensure stability when driving coaxial cables and oscilloscope inputs. For extra protection, protection diodes will be used at the ±5 V rails to clamp the output to safe levels during transients.

Subsystem D — Power Regulation

A USB-C connector provides a nominal 5 V input supply to the system from an outlet.

This 5 V rail feeds a dedicated 3.3 V LDO regulator that powers all digital circuitry, including the ESP32-S3 and MCP4922 DAC, ensuring low-noise and stable operation for logic and reference voltages. The 3.3 V regulator is selected to handle peak ESP32 current transients with sufficient thermal margin, which should be less than 500 mA.

The LM27762 charge pump with integrated LDOs generates regulated ±5 rails to supply the analog output stage, enabling true bipolar signal generation. Local decoupling capacitors are placed at the ESP32, DAC, op-amp, and power device supply pins to minimize noise, voltage ripple, and high-frequency switching disturbances.

2.3 Subsystem Requirements

User Input Subsystem Requirements

- Must provide 3.3 V compatible digital signals.
- Must detect encoder transitions up to at least 2 kHz without missed counts.
- Button latency after debouncing shall be less than or equal to 20 ms.

Microcontroller Subsystem Requirements

- DAC updates must be driven by a hardware timer.

- Sustained update rate must be greater than or equal to 10 kS/s per channel.
- SPI clock must be configured with a margin above the minimum sampling requirement

DAC Requirements

- Must operate in 12-bit mode.
- DAC reference shall be the regulated 3.3 V rail.
- X and Y channels must be updated synchronously within each update cycle.

Analog Output Subsystem Requirements

- Must provide bipolar output swing up to approximately ±5 V under nominal supply conditions.
- DC offset at midscale shall be less than or equal to plus/minus 100 mV at the connector.
- Each channel shall include a series output resistor (approximately 50–100 Ω) to improve stability when driving capacitive loads and to provide fault current mitigation.
- The output stage must remain stable when driving a typical oscilloscope input through a coaxial cable.

Power Subsystem Requirements

- Must accept a nominal 5 V USB input supply.
- The 3.3 V regulator shall be rated for at least 500 mA continuous output current to provide margin for ESP32-S3 peak demand.
- TLDO thermal dissipation must be managed for approximately 0.85 W worst-case power dissipation.
- The LM27762 shall generate regulated ±5 V rails sufficient to support the analog output stage under nominal operating conditions.

2.4 Tolerance Analysis

Risk to project success: The analog output stage must accurately level-shift the DAC's 0–3.3 V output to a bipolar signal centered near 0 V and scaled to approximately ±5 V. Resistor tolerances and op-amp input offset can introduce DC offset at midscale and gain error, which may cause the cursor to drift and reduce usable output swing.

Feasibility analysis (midscale DC offset): When the output voltage is at 0 V, the DAC should be outputting 1.65 V in order to provide both negative and positive swings. This midscale reference is generated using a resistor driver from 3.3V with two equal resistors, which means that mismatching them creates an error in the reference.

Let $R_1 = R$ and $R_2 = R(1 + \epsilon)$, where ϵ is the fractional mismatch. Then:

$$Vmid = 3.3 \cdot \frac{R2}{R1+R2} = 3.3 \cdot \frac{1+\epsilon}{2+\epsilon}$$

Therefore, in order for the output DC offset to remain less than or equal to ±100 mV, the resistor mismatch epsilon must be less than approximately 0.02 (2%). Because the midscale error is amplified by the gain of 3, even small divider mismatches increase the final output offset. Using 1% tolerance resistors limits the worst-case mismatch to approximately 2%, resulting in an estimated output offset of about ±50 mV, which satisfies the ±100 mV requirement. Thus, the design is feasible with standard 1% resistors while maintaining low drift and stable output performance.

3. Ethics, safety, and Societal impact

This project adheres to engineering ethics principles emphasizing safety, honesty, and professional responsibility. Safety considerations include:

- Output current limiting to protect oscilloscope inputs.
- Low-voltage USB power only; no direct mains interfacing.
- Proper labeling of connectors and voltage levels.
- Bench verification of all rails prior to external connection.

We avoid deceptive claims by specifying output swing as “up to plus/minus 5 V under nominal USB supply” rather than implying guaranteed performance under all possible USB sources.

The device improves the educational accessibility of oscilloscope XY visualization and demonstrates responsible mixed-signal engineering practice. Environmental impact is minimal due to low power consumption and a small physical footprint.

4. References

[1] Espressif Systems, *ESP32-S3 Series Datasheet*, Espressif Systems, 2023.

[2] Microchip Technology Inc., *MCP4902/4912/4922 8/10/12-Bit Dual Voltage Output Digital-to-Analog Converter Datasheet*, Microchip Technology Inc., 2018.

[3] Texas Instruments, *OPA2192 Dual, Low-Noise, Precision Operational Amplifier Datasheet*, Texas Instruments, 2022.

[4] Texas Instruments, *LM27762 Low-Noise, Regulated Switched-Capacitor Voltage Inverter Datasheet*, Texas Instruments, 2021.

[5] Texas Instruments, *Understanding and Minimizing DAC Output Errors*, Application Report, Texas Instruments.

[6] Tektronix, *XYZs of Oscilloscopes Primer*, Tektronix, Inc., Application Note.

[7] IEEE, *IEEE Code of Ethics*, IEEE, 2020.