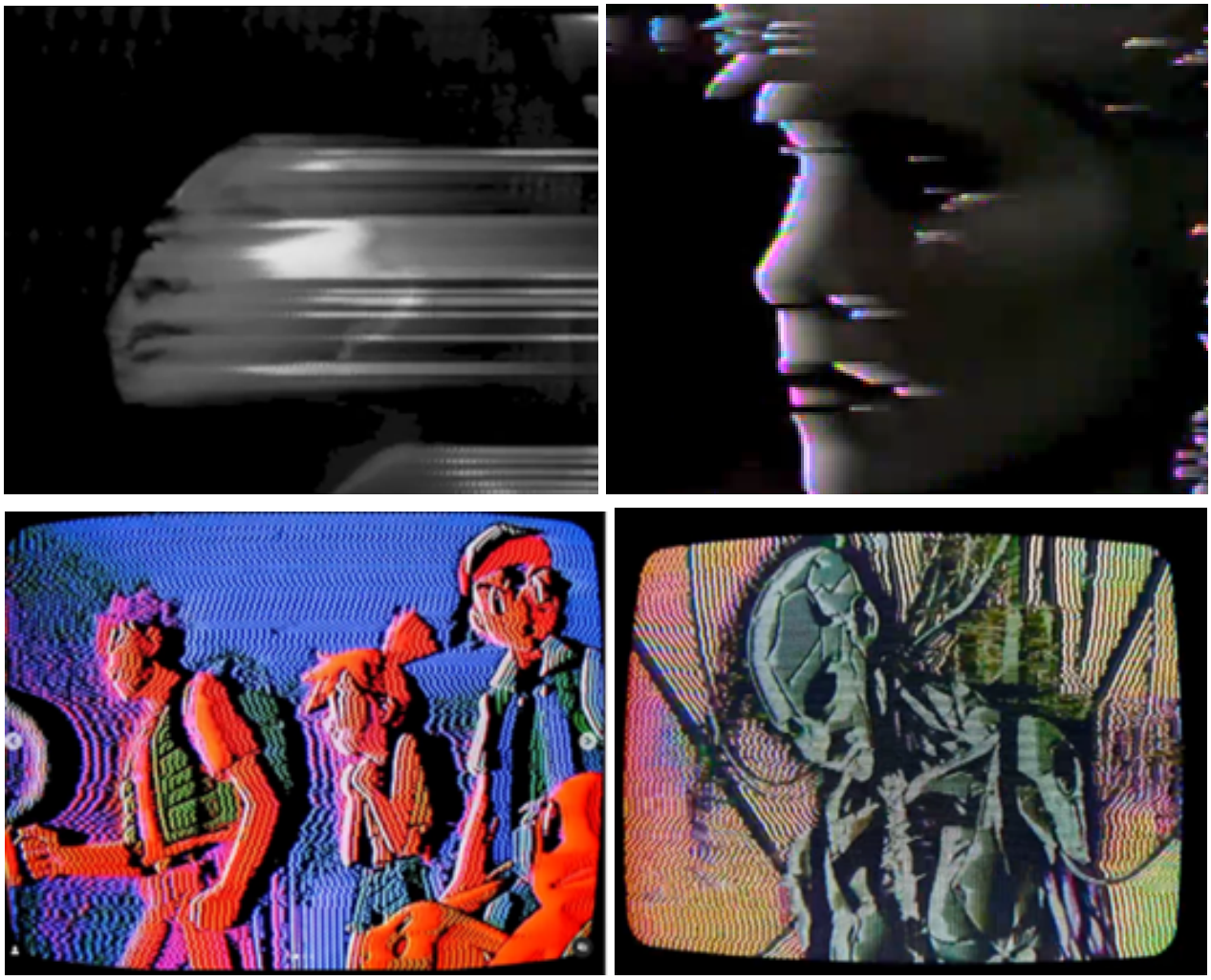
A Modernized Analog Video Distortion Device

ECE 445 Final Report - Spring 2025



Project #16

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Abstract

This document describes the design, implementation, verification, and general technical details of the Televillain, a modernized analog video distortion device. This document also covers the safety and ethical principles put into effect with this project, the cost and schedule followed for this project, and descriptions of the parts used.

Contents

Introduction

1.1 Problem Statement

In recent years, the force of nostalgia has made the aesthetic of analog glitches increasingly popular, and they have found wide use in mediums such as music videos, live concert visuals, video editing, and even film. However, authentic analog glitch devices are made only by a small number of artisans who alter (or "bend") the circuitry of vintage video hardware to introduce these visual artifacts, making them inaccessible to general hobbyist visual artists, such as the VJs who make visuals for house shows on campus.

The cost of a unit generally ranges from $300 to $700, with resold units sometimes reaching over $1,000 [1]. This is due both to the increasing rarity of the hardware they're built from and the small number of people who hand-make these devices. Even after placing an order, the turnaround time can be upwards of 6 months. Additionally, controls on these devices are abstruse, typically consisting of unlabeled switches and potentiometers. This makes operating them confusing and makes them unable to be connected to the often complex visual ecosystem used in VJ-ing (eg. lights, lasers, multiple displays).

The niche nature of this field makes it ripe for innovation, most importantly in the way of making them more accessible to the general artistic community. Live show venues often record performers and audience members live and project the resulting picture in real time against a wall after passing through some sort of video processing algorithm. Sourcing these visual effects requires most venues (such as Gallery Art Bar in Urbana) to hire a third party for the job, which can become expensive [2]. Additionally, most commercial VJs don't offer natural analog effects, the closest being digital emulations of analog effects, which are not always accurate.

The overall goal of this project was to make a robust and easily manufacturable analog glitch device that can be digitally controlled, with an aim towards making them more accessible to hobbyists and people who are interested in analog video. We achieved this by designing video enhancement and distortion circuitry from the ground up using readily available parts and utilizing an MCU to interface with the analog circuitry and provide digital control over parameters of interest. This approach allowed us to simultaneously reduce production costs and expand the functionality of our device compared to other circuit bent video gear on the market.

1.2 High-Level Functionality

To use our device, all that is required is a video input source and output device. Distortion and enhancement of the input video are controlled by the controller block shown in Figure 1. The final processed video signal is sent into a video displayer, either a CRT TV or a digital monitor or projector using an analog video capture card.

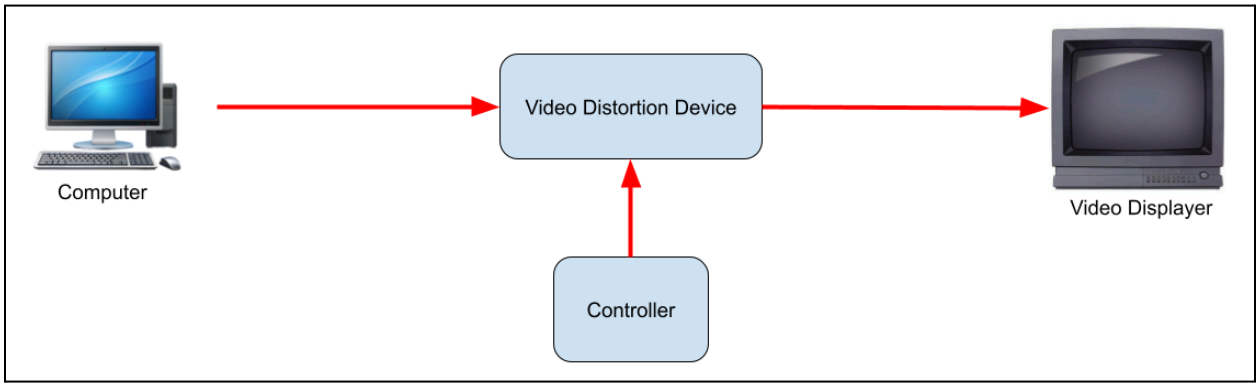


Figure 1: Simplified device interaction diagram

Our design can be divided into four subsystems which form the overall functionality of our device. These subsystems and the way that they interconnect are illustrated in Figure 2. The first subsystem is the controls, which consist of rotary encoders and switches which act as the user interface, and the MCU and DACs which act as the interconnect between the physical controls and analog circuitry. The second subsystem is power, which consists of the +9V barrel connector and +5V and +3.3V regulators which deliver appropriate power signals to the active components on our circuit board. The third subsystem is the enhancer, consisting of passive filters and op-amp amplifiers which enable clean and glitch-free modification of the contrast and saturation of the input video signal. The final subsystem is the distortion stage, which consists of a two-stage variable op-amp filter and amplifier which is the source of the visual artifacts we aim to introduce, such as ringing, rainbowing, ghosting, and tearing (see 2.2.4 for more detail).

Our design has evolved over the course of development, and two main changes were made to the original block diagram in our project proposal. First, we changed our device to require only positive supply voltage by implementing safeguards against 0V signal clipping. We made this change because we could not generate a noise-free negative supply voltage in a timely

manner, and so shifted our design to not be reliant on it. Second, we serialized enhancement and distortion in our final design, whereas we had originally proposed the two to be achieved in parallel. We made this decision because a dedicated clean enhancement stage allowed for subtle changes to the video and a dedicated distortion stage produced more visually appealing glitches.

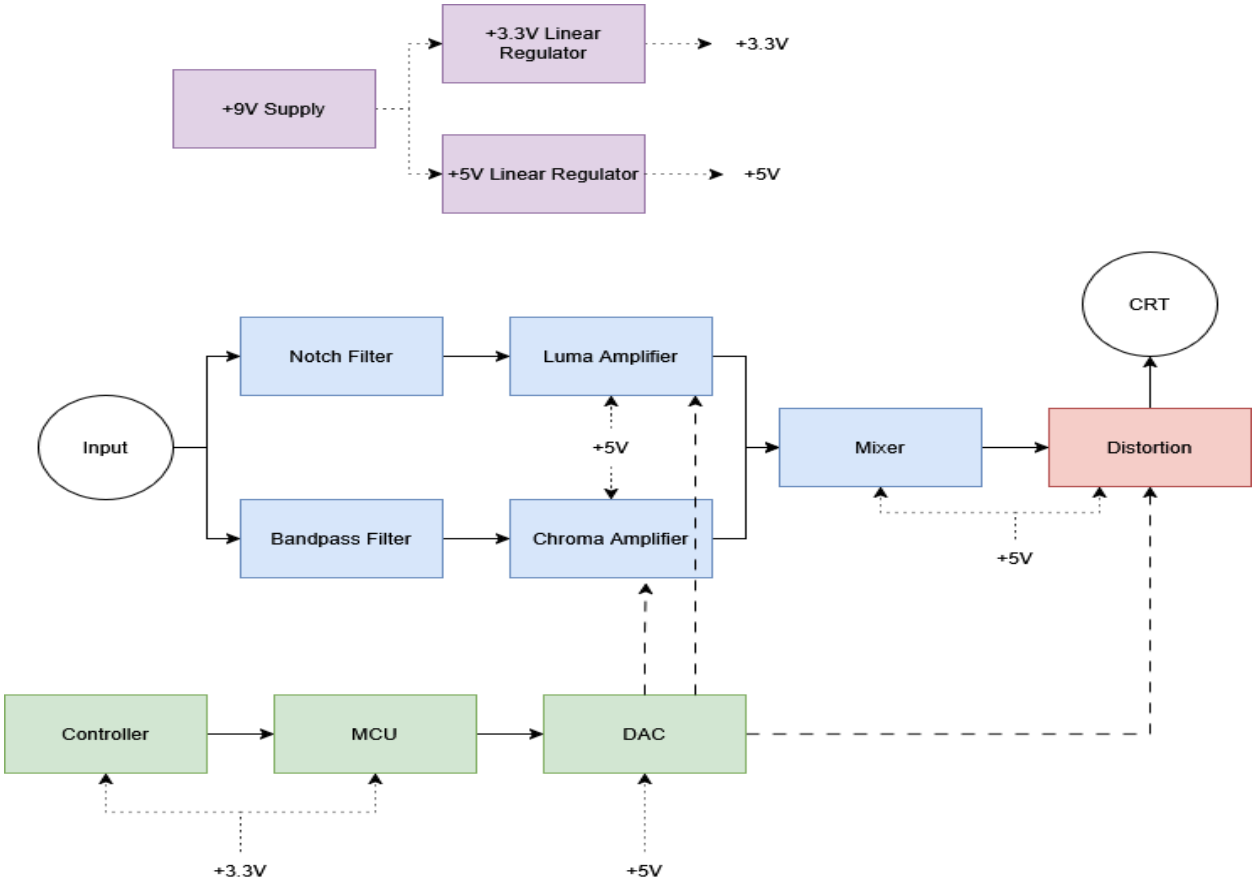


Figure 2: Final device block diagram. Green blocks correspond to the control subsystem, purple to power, blue to enhancement, and red to distortion.

1.3 High-Level Requirements

The following are the high level requirements for our project:

1. The operating frequency range of our bent enhancer circuit must accommodate the full 10MHz bandwidth of the video signal [3].
2. Glitch strength must be able to be varied from suppressed to fully visible via control voltage.
3. Video output must remain within the range of 0V to ~1V to ensure the signal is in-spec with a CRT [3].
4. Sync signals must be preserved and appear with an amplitude of -300mV, unless being intentionally subverted [3].

2 Design

2.1 Functional Overview & Design

2.1.1 Enhancement Subsystem

The video enhancement subsystem is responsible for dividing the video signal into its brightness and color components, amplifying each, and then recombining them. These parameters are digitally controlled via the control subsystem and vactrols. This subsystem also protects the "housekeeping" parts of the signal (sync pulses, color burst) by providing a DC offset so that no clipping of negative voltage occurs. The video distortion subsystem will follow this subsystem (see section 2.2.2). The diagram below shows the block diagram for the enhancer.

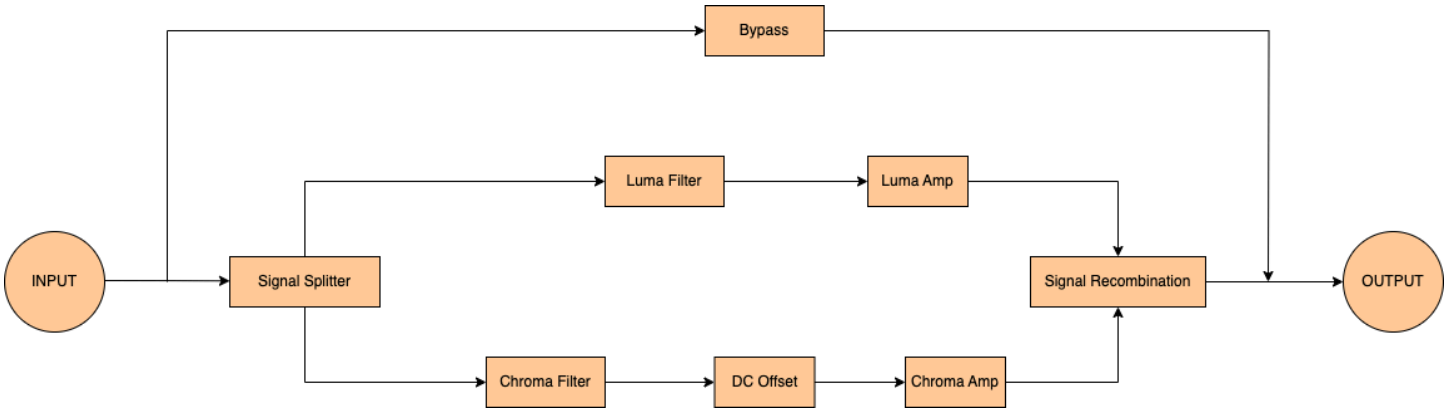


Figure 3: Block diagram of enhancer subsystem.

In this design, we use the LMH6645 voltage feedback amplifiers, chosen for their wide bandwidth. Alternatively, discrete transistors could also have been used to achieve similar results, but we chose to use these devices because of the ease of configuring them and their small footprint.

Components

The signal splitter is made up of two op-amps in a unity-gain buffer configuration in order to properly isolate the signal between both paths. The luma filter is a passive notch filter with a center frequency at 3.58 MHz, which removes the chroma subcarrier centered at that

frequency. The chroma filter is a passive bandpass filter with a center frequency at 3.58 MHz, which removes the luma signal. Post-filter, both the chroma and luma amplifiers use a non-inverting amplifier configuration to boost the signal components according to Equation (1.1). In addition, a small portion of the DC supply voltage is summed with the AC chroma signal according to Equation (1.2) to prevent the signal from being clipped at negative voltages. Finally, the signal is recombined using an op-amp in a non-inverting summation configuration. Because the chroma filter's attenuation is stronger than luma's, this is compensated by adjusting the ratios in which the two signals are summed and then boosting the combined signal according to equation (1.3). Appendix A contains the circuit schematics and component values used, as well as frequency responses of the separation filters.

$$\boxed{1 + \frac{Rvac}{R_2}} \tag{1.1}$$

$$\boxed{\left(1 + \frac{Rvac}{R_3}\right)\left(\frac{R_1}{R_1 + R_2}(9) + \frac{R_2}{R_1 + R_2}V[chroma]\right)} \tag{1.2}$$

$$\boxed{\left(1 + \frac{R_3}{R_4}\right)\left(\frac{R_2}{R_1 + R_2}V[luma] + \frac{R_1}{R_1 + R_2}V[chroma]\right)} \tag{1.3}$$

Verification of this subsystem was the most involved of all of our subsystems. For all tests, we used the standard CRT test pattern, shown in Fig 4. To begin, we verified the performance of our passive filters by viewing their outputs on an oscilloscope. Doing this allowed us to identify attenuation from our filters and thus compensate them. The output of the luma filter and chroma filter can be seen in Fig 5 and Fig 6 respectively. Next, we used the test pattern to verify the performance of our amplifiers. We connected the circuit output to our CRT and debugged the circuit while viewing its output live, which allowed us to diagnose issues such as loading and excessively low input impedance. While we used online tools which could

digitally increase contrast and saturation and compared our outputs against them, we were generally able to visually assess the performance of our amplifiers. More comprehensive requirements and verifications can be seen in Appendix R.1.

Figure 4: The standard CRT test pattern.

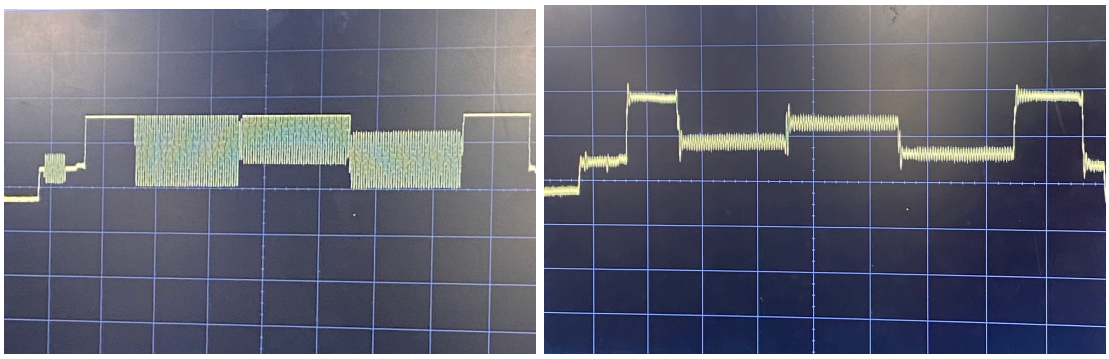


Figure 5: A composite video signal filtered down to just the luma signal (right), the chroma signal is attenuated.

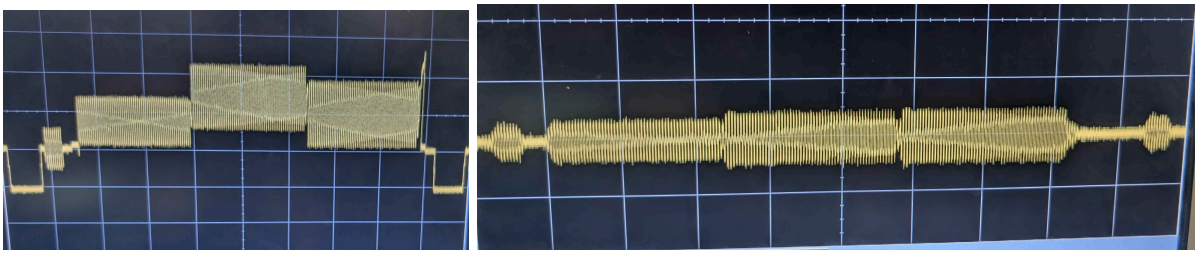


Figure 6: A composite video signal filtered down to just the chroma signal (right), the luma signal is attenuated.

2.1.2 Distortion Subsystem

The distortion subsystem is responsible for generating the glitches we aim to achieve from this device. It functions as a variable filter amplifier whose characteristics such as filter type, cutoff, and resonance are controlled digitally by rotary encoders connected to vactrols. Active circuit components receive power from the power subsystem.

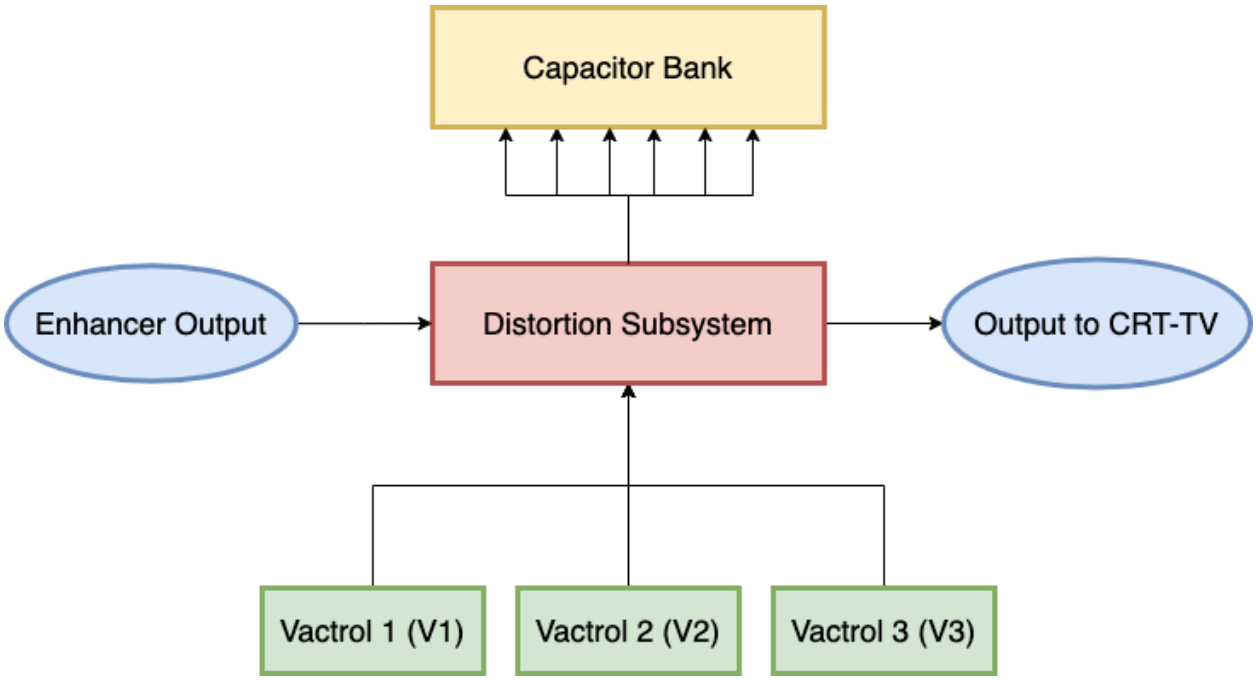
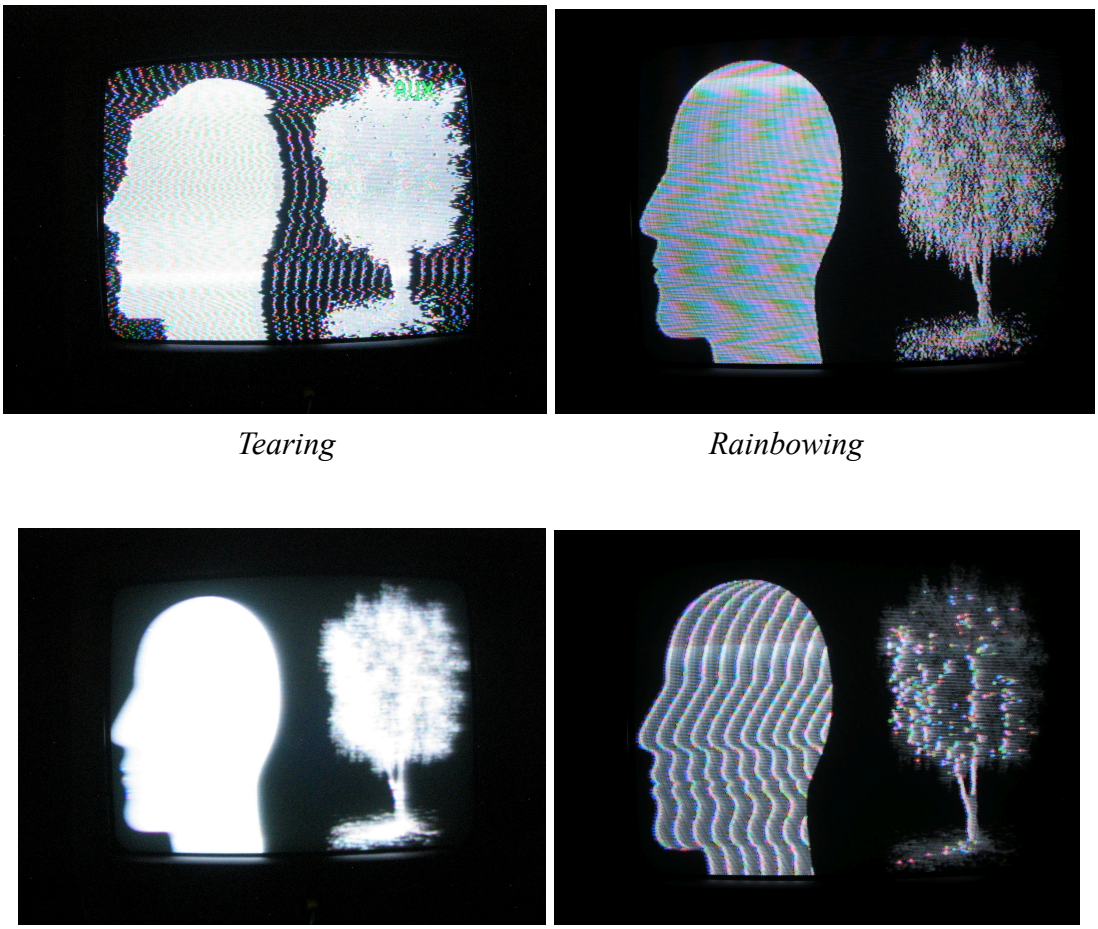


Figure 7: Block diagram of distortion subsystem.

The block diagram above shows how the distortion is controlled from three vactrols, with even more effect variation granted by the capacitor bank, where the user can choose to engage and disengage six different shunt capacitors in parallel. These capacitors destabilize the amplifier circuit as the feedback signal becomes more and more out of phase with the input as capacitance increases. This prevents the op-amps from reaching a constant voltage between their input pins and creates intense voltage swings which contribute to the glitches seen at the output. They also create resonance in the frequency response which causes a “ringing” effect in the video. See Appendix B for the circuit schematic and frequency response graphs at selected operating points.

Verification of this subsystem relied heavily on qualitative analysis. Because there is

technically no “correct” way to implement distortion, our tests centered mainly on qualitative comparisons between our outputs and those of existing circuit bent devices to try to approximate the effects they were able to achieve as closely as possible. To unit test effects, we used a monochromatic test image featuring a simple shape (a simple profile of a face) and a complex shape (a tree) to assess how the device operates at low and high frequencies respectively. These tests are shown below in Fig 8. More comprehensive requirements and verifications can be found in Appendix R.2.



Tearing *Rainbowing*

Ghosting *Ringing*

Figure 8: Video Distortion Effects

2.1.3 Control Subsystem

This subsystem forms the user interface of the device. The user inputs digital control signals using a row of rotary encoders mounted on the device. The signals from the encoders are transmitted to an STM32 microcontroller which decodes these signals into voltage levels to be delivered to the enhancer and distortion vactrols. The MCU communicates over SPI to several DAC ICs which generate and deliver voltages in the range of 0 to 0.5 V. These voltages are then offset by 2.5V and sent to the vactrols to control their resistance in the enhancement and distortion subsystems. We incorporate a GPIO input from a separate switch that toggles which set of DACs to output from, allowing the three encoders to control up to six parameters, though only five were used in practice. The figure below shows the block diagram for the control subsystem.

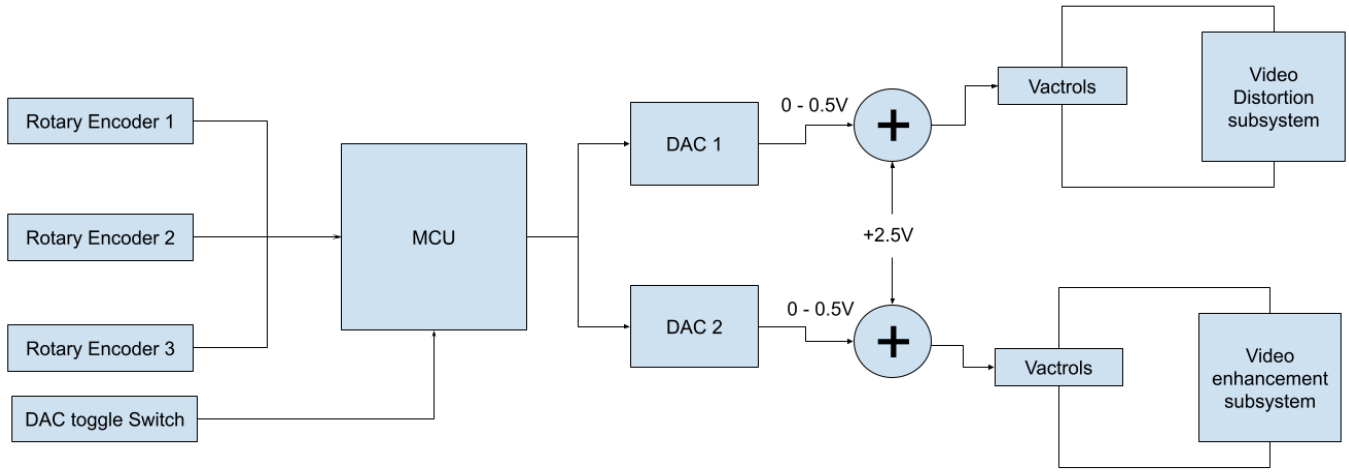


Figure 9: Block diagram of control subsystem.

Vactrols

The vactrol is the device that we use as a voltage-controlled resistor (VCR). A voltage bias lights up an LED, which shines directly onto a photoresistor. The higher the light's intensity on the photoresistor, the smaller the resistance of the photoresistor. The figure below shows a diagram of a vactrol device. We apply between 2.5V to 3V to the vactrol to vary resistance from 80-2000 Ohms.

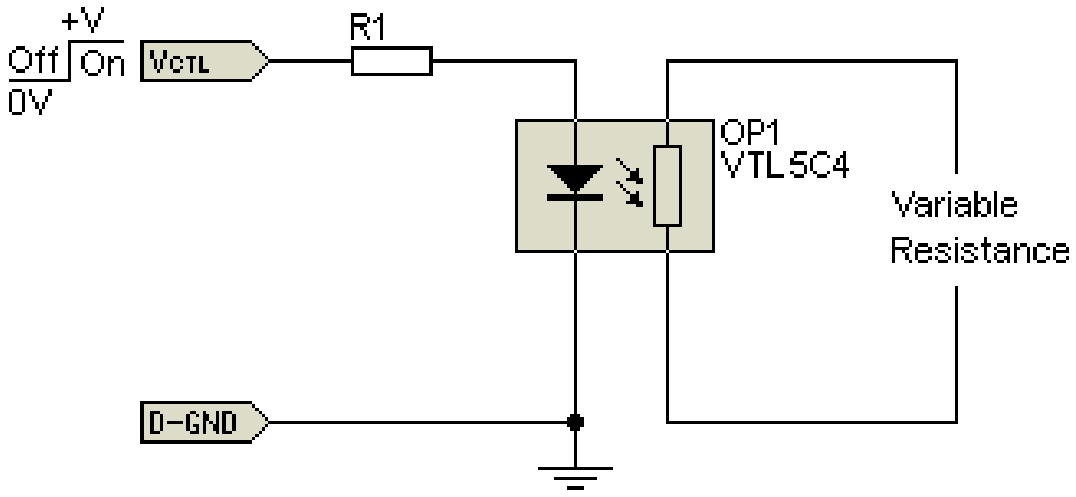


Figure 10: Vactrol device. The photoresistor circuit is optically isolated from the LED circuit.

See Appendix C for the vactrol voltage offset circuit producing the 2.5V offset to the DAC.

Digital to Analog Converter

The DAC takes the signal from the MCU, and converts it into an output voltage to be sent into the vactrols, controlling the vactrol's resistance. Our DAC IC has 4 DACs within it, so it also needs an address signal to know which DAC to update. It is an 8 bit DAC, so it can output voltages between 0 and 255/256*Vref, where Vref is the reference voltage. The address of the DAC and 0 to 255 value are sent by the MCU using SPI protocol. Load, LDAC and clock signals are also sent by the MCU. We use it to send 0 to 0.5V voltage signals, which is then offset by 2.5V before going to the vactrol to control the resistance in the other subsystems.

Microcontroller Unit

The MCU serves as an interface between the signal the rotary encoder sends, and the voltage output produced by the DAC. It reads the output of the rotary encoder using combined timers set in encoder mode, and increments a timer up or down based on this input. Then, it outputs this timer value to the DAC through a master only SPI protocol sending 2 address bits, 1 range bit, and 8 value bits (11 bits in total). The DAC which receives the input is determined by a

GPIO pin reading the value of the function switch. See Appendix C for more details on code in the microcontroller, and the pins of the microcontroller.

Encoders

The rotary encoder takes in rotation and produces two signals called CLK and DT. If DT is after the rising edge of CLK or before the rising edge of the CLK determines if it is turning clockwise or anti-clockwise respectively. The clockwise rotation is ultimately used to increase resistance, and anti-clockwise rotation is used to decrease resistance. The figure below shows the square wave outputs from the encoder, as well as the metal traces that send the high part of the square wave. [4]

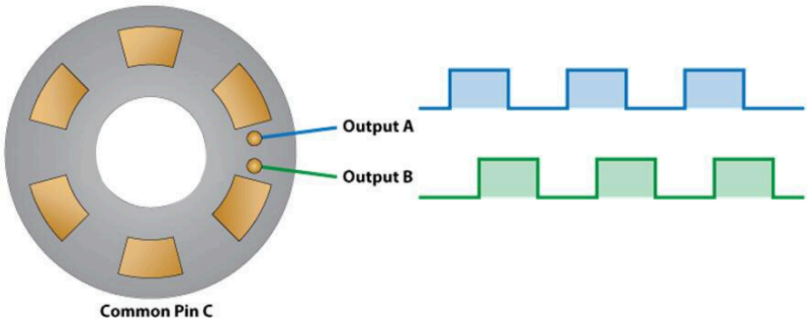


Figure 11: Encoder mechanics.

Verification of our control subsystem involved unit tests on our encoders and vactrols. To test the encoders, we used an oscilloscope to measure the outputs of their pins and ensure that we correctly connected them to the MCU. We then tested the code by ensuring that we could see the encoder values stored as variables in the code correctly incremented and decremented. To find the optimal voltage values to send to the vactrols, we used a power supply and multimeter to vary the current into the LED end and measure the resistance yielded. By doing this, we found that a range of 2.5V - 3V provided the optimal range of resistance values. To test integration of the DACs and vactrols, we connected them using a dev board and breadboard and debugged the outputs of the MCU until we could confidently control all vactrols via the MCU. More comprehensive results and verifications can be found in Appendix R.3.

2.1.4 Power Subsystem

The power subsystem is responsible for powering all parts of the design. It consists of a 9V DC power supply which feeds into two parallel linear voltage regulators. One regulator provides a stable 3.3V to the MCU. The other regulator regulates the 9V supply to 5V to power the DACs. The unaffected 9V power supply powers the op-amps, with their negative supply terminal grounded. The block diagram for the power subsystem is shown below. We consciously chose to omit any form of bypass capacitance which one would usually include to smooth the voltage supply. This is because the voltage supply fluctuations described in section 2.1.2 are necessary to achieve the glitches we are designing for. The use of bypass capacitors would dry up these glitches by forcing the distortion amplifier into a more stable state, and thus it was beneficial to leave them out of the power design. Appendix D contains more detailed schematics and figures.

However, this omission made denoising the power supply essentially impossible, which became a problem when we attempted to use a switched-capacitor buck converter to generate a negative supply. We realized too late that the 2KHz switching noise of the buck we purchased was low enough to be visible on screen, inducing unwanted noise. With no reliable way to denoise the supply without also removing the vital distortion power fluctuations, we opted to work around a single positive voltage supply and leave the negative supply out.

Verification of this subsystem was fairly straightforward. To verify that our power subsystem worked, we used an oscilloscope to measure the actual voltage going to our power pins on active components. We observed the ripples on our enhancer and distortion op-amps and determined that this was acceptable, because it did not compromise the performance of the enhancer. We also checked regulators for excessive heat, and were able to identify a short in our PCB from the heat emitted by our 3.3 volt regulator. Appendix R.4 contains more detailed tests which were performed.

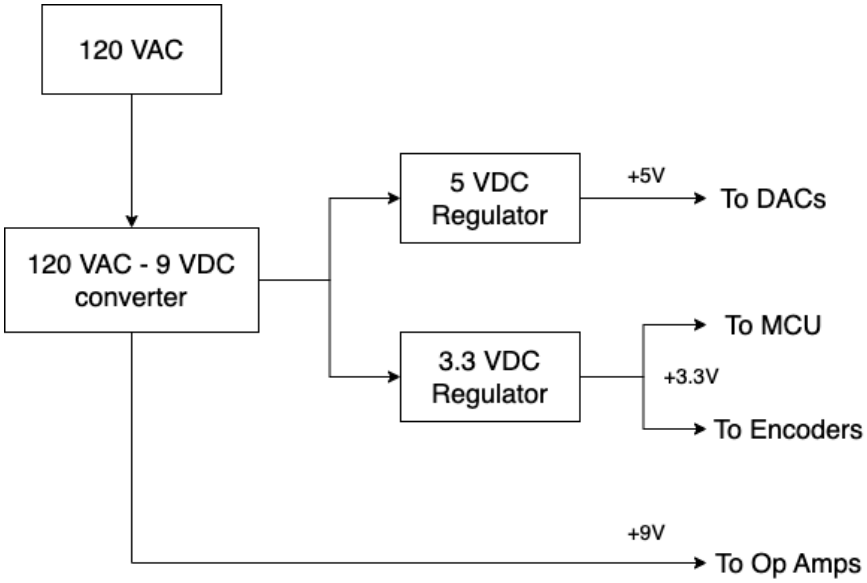


Figure 12: Block diagram of power subsystem.

2.2 Physical Design

The design of our user interface is shown in the diagram below. It includes an input RCA port, an output RCA port, a barrel jack that connects to our 120 VAC to 9 VDC power adapter, a switch to toggle between a grounded and floating negative power supply terminal on the op-amps used in our distortion circuit (which effectively bypasses it), a switch to bypass the enhancer stage of the circuit and route the input signal directly to distortion, six switches that can engage and disengage parallel capacitors in the capacitor bank, a switch to toggle which DAC to route the encoder counter value to, and a button to reset the program on the MCU. See Appendix P for the full PCB layout.

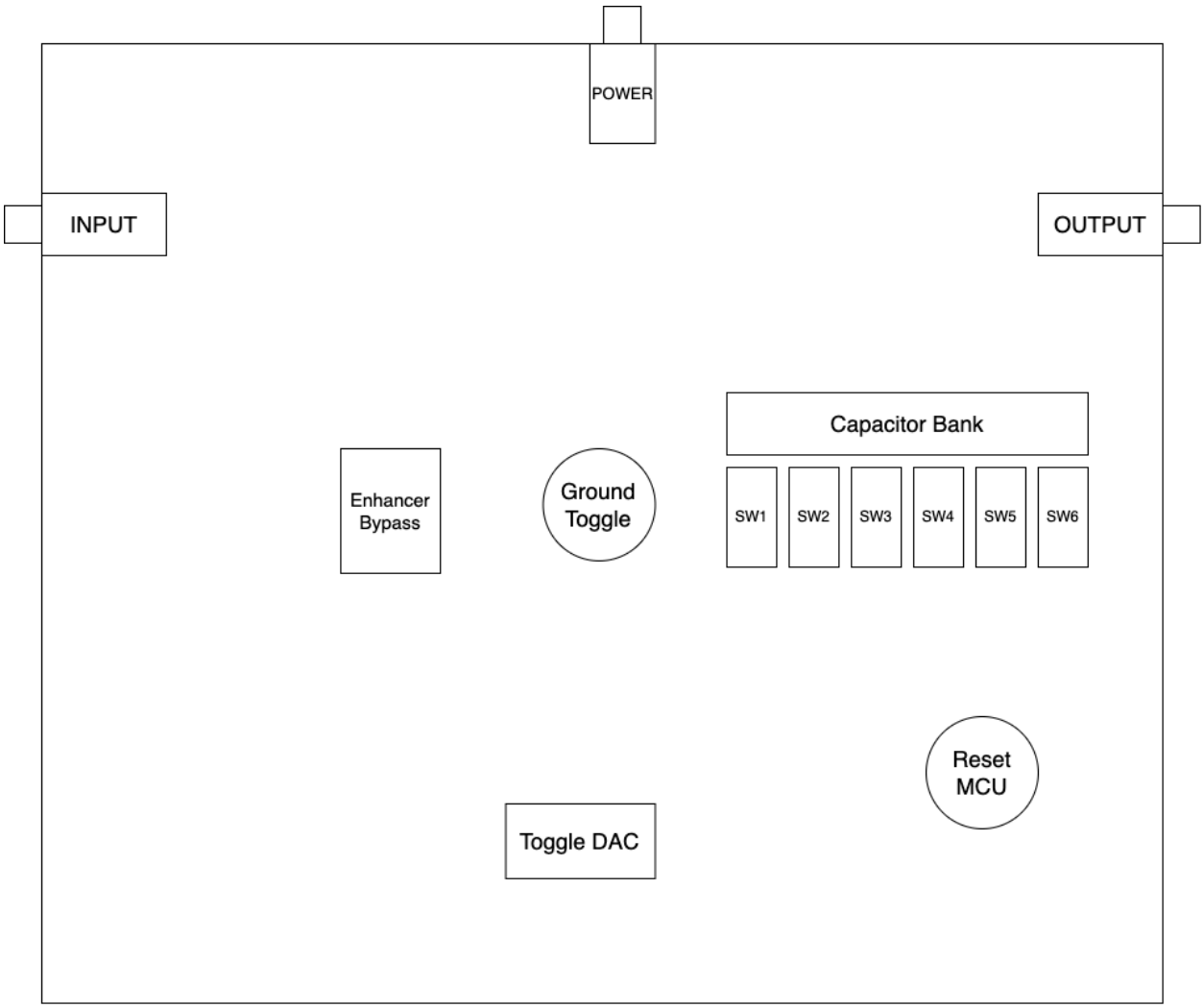


Figure 13: Physical layout on our PCB of the user interface.

3 Cost Analysis

3.1 Labor Costs

We expect a salary per team member of $40/hr * 2.5 * 80 hrs. This comes out to $8,000 per team member, yielding a total between three team members of $24,000.

3.2 Part Costs

The total cost before taxes is $106.36 for all the parts on our PCB. With a 5% shipping cost and 10% sales tax, our total cost becomes $122.31. The unit cost of our PCB was $11.95. With an assumed 5% shipping cost and 10% sales tax, we add an additional $13.74 to the total cost, which brings our total cost to $136.05. See the appendix E for the tabulated costs for each part.

4 Conclusion

4.1 Accomplishments

After completing our project, we were able to achieve a standalone device on one PCB that only takes an RCA input, an RCA output, and a power port as its peripherals. Additionally, we achieved our very important goal of digital control over analog circuitry, opening the possibilities of control types for the future. Our encoders are multi-functional, with one encoder controlling both an enhancement parameter and a distortion parameter, based on the value read from a switch. Finally, this device is highly versatile, with many features for creating unique glitch effects.

4.2 Challenges

Hue Shift

One major challenge we encountered was hue shifting. We were not able to implement an analog voltage controlled phase shift circuit due to the price of it (roughly $60 - $80).

Negative Voltage

Our original design included negative voltage capacity for our op amps by using a buck converter, but this introduced too many unwanted, non-interesting effects at the output (such as static and scrolling). We fixed this issue by DC offsetting our signal so that it only operated in the positive voltage space, no need for negative capacity on our op amps.

Integration

We experienced signal drop-out and loading issues when we first attempted to combine our enhancer and distortion stages. Eventually, we redesigned the circuit to include an op amp buffer between these stages, as well as different resistor values to reduce the reduction in signal.

Limited Timers

Our MCU had access to only three timers for reading our encoders. Since we needed five DAC outputs to power five vactrols. We incorporated a switch to fix this issue, allowing three encoders with three timers to control five different vactrols by switching which DAC the encoder would be routed to.

4.3 Ethical Considerations

In accordance with the IEEE Code of Ethics, we disclosed all personal knowledge gaps and uncertainties with each other in order to fully understand all issues collectively during the development process. Likewise, we only undertook tasks with a sufficient knowledge basis, ensuring team safety with testing with lab instrumentation (e.g. power supply) [5]. We took measures to ensure the width of the copper etchings on our PCB (especially copper traces connected to power sources) are wide enough to prevent excessive heat and thereby potential damages, as in accordance with the IPC 2221 standard [6]. In addition, in regulating voltages and currents throughout our device, we abided by OSHA 1910.303(b)(5), preventing faults between electrical components. For example, we provided voltage buffering when necessary between modules to lower input current. This was achieved with current dividers when appropriate [7].

While using the power supplies in the ECEB 2070 lab, we made sure to set a current limit on our constant voltage power output settings to protect our chips, and prevent burns from ICs becoming overheated.

We will provide a clear warning of seizures for users of this product, in accordance with the Federal Hazardous Substances Act (FHDA) and the FDA's 21 CFR document, section 369.10. [8].

4.4 Future Work

4.4.1 Presets

We think the current implementation can be improved by saving certain settings of the encoders in the MCU, so that they can be quickly retrieved without manually turning the knobs (encoders) to the required states everytime. This upgrade would make the instrument significantly more user friendly, as individuals could directly go to their preferred settings. Moreover, we can provide the user with default settings that produce interesting characteristic glitches, without the user having to find them manually through trial and error.

4.4.2 Control Through External Digital Signals

Now that we have achieved digital control of the enhancement and distortion system, we think that the potential for dynamic glitches based on audio or other external signals is unlocked. This could be done by controlling enhancement and distortion based on the properties of an external signal such as the amplitude and pitch of an audio signal. Without the groundwork we laid in this project, this would be a very difficult task, but by implementing digital control we have laid the foundation for extensive modulation opportunities. Moreover, this would further improve the functionality of our product for our target customer base (visual artists), and allow further integration and synchronization with larger visual systems which encompass lights, lasers, smoke machines, and multiple displays or projectors.

4.4.3 PCB Optimization

While our PCB is fully functional, it is far from optimized. Our final PCB ended up quite large, mostly due to the use of through-hole passive components and including header pins for all MCU pins. If we instead used SMD components and minimized the number of header pins, we could significantly cut down on size. Additionally, we could reduce reliance on analog switches to further digitize our design. The use of an analog multiplexer would allow digital signals to replace our analog capacitor switch bank, allowing this parameter to be encompassed in the digital controls.

References

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[6] IPC, "IPC-2221A: Generic Standard on Printed Board Design," *IPC*, 2003, Section 6.2.

[7] Occupational Safety and Health Administration (OSHA), *1910.303 - General Requirements for Electrical Installations*, OSHA. [Online]. Available: https://www.osha.gov/laws-regs/regulations/standardnumber/1910/1910.303. [Accessed: Mar. 6, 2025].

[8] U.S. Food and Drug Administration, "21 CFR § 369.10 - Conspicuousness of warning statements," *Electronic Code of Federal Regulations*, [Online]. Available: https://www.law.cornell.edu/cfr/text/21/369.10. [Accessed: May 7, 2025].

Appendices

A Enhancer Details

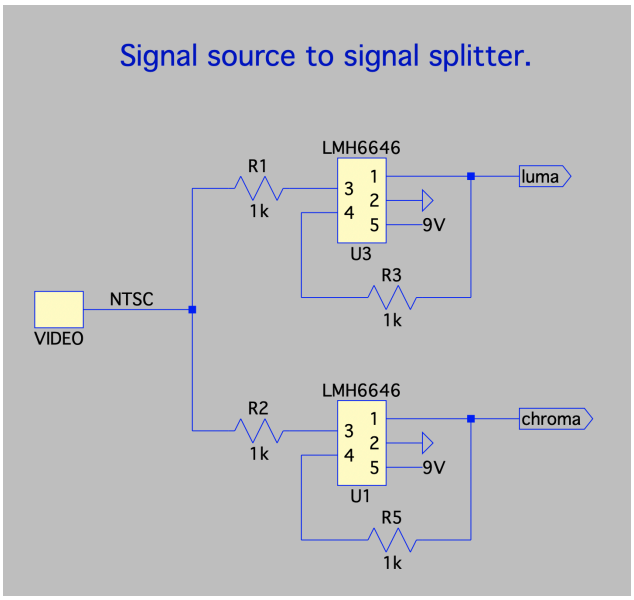


Figure A.1: Circuit for enhancer signal separation. Input impedance is very high while output impedance is very low, meaning the circuits are effectively isolated at the op amp inputs and the loading/voltage division effects are negligible at the output.

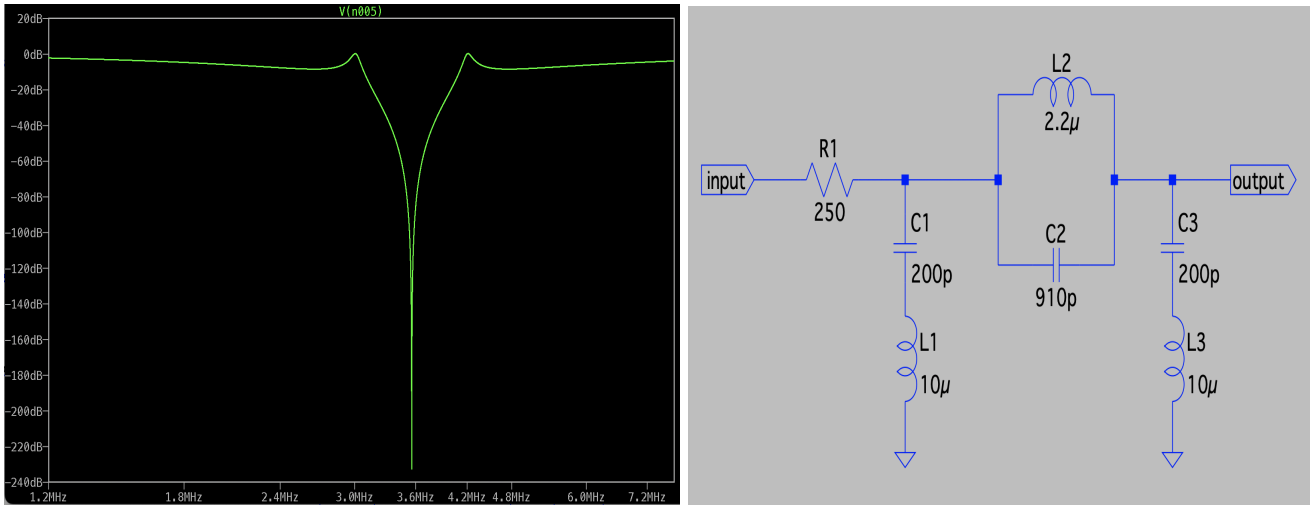


Figure A.2: Magnitude response and circuit of luma filter. Chroma is almost completely attenuated due to notch at 3.58 MHz. The circuit is second order band-stop.

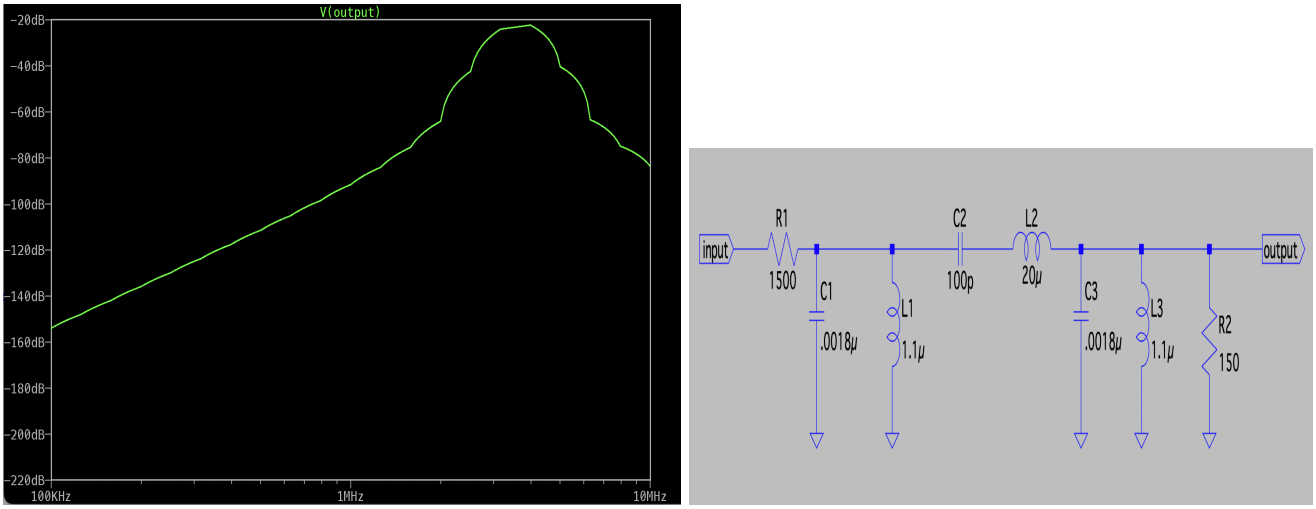


Figure A.3: Magnitude response and circuit of chroma filter. Chroma is preserved at 3.58 MHz center frequency of filter, luma is attenuated. The circuit is a second order band-pass.

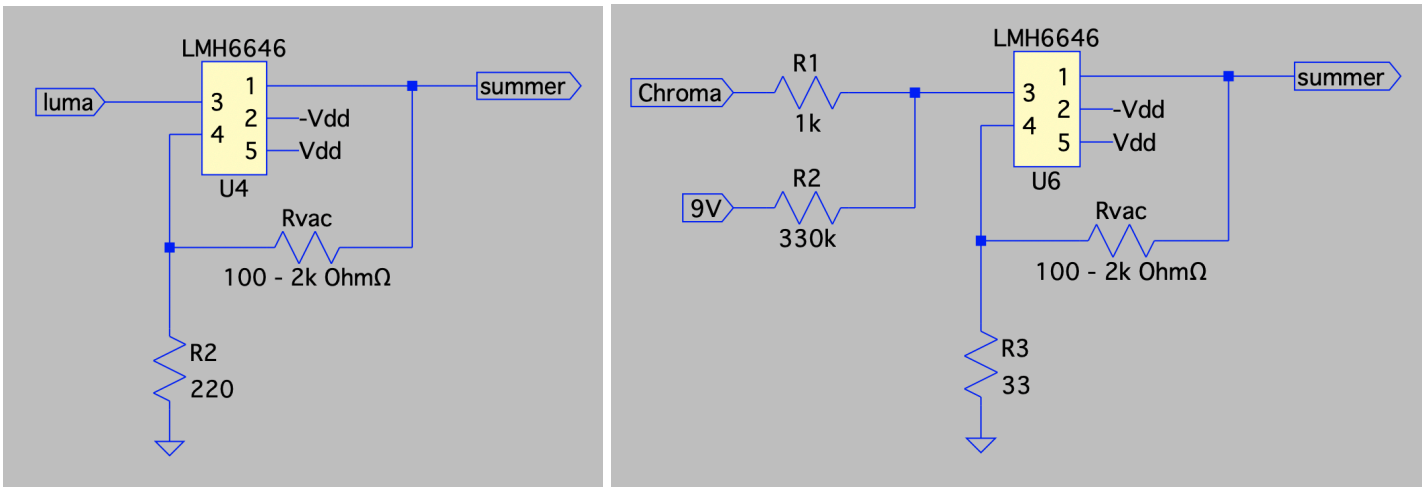


Figure A.4: Non-inverting amplifier configuration for luma signal line (left) and non-inverting amplifier configuration with DC summation stage for chroma signal line (right).

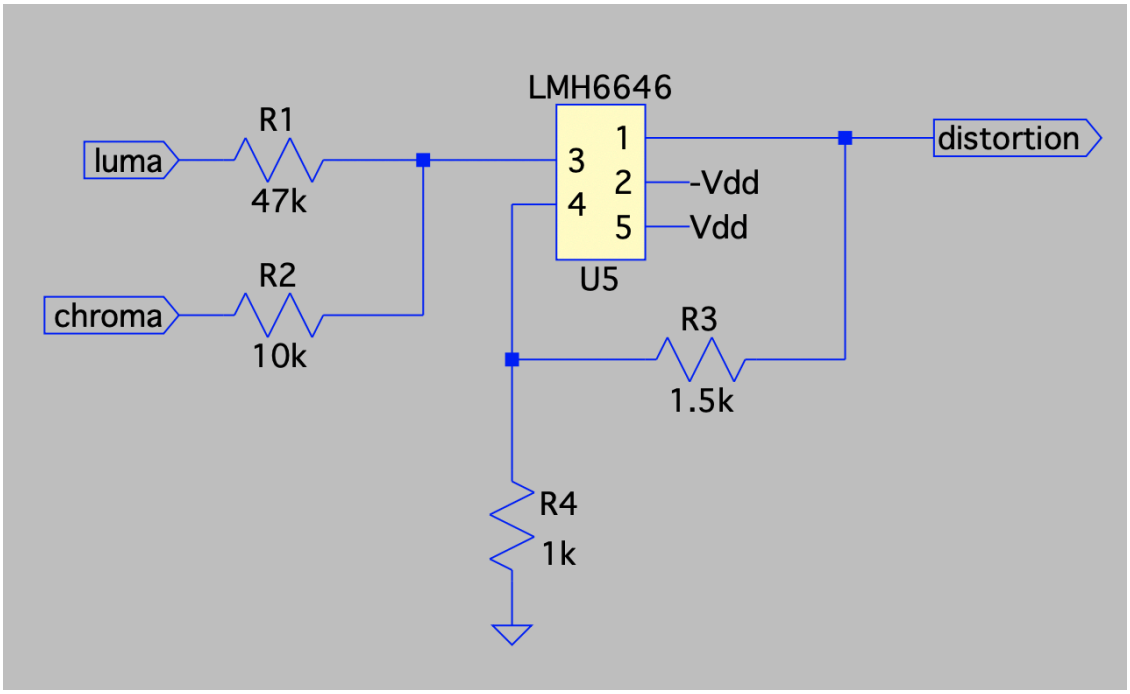
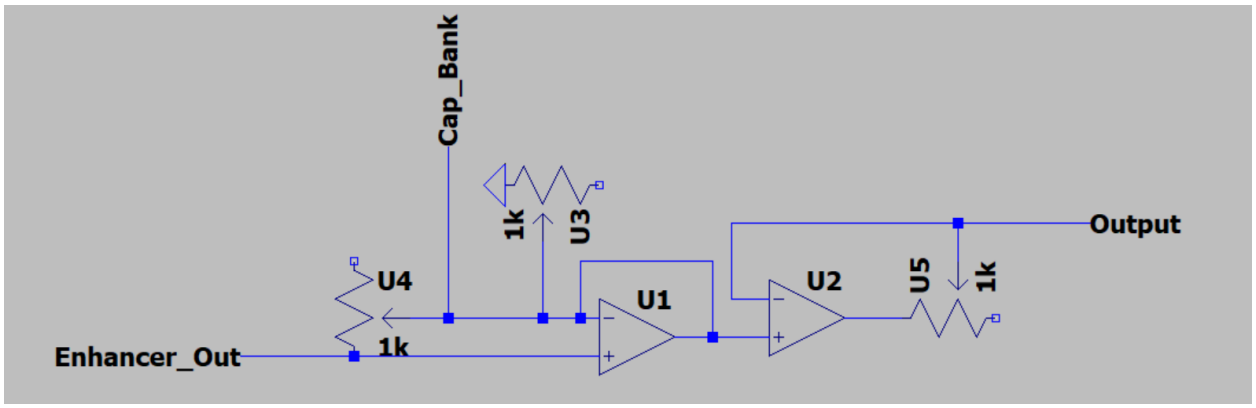


Figure A.4: Non-inverting summer configuration for signal recombination.

B Distortion Details

B.1 Distortion Circuit



B.2 Distortion Properties

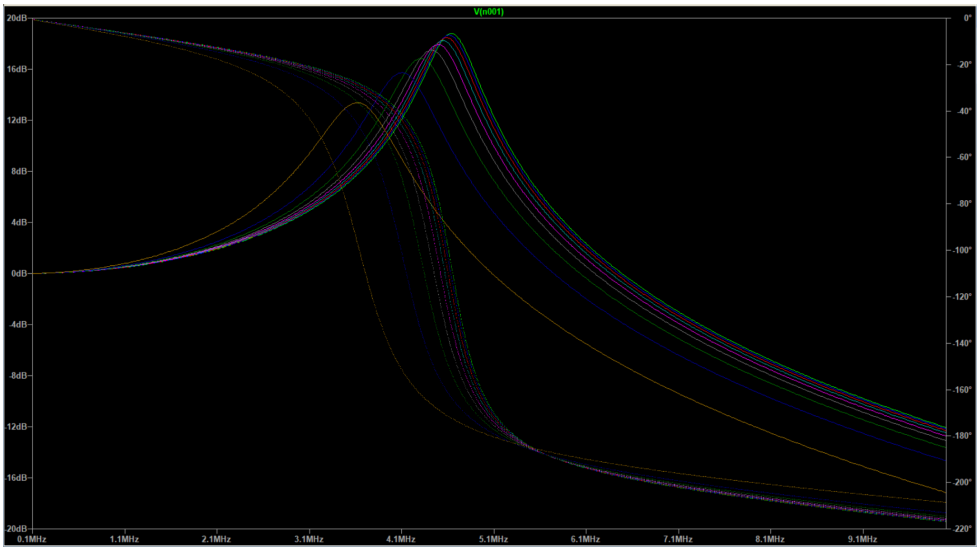


Figure 4: Bandpass response with significant phase shifting when vactrol V1 is varied (vactrol V2 is at 75% of its maximum resistance and vactrol V3 is at 95% of its maximum resistance). The capacitance of the capacitor bank is set to 5 nF. This illustrates V1's ability to vary the cutoff frequency of our distortion circuit.

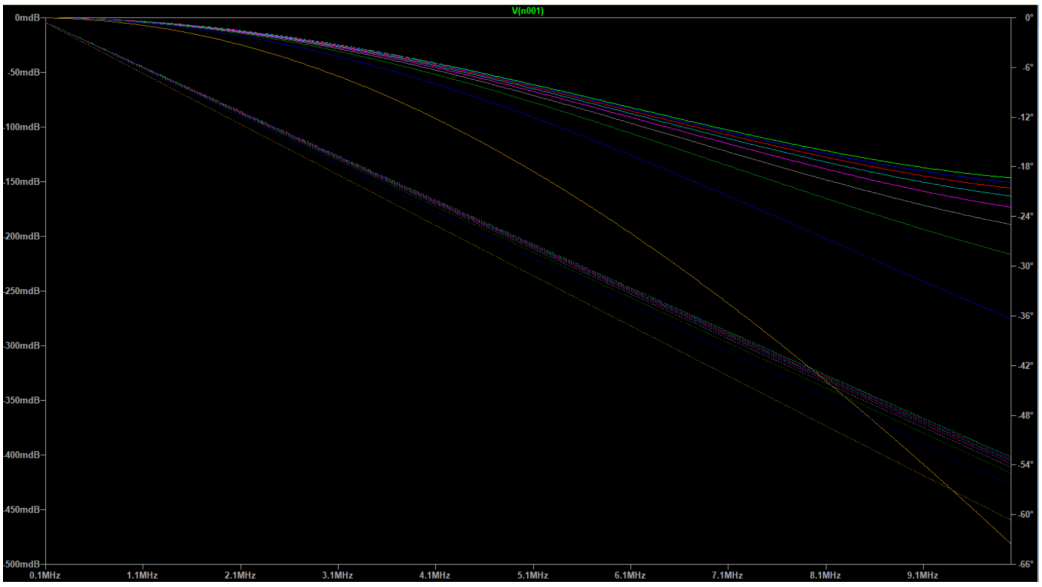


Figure 5: An increasing quality lowpass filter when vactrol V2 is varied (vactrol V1 is at 5% of its maximum resistance and vactrol V3 is at 95% of its maximum resistance). The capacitance of the capacitor bank is set to 5 nF. This illustrates V2's ability to control the feedback of our filter.

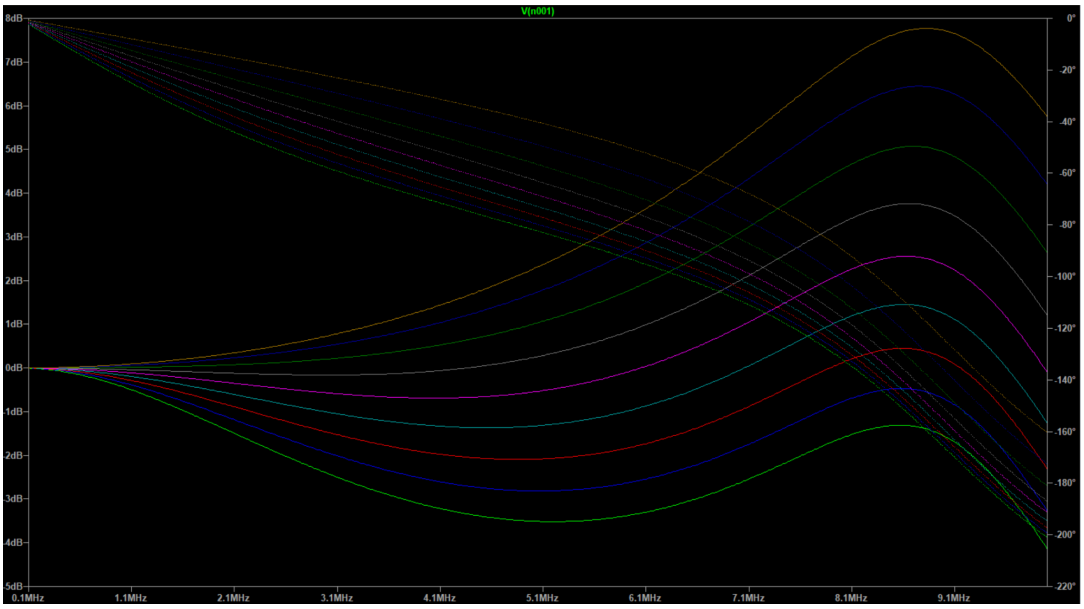


Figure 6: Highpass-bandpass hybrid response when vactrol V3 is varied (vactrol V2 is at 75% of its maximum resistance and vactrol V1 is at 80% of its maximum resistance). The capacitance of the capacitor bank is set to 1 nF. This illustrates V3's use as a post-gain amplifier that doesn't significantly affect the filter curve.

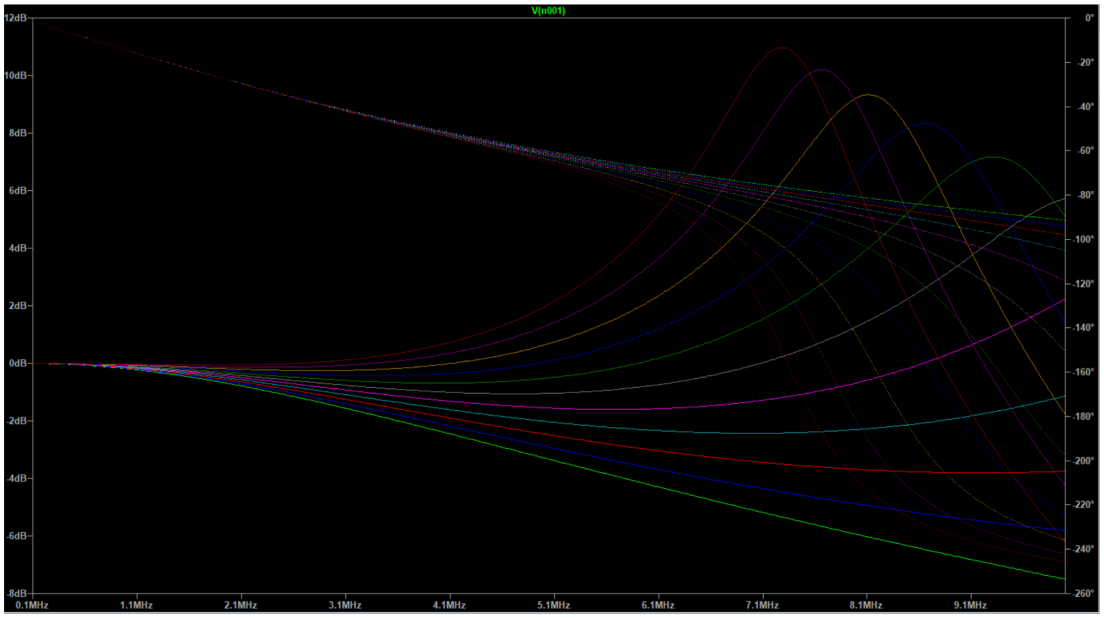


Figure 7: Filter response shifting from lowpass to highpass to bandpass as the capacitor bank is varied from 0 to 2 nF (vactrol V1 is at 5% of its maximum resistance, vactrol V2 and V3 are at 50% of their maximum resistances). This illustrates the capacitor bank's role in controlling the character of the filter.

C Control Details

C.1 Vactrol Offset

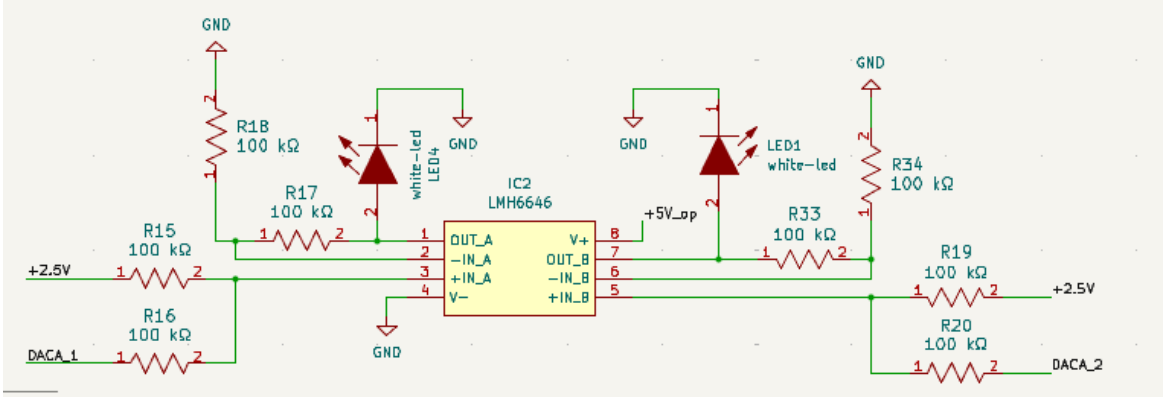


Figure C.1: This circuit shows the non-inverting op amp summer circuit that adds the 2.5 V offset with the DAC output (0 - 0.5 V) and sends the op amp output into the vactrol. The 2.5 V is generated via a simple voltage divider circuit, dividing down 5 V. the resistances used in this voltage divider are not comparable to the resistances of the op amp summer in order to reduce unintentional loading effects.

C.2 DAC Details

Setup

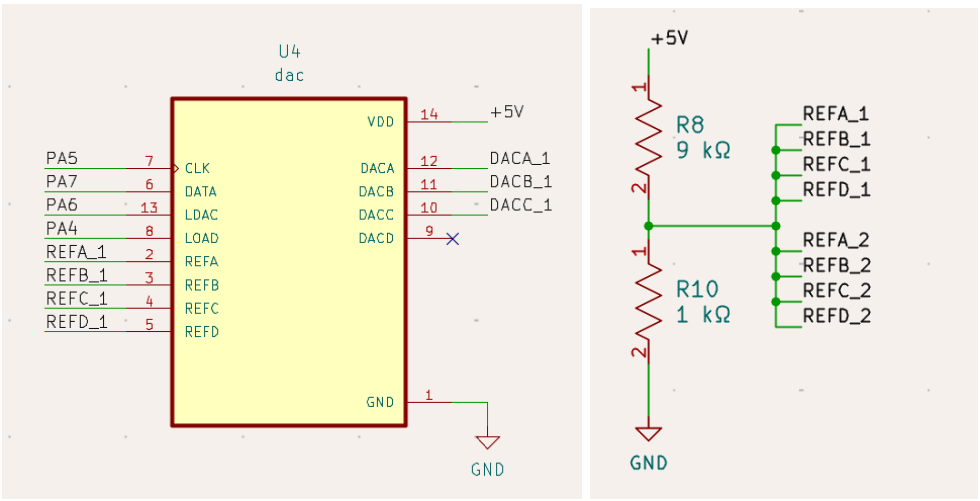


Figure 4: DAC Pins configuration, and voltage divider for 0.5V ref signal

Pins

1. GND -- Ground
2. REFA -- Reference voltage for DAC A, set to 0.5V using a voltage divider
3. REFB -- Reference voltage for DAC b, set to 0.5V using a voltage divider
4. REFC -- Reference voltage for DAC C, set to 0.5V using a voltage divider
5. REFD -- Reference voltage for DAC D, set to 0.5V using a voltage divider
6. DATA -- Data signal, connected to SPI1_MOSI from the MCU
7. CLK -- Clock signal, connected to SPI1_CLK from the MCU
8. VDD -- Voltage supplied, this has to be 5V sent by the power subsystem
9. LDAC -- Signal to update output, connected to SPI1_LDAC from the MCU
10. DACA -- Out signal of DAC A
11. DACB -- Out signal of DAC B
12. DACC -- Out signal of DAC C
13. DACD -- Out signal of DAC D
14. LOAD -- Used to update the input of the DAC registers

C.3 MCU Details

MCU code

The figure below shows a flow chart of the program we implemented on the MCU. The code starts by using an interrupt to run a check to determine which encoder was turned. Then, it offsets the counter value given by the timer by some number of bits corresponding to the appropriate DAC output (either output A, B, or C). The program then reads the DAC switch value at a GPIO port to determine which of two different DAC chips the counter's value should be sent to, adding the new counter value to the old counter value held in the DAC's output.

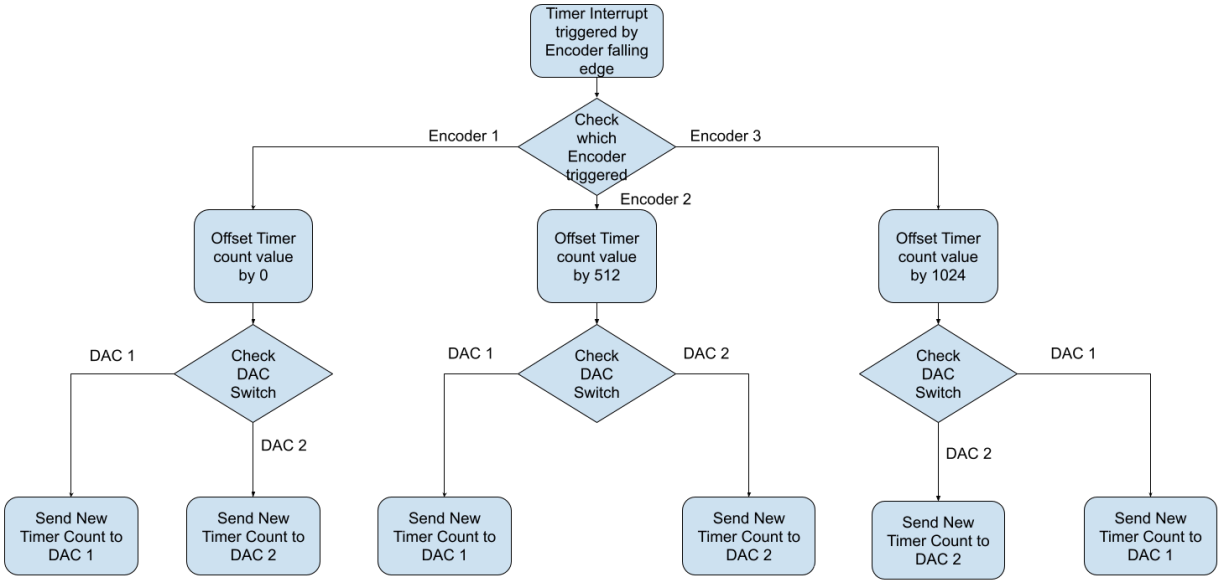


Figure 10: Flow diagram for MCU program.

MCU Pins

The pinout for our MCU is shown below. The pins dedicated to timers are grouped together and assigned an encoder. The SPI communication pins for the DACs are also grouped at the bottom of the MCU. The SPI1_LOAD and SPI1_LDAC signals used for both of the two DAC chips. Both DAC chips get individual data (SPIx_MOSI) and clock (SPIx_SCK) signals, as shown below.

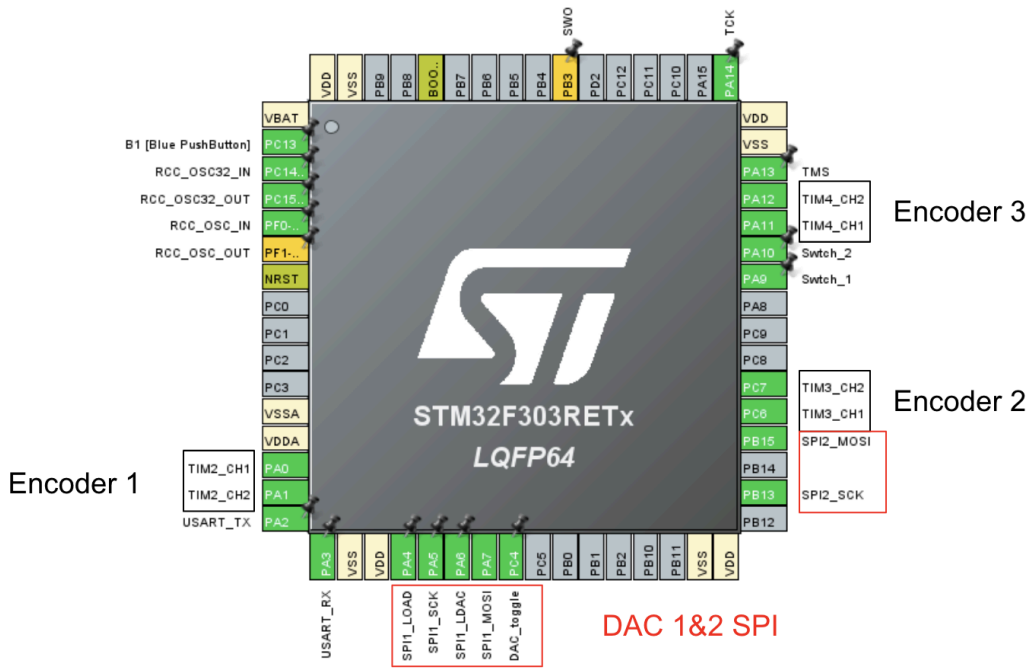


Figure 11: Pinout from MCU.

Inputs

1. TIM2_CH1 -- Timer connected to CLK of rotary encoder 1
2. TIM2_CH2 -- Timer connected to DT of rotary encoder 1
3. TIM3_CH1 -- Timer connected to CLK of rotary encoder 2
4. TIM3_CH2 -- Timer connected to DT of rotary encoder 2
5. TIM4_CH1 -- Timer connected to CLK of rotary encoder 3
6. TIM4_CH2 -- Timer connected to DT of rotary encoder 3

Outputs

1. SPI1_LOAD -- Load signal sent to DAC used to send values to DAC register
2. SPI1_LDAC -- Load DAC signal sent to DAC to ask it to update its output values
3. SPI1_SCK -- Clock signal sent to the DAC1
4. SPI1_MOSI -- Data signal sent to the DAC including the address of the DAC (2 bits) to which the value has to be sent and the value (8 bits) that needs to be sent. The range value is always set to 0 (1 bit)
5. SPI2_MOSI -- Data signal sent to the DAC2 including the address of the DAC (2 bits) to which the value has to be sent and the value (8 bits) that needs to be sent. The range value is always set to 0 (1 bit)
6. SPI2_SCK -- Clock signal sent to the DAC2

D Power System Fluctuations

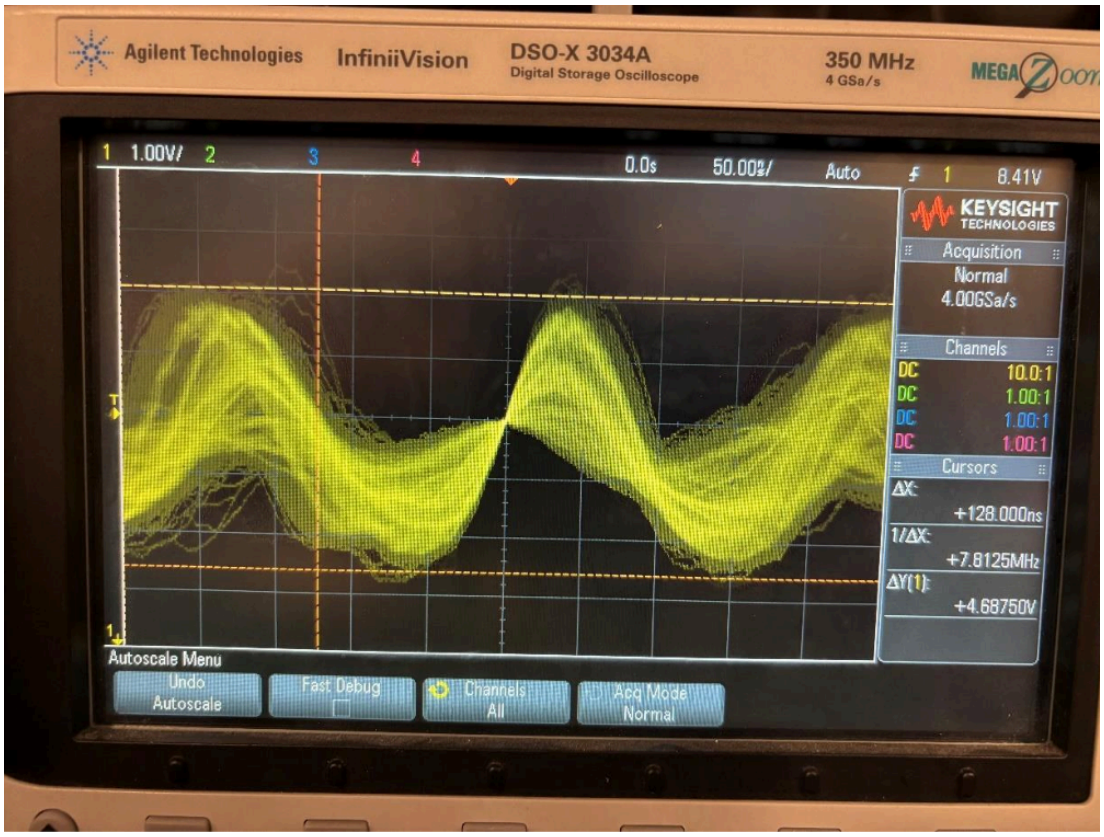


Figure D.1: 4.5V voltage swing along the positive power supply line.

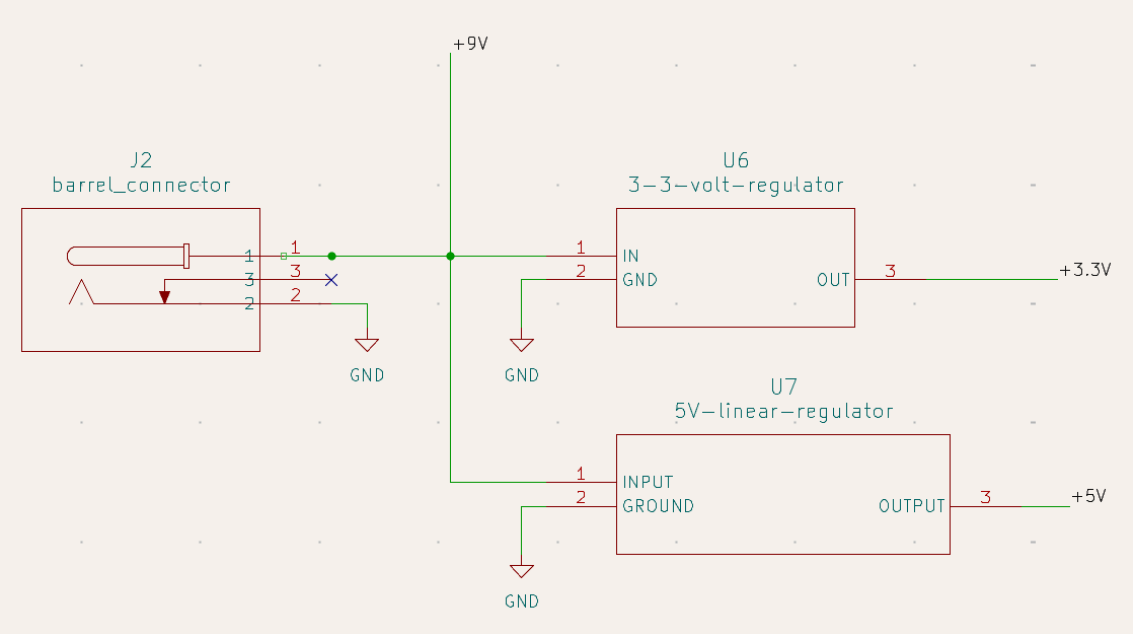


Figure D.2: Circuit schematic of power subsystem.

E Costs Tabulated

Description	Manufacturer	Quantity	Ext. Price	Catalog Number
Header Pin	Würth Elektronik	70	$4.98	732-5314-ND
Switch	Same Sky	9	$7.47	2223-SLW-1276864-4A-D-ND
10 kΩ Resistor	YAGEO	11	$0.43	13-MFR-25FRF52-10KCT-ND
1.8 nF Capacitor	TDK Corporation	2	$0.64	445-180714-1-ND
100 kΩ Resistor	Stackpole Electronics	22	$4.84	CF18JT100KCT-ND
33 Ω Resistor	Stackpole Electronics	1	$0.10	CF14JT33R0CT-ND
100 nH Inductor	Bourns Inc.	2	$0.42	M10147-ND
RCA Connector	Same Sky	2	$3.08	CP-1422-ND
1 kΩ Resistor	Stackpole Electronics	11	$0.29	CF14JT1K00CT-ND
Dual Op Amps (LMH6646)	Texas Instruments	4	$11.48	926-LMH6646MAX/NOPB
0.1 uF Capacitor	KEMET	6	$1.32	399-9870-1-ND
Push Button	C&K	2	$3.12	401-1995-ND
1 nF Capacitor	Vishay	2	$0.82	BC5260CT-ND
White LED	VCC	5	$3.25	VAOL-5LWY4
10 uH Inductor	Abracon LLC	2	$0.32	535-AICC-02-100K-TCT-ND
Photoresistor	Adafruit Industries LLC	5	$8.10	1528-2141-ND
500 pF Capacitor	Vishay	2	$1.14	BC5191-ND
330 kΩ Resistor	Stackpole Electronics	1	$0.10	CF18JT330KCT-ND
4-Channel 8-bit DAC	Texas Instruments	2	$13.52	296-1862-5-ND
1 uF Capacitor	TDK Corporation	2	$0.98	445-173374-1-ND
3.3V Linear Regulator	STMicroelectronics	1	$1.13	497-7312-5-ND
9 kΩ Resistor	Vishay	1	$1.09	541-CMF559K0000BHEBCT-ND
1.5 kΩ Resistor	Stackpole Electronics	1	$0.10	CF12JT1K50CT-ND
STM32F303RET6 Microcontroller	STMicroelectronics	1	$9.84	497-15163-ND
47 kΩ Resistor	Stackpole Electronics	1	$0.10	CF12JT47K0CT-ND
5V Linear Regulator	STMicroelectronics	2	$1.00	497-1443-5-ND
2.2 uH Inductor	TDK Electronics	1	$0.29	495-76019-1-ND

10 nF Capacitor	Murata Electronics	1	$0.59	490-9257-1-ND
Single Op Amp (LMH6645)	Texas Instruments	6	$13.20	926-LMH6645MAX/NOPB
1 uH Inductor	EPCOS- TDK	2	$0.50	495-5547-1-ND
2.2 uF Capacitor	Panasonic Electronic	1	$0.26	10-ECA-0JM471ICT-ND
100 pF Capacitor	Vishay	3	$0.63	BC2657CT-ND
0.33 uF Capacitor	TDK	2	$0.60	445-173139-1-ND
4.7 uF Capacitor	TDK	1	$0.37	445-173255-1-ND
Encoder	Bourns	3	$4.83	652-PEC12R-4215F-S24
20 uH Inductor	Würth Elektronik	1	$0.98	732-3765-ND
200 pF Inductor	KEMET	2	$0.76	C325C201K3G5TA-ND
910 pF Capacitor	KEMET	1	$0.38	399-C325C911JAG5TA-ND
Barrel Connector	Kycon	1	$0.56	2092-KLDX-0202-AC-ND
150 Ω Resistor	Stackpole Electronics	1	$0.10	CF18JT150RCT-ND
2x3 Connector	SparkFun	1	$1.80	474-PRT-10877
250 Ω Resistor	Vishay Dale	1	$0.65	1135-1592-ND
1.5 kΩ Resistor	Stackpole Electronics	1	$0.10	CF12JT1K50CT-ND
220 Ω Resistor	Stackpole Electronics	1	$0.10	CF14JT220RCT-ND

Figure 15: Itemized list of components and costs.

R Requirements and Verification

R.1 Enhancer Subsystem

Table 1: Video Enhancement Subsystem - Requirements & Verification

Requirements	Test	Verification
• The contrast will be controlled by amplifying the luma component of the composite video signal and must be able to amplify between a factor of -2 and 2.	• Apply the appropriate 2:1 feedback resistor ratio such that a voltage control domain of [-1V, 1V] provides an amplification range (in V/V) of [-2, 2]. • Confirm our design using a waveform generator to send a sine wave into the amplifier, then looking at the output signal with an oscilloscope, correcting our design as necessary.	• Yes, we have confirmed amplification between 0.5 to 2. However, we could not do negative amplification because of the challenges with negative voltage supply. • Yes, our amplifier can amplify an AC signal of high frequency around the chroma subcarrier frequency effectively, but phase shifting and non-linearities begin occurring around the 5 MHz range.
• The brightness will be controlled by applying a DC offset to the luma signal, which must range from pure black (0V) to pure white (715mV).	• Attenuate chroma subcarrier with a properly tuned notch filter and provide DC offset from a voltage source and voltage divider circuit if needed. • Apply a diode clipping circuit to ensure the signal does not pass 715mV in amplitude. • Analyze results through an oscilloscope and verify both the DC offset and the clipping.	• Yes, we can isolate the luma subcarrier by filtering chroma. • The TV automatically acts as a diode clipping circuit, so we did not require one for our design and demonstration. • We do not apply a DC offset to our luma line, but we can see the signal begin to clip at +5 V on the TV.
• The saturation will be controlled by amplifying the sinusoidal chroma subcarrier component, which encodes color, and must be able to amplify between a factor of -5 and 5.	• Apply a bandpass filter to isolate the chroma subcarrier • Setup the amplifier circuit making sure to apply a 4:1 feedback resistor to shunt resistor ratio. • Use a 2V peak-to-peak sine wave with zero DC offset. The oscilloscope should	• Yes. Our circuit can amplify a chroma signal linearly based on the transfer function of the amplifier, and we can achieve a 5 V/V gain. Since we don't have any negative voltage capacity for our op amps, we need to DC offset our signal appropriately to prevent clipping during

Requirements	Test	Verification
	display (approximately) a 10V peak-to-peak sine wave at the output of the amplifier.	amplification.
• To control these effects, control voltage will be delivered to the amplifier ICs from a DAC to control their gain. Control over the full range of effects must be achieved using a control voltage between -1V and 1V.	• Send a digital test signal via our MCU and observe the output from our DAC to verify correct operation. • Write code in STM32 Cube IDE to convert output of infinite encoder to a value between -1V and 1V, clipping the encoder value if necessary.	• The MCU can communicate with the DAC to generate voltage outputs. • Our design has changed since this requirement was added, but the encoder indeed can set a voltage between a range of 0 to 0.5 V. We no longer need a negative voltage to be generated from the encoder since we have negative amplification in our circuit.
• Sync pulses must be protected using a sync extraction IC. When reinserted at the end of the processing chain, its voltage must be at -300mV in order to remain in spec with the video signal.	• Verify the separation of sync from the video signal via an oscilloscope • Utilize an op amp summer to add sync back into the base signal after the base signal passes completely through the processing circuit. • Make note of any temporal deviation between the restored sync signal and the base signal post processing.	• We did not implement sync separation in our final design as it was not required. • Since we incorporated a DC offset, sync would not be subject to clipping below 0 V, since it was always in the positive voltage space.
• In order to ensure the distorted image can be displayed on a CRT, the luma signal must be clipped at 0mV and 715mV.	• Generate a 1V zero-to-peak sine wave and run it through our clipper circuit. • Analyze the output on an oscilloscope. There should be a clear, abrupt cutoff at 715mV.	• We did not require a clipping circuit, since our TV could operate well above the 715 mV cutoff we had set for ourselves before.

R.2 Distortion Subsystem

Table 2: Video Distortion Subsystem - Requirements & Verification

Requirements	Testing	Verification
• To control the quality of these glitches, the fed-back signal will pass through RC highpass and lowpass filters to achieve the ringing and ghosting effects, respectively. We will experiment with various feedback configurations to find visually appealing setups. Our feedback configurations should be unity gain.	• Make sure that applied effects are the result of added circuitry and not loose wires or capacitive effects from outer forces. • Analyze changes in overall signal gain from feedback loop with an oscilloscope.	• Yes, the effects are a result of the circuitry. • The signal gain is high enough that it is displayed clearly on a CRT-TV
• To control the strength of our distortion effects, we will vary the amplitude of the fed-back signal, via a control voltage ranging either -1V to 1V or 0V to 1V. This can be done with a specialized voltage-controlled amplifier IC.	• Ensure through visual inspection on both a CRT TV and oscilloscope a smooth transitioning from no distortion to a full distortion effect when adjusting the feedback gain.	• We can successfully and smoothly adjust the gain of our signal with no noticeable transient effects showing in the TV. • We no longer require negative voltages in our circuit.

R.3 Control Subsystem

Table 3: Control Subsystem - Requirements & Verification

Requirements	Testing	Verification
• To interface with a controller, we must either connect a pre-built controller to the MCU over USB, or build a custom controller which can communicate over a simpler protocol, such as SPI.	• Determine the controller's expected protocol to transfer data to the MCU. • Verify that the controller is communicating with MCU via a basic pin readout program on the STM32Cube IDE.	• The controller (encoders) produce phase offset squarewaves to communicate with MCU • Yes, we used live variable debugging to verify communication between encoders and MCU
• The MCU must interpret the signals indicating changes in the positions of joysticks, knobs, or the press of a button and send signals to a DAC using SPI to tell it to change voltage levels in the analog circuitry.	• Read the value of pins attached to switches to make sure they toggle between two discrete values appropriately.	• Yes, we used live variable debugging to verify switch values.

R.4 Power Subsystem

Table 4: Power Subsystem - Requirements & Verification

Requirements	Testing	Verification
• We will use a 9V DC power supply to deliver power to all components, and use a linear regulator to step the voltage down to 5V for the DACs, and 3.3V for the MCU and encoders.	• Read the power supply voltages with a digital multimeter and confirm that the powers read 9 V, 5 V, and 3.3 V. from the corresponding voltage regulator.	• The voltage values read back accurately within a tolerant error.
• We will use a buck converter to additionally convert the positive 5V DC voltage to a -5V DC voltage.	• Input 5V into the buck converter and use a multimeter to read the DC voltage output of the buck converter. Ensure the output is -5V.	• We no longer use a buck converter in our circuit.

P PCB Layout

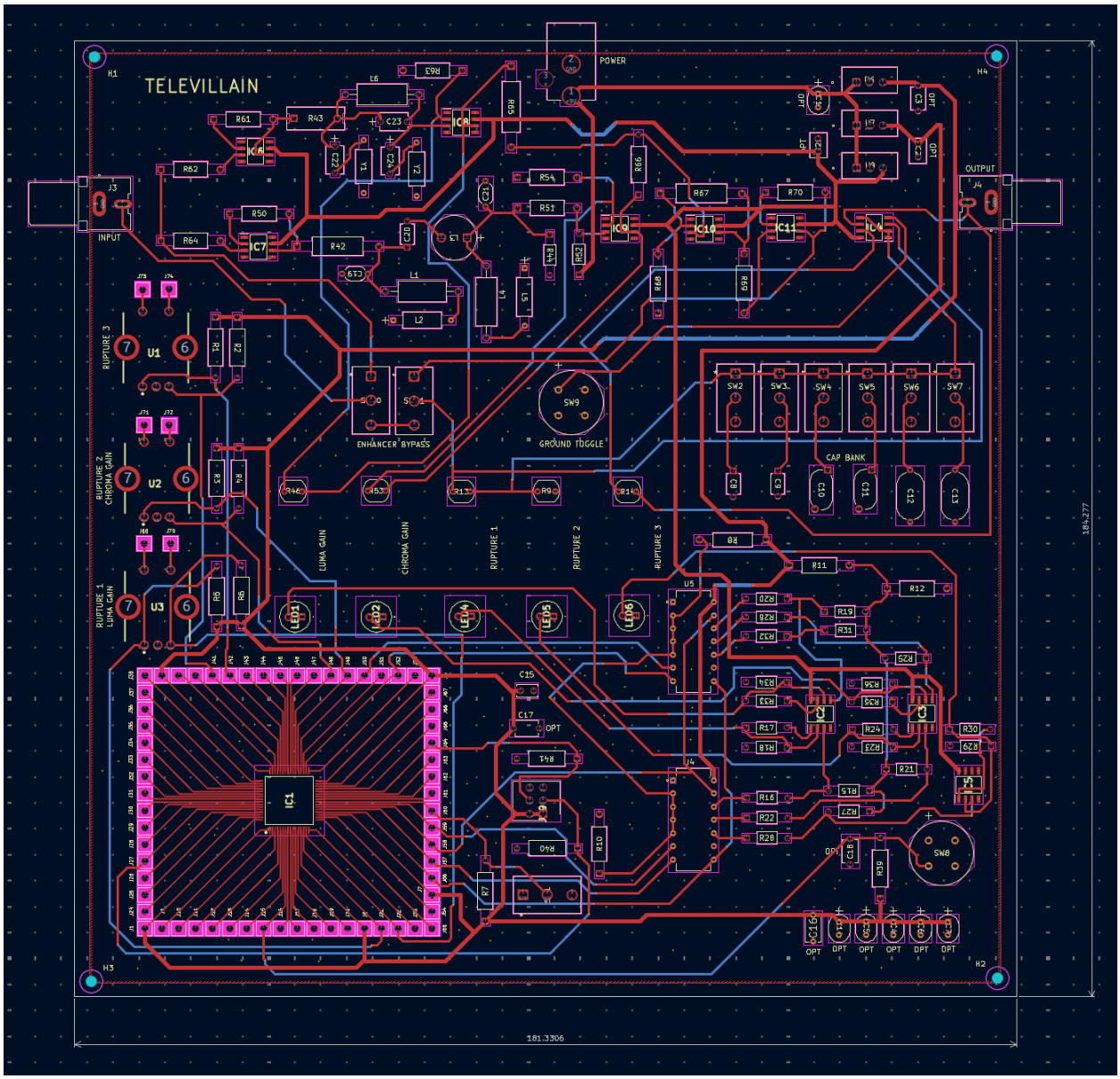


Figure P.1: PCB Layout of Televillain.