Project #3: CCD Image Sensor Board for Film Camera Retrofit

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Final Report for ECE 445, Senior Design, Spring 2025

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4 May 2025

Project No.3

Abstract

This report details our project which modifies a film camera to become a digital camera. This is accomplished by constructing a self-contained module containing a Printed Circuit Board (PCB) with a Charge Coupled Device (CCD) imaging sensor that fits onto the back of a film camera, replacing the original film for capturing the image. The module then interfaces with the camera to capture images precisely when the camera's shutter fires. This camera and module assembly is able to save 6 megapixel raw bayer images at a rate of 1 image per second to microSD cards, is powered by rechargeable batteries, and can be adapted to fit other cameras. Even with its highly compact design, the assembly's images are clean with little noise, and there is room for additional software features.

This report will provide an overview of the design process, validation, and resources undertaken by the designers of this project.

Contents

1. Introduction

The sudden explosion of demand for old CCD sensor equipped cameras amidst the digicam trend [1][2] is mismatched against a supply of 10-20 year old cameras that are increasingly unreliable and outdated. Between strong consumer demand for these out-of-production cameras, a rise in age-induced failures, and a shortage of outdated, scarce accessories such as proprietary batteries and obsolete storage cards, functioning examples of these CCD cameras are now very difficult to obtain and more fragile than ever.

Our project creates a new source of reliable CCD sensor cameras that can meet modern expectations. Our project accomplishes this by creating a PCB that accepts commonly available salvaged CCD sensors and interfaces them with plentiful advanced film cameras. By using powerful modern microcontrollers and compact, highly integrated circuitry, we have minimized our PCB's Bill Of Materials (BOM) cost and maximized reliability, compatibility, and efficiency. Furthermore, the rising price of film [3] has created a glut of technologically advanced film cameras that are too expensive to operate (akin to an inkjet printer), ensuring that this conversion remains practical. In practice, our PCB and resulting conversion emulates the Kodak DCS460 digital camera conversion from 1995, but it benefits from modern 2025 electronics and is thus more compact, more functional, and more efficient.

This report will thoroughly detail the process and reasoning behind designing this device. Chapter 2 will give an overview of the overall PCB design and its main subsystems - the CCD and its supporting hardware, the power supply rails, the microcontroller, and the battery management system. Chapter 3 will focus on steps taken to verify the functionality of this design, Chapter 4 will provide a cost analysis of the design process, and Chapter 5 will wrap up the report by detailing key functional aspects of the completed device and possibility for future work. This report will also include references to existing projects that were used to derive inspiration and technical solutions during the design process to further provide context behind certain design decisions.

2 Design

2.1 Introduction

The self-contained module is composed of four subsystems: the CCD sensor and its accompanying circuitry, the power supply, the microcontroller, and the battery and its charging and protection circuitry. The module explicitly targets one film camera, the Nikon N90s from 1994, but could potentially be adapted to other cameras with minimal software changes.

We base the design's functionality off of a set of high level requirements that we laid out in the beginning of the design process. These requirements were prescribed as follows:

- The completed module will connect to the Nikon N90s camera, and it will save 6 Megapixel color images in uncompressed RAW format.
- The UI will consist of, at minimum, 3 buttons (Delete, Navigate, Select) and a dot-matrix display for status readout.
- The module will accept and save images to SDHC/SDXC cards of at least 32GB capacity.
- The module can be charged over USB-C.
- The N90s camera and module will shoot at a rate of 1 picture per second, with no loss of data.

The organization and functionality of the four subsystems remained constant throughout the semester, but minor tweaks were made to component selection. Due to thorough initial research, many of these requirements proved reasonably attainable, and our final design meets or needs minimal modifications to meet these requirements.

The expected bottlenecks in the design's component choice did not prove to be major limitations, and no major unforeseen limitations appeared. However, these weaknesses do limit future growth of the design. The most notable limitations are centered around the microcontroller, as its single-core architecture and sparse resources limit headway for additional software features and faster image readout and saving.

2.2 Design

The design process prioritized functionality and correctness, cost-effectiveness, and the use of efficient, modern parts and design practices. These concerns were evaluated for each subsystem, and the impact of these concerns is described in detail in each subsystem's section.

The subsystem breakdown can be seen in Figure 1:

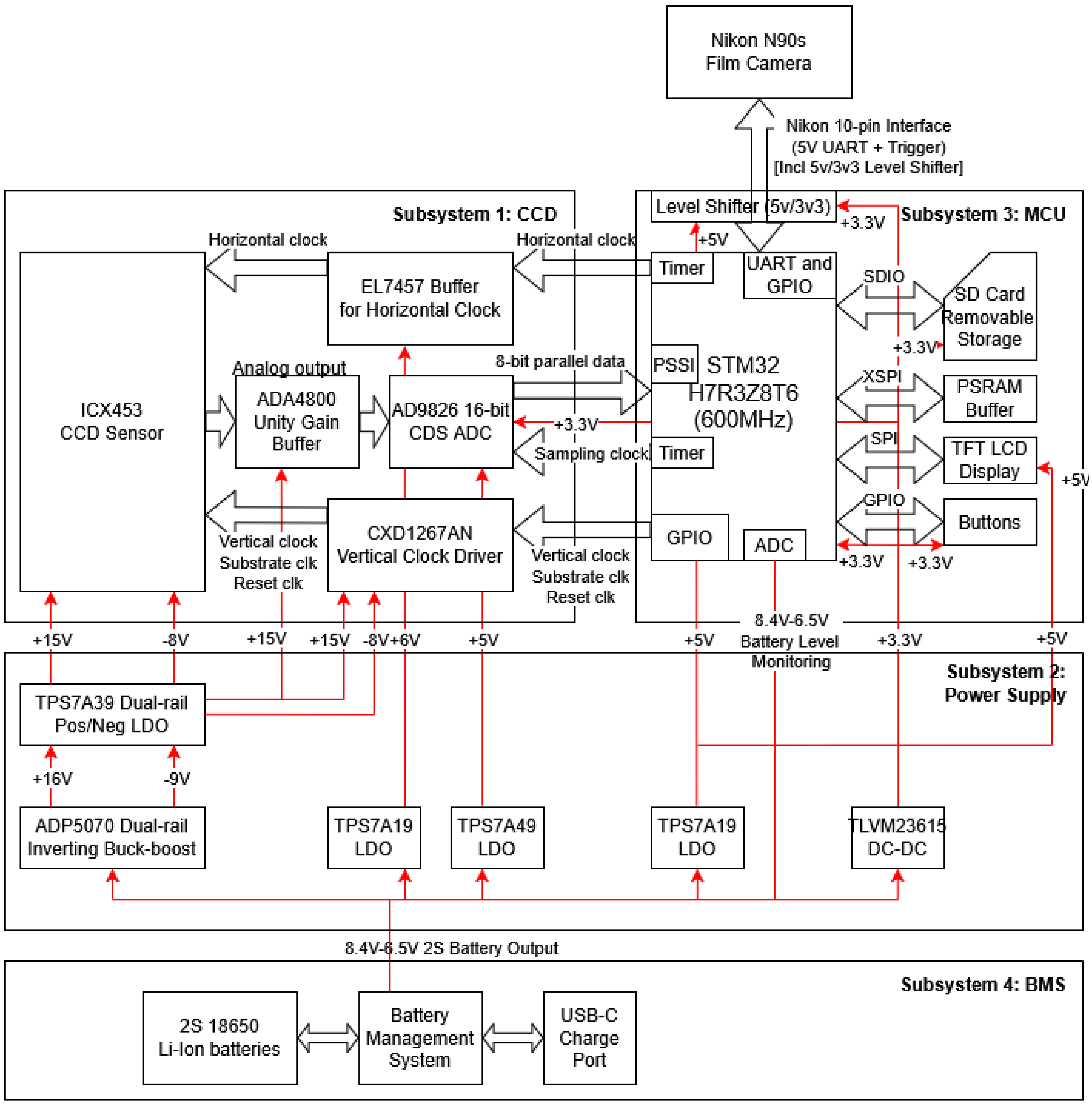

Figure 1: High-level block diagram

2.3 Subsystem Overview

2.3.1 Subsystem 1: CCD sensor, driving circuitry, and A-D

Subsystem 1 is responsible for properly driving the CCD sensor, and it sends digitized pixel data to Subsystem 3. We are intimately aware that driving the CCD sensor is not only the most critical and irreplaceable part of our project but also the most error-prone part of our project. Thus, our design borrows many aspects of the parts selection, operation, and schematic of Subsystem 1 (as seen in Figure 2) from the well-proven open-source CAM86 [4][5][6][7][8] astrophotography camera project. To cut cost and improve parts availability, we replaced the AD811 buffer amplifier used in CAM86 with the ADA4800 used in another CCD camera project, the Sitina1.

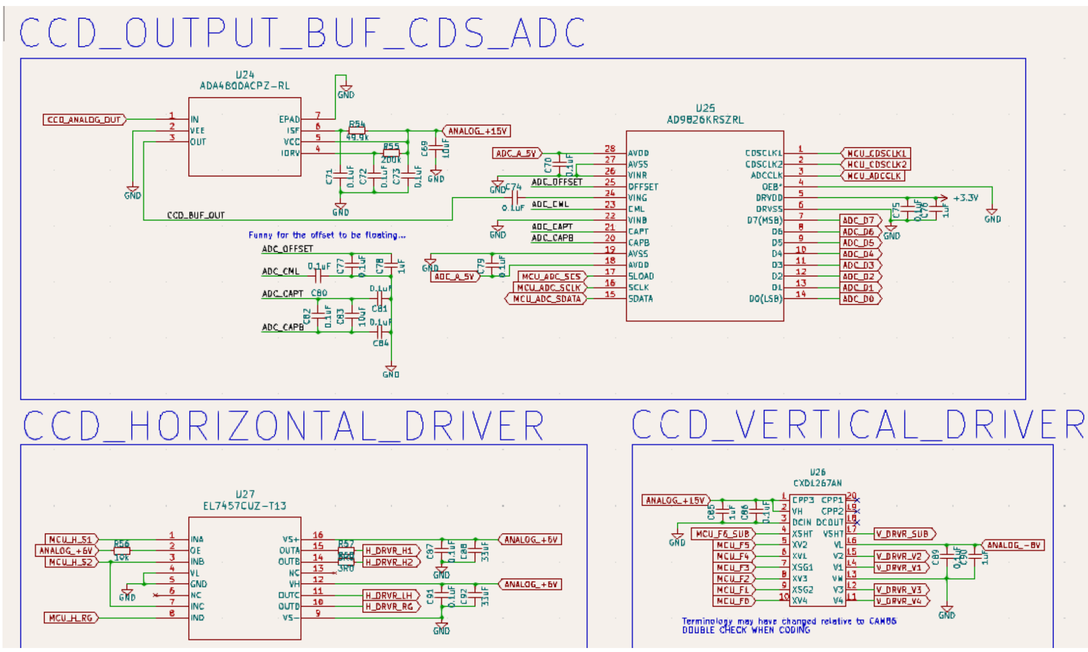

Figure 2: CCD driving circuitry schematic

This subsystem includes the Sony ICX-453 CCD sensor as salvaged from old cameras, CXD1267 CCD vertical clock driver, EL7457 horizontal clock driver, ADA4800 low-noise buffer, and AD9826 16-bit CDS ADC. Our emphasis on verifying this design prior to PCB manufacture have paid off, as the design flawlessly tolerates our design's operating CCD clock frequency of 12.5MHz (in contrast to the original design's 4MHz CCD clock frequency). This layout can be seen in Figure 3.

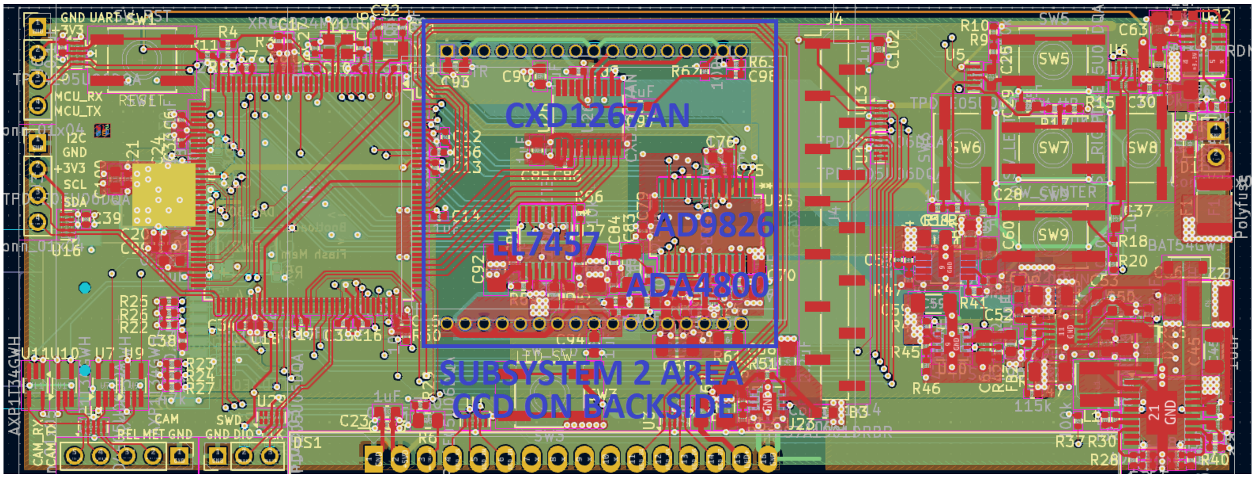

Figure 3: Subsystem 1 PCB layout

2.3.2 Subsystem 2: Power supply system

The ICX453 CCD sensor requires +15V, -8V, and +6V and may draw moderate current at times due to its large capacitances. Additionally, the supporting circuitry in Subsystem 1 and Subsystem 3 (Microcontroller, SDcard, and UI) will require 5V and 3.3V rails to support their components. This totals to 5 discrete voltages used in our project, powered by 2s Lithium Ion battery cells (a source that varies between 6.5-8.4V)

The power supply architecture for our project primarily targets low noise and secondarily targets a small footprint and good power efficiency. Low noise is necessary since Subsystem 1 is partially analog and generates digital picture data, so best picture quality requires careful power rail noise suppression. Footprint and power efficiency considerations are driven by the desire to minimize Size, Weight, and Power (SWAP) on a hand-held, battery-powered device. The resultant layout can be seen in Figure 4.

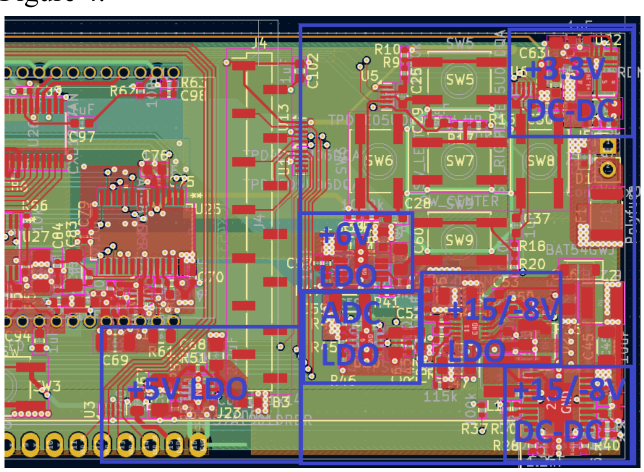

Figure 4: Subsystem 2 PCB layout

Correspondingly, we are implementing a multi-rail power supply architecture that emphasizes compactness and low noise.

- +15V and -8V used by Subsystem 1 are created by DC-DC boost conversion (ADP5070) followed by low-noise LDO regulators (TPS7A39). Boost conversion is necessary to generate the negative voltage and the greater positive voltage with sufficient efficiency, while the LDO removes noise and isolates load transients.
- +6V used by Subsystem 1 is created by an LDO (TPS7A1901). This model is selected for relatively high current and good transient characteristics, as well as low noise and component count compared to buck converter solutions. The small drop from battery voltage also means that an LDO does not sacrifice much efficiency compared to a switching converter. The +6V rail especially emphasizes transient performance, since the CCD horizontal clock switches a load very frequently (at 12.5MHz).

  Figure 5 demonstrates why this LDO was selected: high PSRR at the expected noise frequency (1MHz of DC switching supply and 12.5MHz of CCD clock), low quiescent current, and safe high-current operation at the expected input battery voltage levels. Values are calculated using TI WEBENCH POWER.

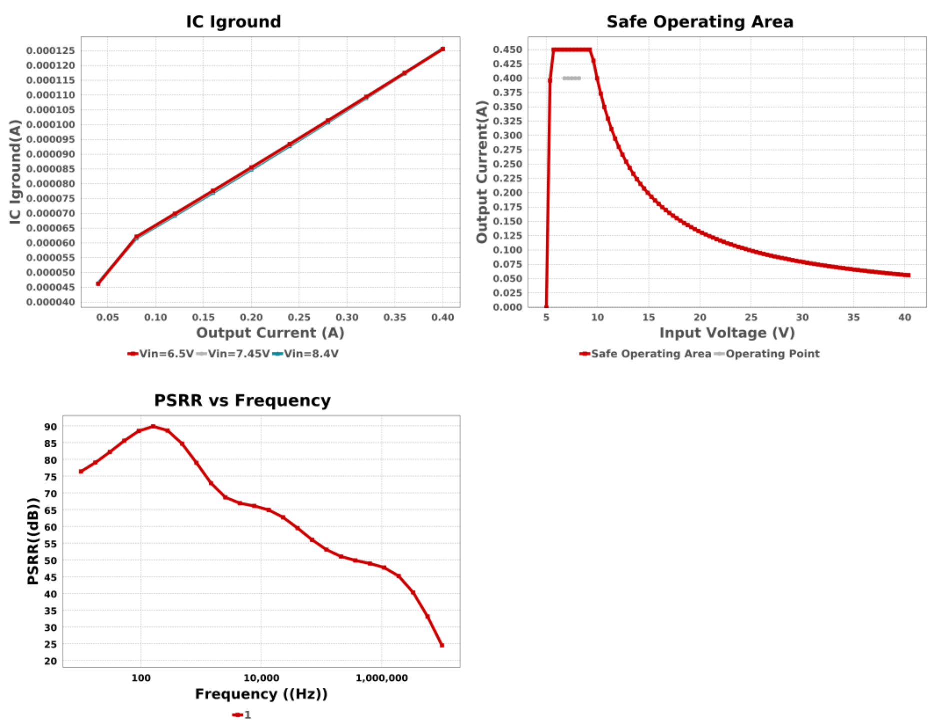

Figure 5: TPS7A1901 operating information graphs

- +5V used by Subsystem 3 is created by another LDO (TPS7A1901 again) primarily due to simplicity. While a switching converter would be more efficient, this is a lightly loaded rail primarily used for signalling.
- +5V used by the ADC in Subsystem 1 has a dedicated rail served by a special low-noise LDO (TPS7A49) in order to ensure the CCD readout analog circuitry is undisturbed by other component. We considered the efficiency loss compared to a switching component to be a worthy sacrifice.

The following specifications are highlighted in Figure 6 to show our selection criteria. Values calculated using TI WEBENCH POWER.

Operating Values

#	Name	Value	Category	Description
1.	Output Noise RMS	22.134 µV	General	Noise RMS
2.	IC Iground	853.814 µA	IC	IC ground current
3.	IC Pd	347.172 mW	IC	IC power dissipation
4.	IC Tj	52.011 degC	IC	IC junction temperature
5.	IC Tolerance	29.7 mV	IC	IC Feedback Tolerance
6.	ICThetaJA	63.4 degC/W	IC	IC junction-to-ambient thermal resistance
7.	Iin Avg	100.85 mA	IC	Average input current
8.	IOUT_OP	100.0 mA	Op Point	Iout operating point
9.	Input Ripple Frequency	10.0 MHz	Op Point	Input Source Ripple Frequency for PSRR Calculation
10.	PSRR est.	-47.72 dB	Op Point	Power Supply Rejection Ratio estimated
11.	VIN_OP	8.4 V	Op Point	Vin operating point
12.	Total Pd	347.172 mW	Power	Total Power Dissipation
13.	BOM Count	7	System Information	Total Design BOM count
14.	Efficiency	58.96 %	System	Steady state efficiency

Figure 6: LDO operating values table

- +3.3V used by Subsystem 3 uses an integrated-inductor switching DC-DC converter (TLVM23615) since the +3.3V rail is heavily loaded by relatively noise tolerant digital devices. Integrated inductor solutions are small, cheap, and reduce part count.

Layout focused on isolating noise sources and maximizing current handling capacity. Layer 3 was dedicated to power routing, and when this was insufficient some of the unpopulated back layer was also used. Vias were used extensively to ensure power planes and devices were well connected, power rails with high transient loads received generous bulk capacitance (within regulator specification), and special care was taken to ensure that all passives were well within operating tolerances even with temperature or age derating. Low ESR tantalum capacitors with generous voltage rating margin were used when X7R ceramics could not supply sufficient capacitance at the expected DC bias.

2.3.3 Subsystem 3: MCU, camera I/O, SDcard, User Interface

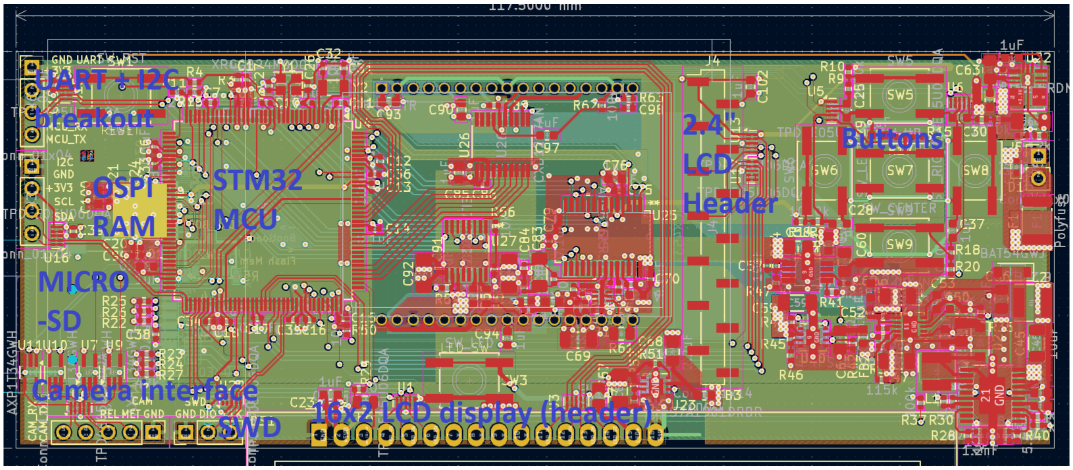

Figure 7: Subsystem 3 PCB layout

Subsystem 3 (as seen in Figure 7) consists of an STM32H7R3Z8T6 MCU, 128Mbit OSPI PSRAM buffer, SWD programming port, microSD card slot, user-accessible buttons, and a 2.4" color 320x240 LCD display. The MCU is responsible for the following:

- Controlling Subsystem 1 and receiving its image data. Clocks are generated with onboard timers or GPIO pins, and image data will be received with the DCMIPP/PSSI interface or GPIO pins.
- Controlling Subsystem 2 to implement power saving functionality. This is accomplished with GPIO pins.
- Monitoring battery voltage from Subsystem 4. This is accomplished with the onboard ADC.
- Synchronizing with the Host Camera through the camera's Nikon 10-pin interface (including a triggering signal and a serial interface for querying the camera's state and configuration)
- Buffering images to OSPI PSRAM to enable rapid shooting
- Processing and saving images to the microSD over SDIO, maximizing readout speed to flush the buffer as quickly and possible
- Accepting user inputs via button press and reacting accordingly, including configuration changes and a delete button that erases the most recently saved file. This will include the user-accessible power button, so that a power-off does not cause data loss.
- Driving the color 2.4" LCD display to display captured images or other graphics

We originally specified the STM32H7R3V8T6 (100 pin LQFP package), but switched to using the 144 pin STM32H7R3Z8T6 instead due to a shortage of pins. The additional pins eased PCB design by providing more flexibility, and enabled provisions for additional components such as a GPS module for geotagging and a light sensor for color balance. The STM32H7 family was selected for its high clockspeed, high-speed I/O, significant processing power, SDIO capability, XSPI PSRAM interface, and JPEG engine for real-time JPEG compression at minimum cost and without sacrificing realtime, responsive bare-metal operation. JPEG compression and requisite Bayer conversion, image playback, GPS tagging, or light sensing are still not part of the success criteria, but allocating for these features at design time dramatically enhanced our design's future growth potential.

As Subsystem 1 is largely based on the CAM86 [4][5][6][7][8] project, some of the code from CAM86 [4][5][6][7][8] was referenced or borrowed to form the interface between Subsystem 3 and Subsystem 1. Borrowed code required substantial revision due to the integration of substantially more functionality in this project, and the use of an STM32 MCU as opposed to CAM86's AVR MCU.

Subsystem 1 layout prioritized signal integrity, with high-speed devices such as the OSPI PSRAM, SDcard, and communication with the ADC and clock drivers being routed first. Slower clock signals and occasionally toggled signals were routed afterwards. Trace lengths were painstakingly matched to be within SDCard and PSRAM tolerances, and trace widths were selected in accordance with impedance calculations according to these components' specifications. The entirety of the second layer of the PCB was a ground plane, enabling healthy ground stitching and effectively shielding signals from interference. All devices received high-frequency decoupling capacitors on all power pins without exception.

2.3.4 Subsystem 4: Battery Management System

The final BMS subsystem utilizes the FM7021DB BMS and 8205LA switching FET to protect a pair of series-connected 18650 Lithium Ion rechargeable batteries. The BMS and FET are bundled together in a compact, low-cost, commercially available module that was soldered to a battery holder. As this module has been proven in a previous personal project, it was selected to minimize risk and cost.

An additional PCB module for powering the film camera from the BMS subsystem was also constructed. As constructed, this module uses the integrated-inductor TPSM84338 DC-DC buck converter to convert from the battery input to 5.5V (a nominal voltage for many 6V camera batteries). Special care was taken to filter this module's input and tune its output transient response, as the camera suddenly draws a large current upon operating its shutter and could insert noise back into the module's power source. This filter uses an inductor connected in series with the input power supply to minimize the current ripple exposed to the battery. To come up with the inductor value, the standard equation $L = \frac{(V_{in} - V_{out})DT}{\Delta I}$ was used and the inductor value was ascertained to be 2.7 uH. For this calculation we used a V_{in} = 7.5V, V_{out} = 5.5V, $f_{sw} = 700kHz$, ΔI = 780mA. The value for ΔI was chosen considering the batteries ESR to be 100 mΩ and an acceptable battery voltage ripple to be 1% of the battery output.

The output filter was designed to minimize the transient ringing at the camera input to ensure that the camera does not mistakenly believe its battery is dead. For this purpose, we used a feedforward capacitor to improve the converter's output rise time without creating problematic output overshoot. The capacitor was chosen according to the equation shown in Figure 8 provided in a TI general guide to optimize transient responses of power converters. [8]

$$\text{Cff\_op} = \frac{1}{2\pi \times f_{\_nocff}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Figure 11: TI general guide transient response optimization equation

3. Design Verification

Our process for verifying our design was unique to each subsystem. We started off with an LTSpice simulation to verify that the CCD sensor supporting circuitry would be capable of supplying signals that meet the CCD's input specifications. The CCD has significant parasitic capacitances and requires certain rise and fall times on its clocks. We can accurately calculate if our driving circuitry is capable of meeting these timings and transient current requirements using the equivalent circuit capacitances labelled on the CCD's datasheet and the known current carrying capabilities of the supporting circuits.

To test this, we constructed a simulation of the horizontal driving circuitry (as seen in Figures 12, 13) according to the CCD sensor's equivalent circuit. The EL7457 horizontal clock driver is specified to 2A current with an RDSon of 3Ohm, and the rise/fall times must be 5ns for 90% change. The LTSpice simulation below shows both these criterias are met; the transient current is around 1.2A and the rise/fall time for 90% change is around 3.3ns. With sufficient bulk capacitance, the +6V power supply should be capable of handling these momentary transients.

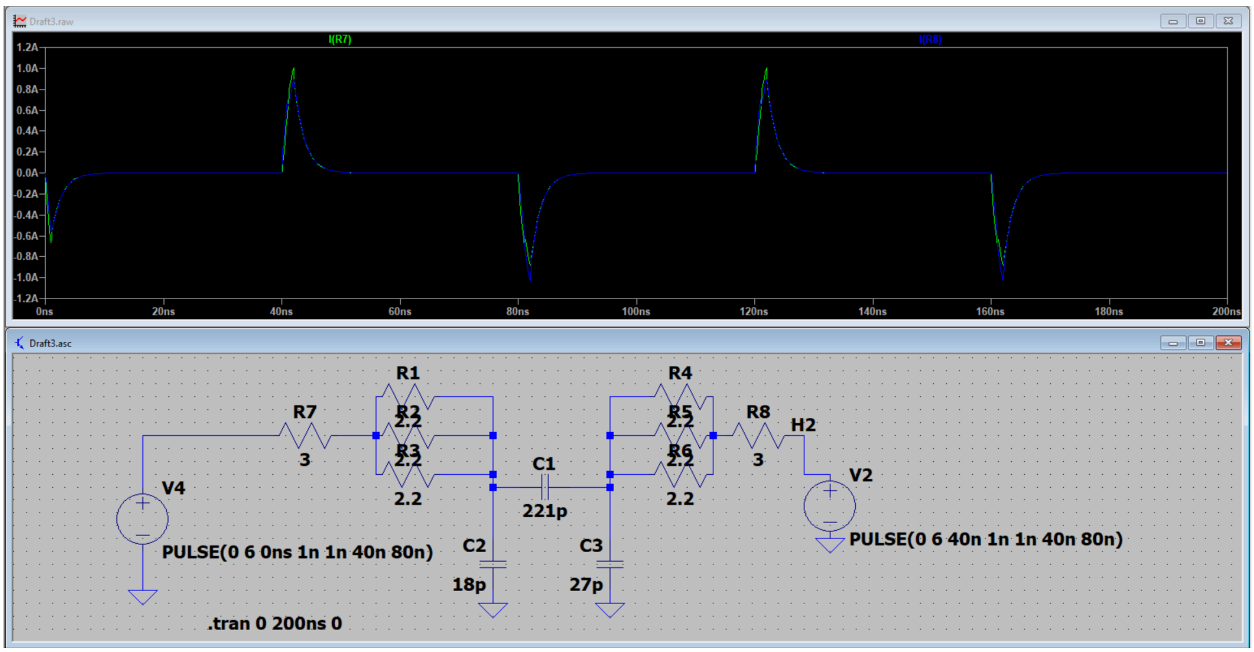

Figure 12: Horizontal driving circuitry simulation

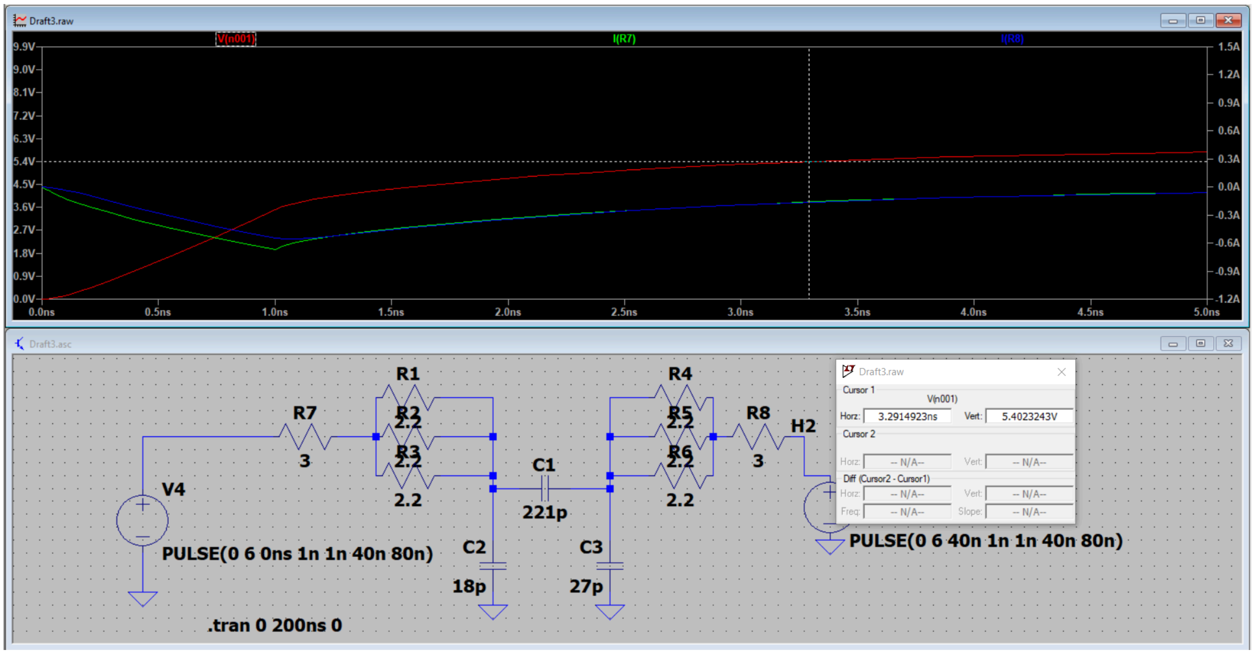

Figure 13: Additional CCD driving circuitry simulation

We recognized the importance that power rails would play in our design given the poor noise resilience of the CCD sensors. As such, once we had the physical PCB we prioritized testing our power rails. The rails and the BMS were tested using a multimeter and the results are detailed in the design and verification table in the appendix.

To verify the functionality of the physical CCD sensor subsystem 1 in conjunction with the MCU subsystem 3, we looked at the output of the CCD sensor being run with the clock generated using the MCU on an oscilloscope to conduct primary testing before actualizing these signals via an ADC. These results can be seen in Figure 14. This helped us confirm our driver code was functioning and our CCD sensors were working as expected without having to worry about the ADC mechanism in subsystem 1.

Figure 14: CCD & MCU conjunction test on an oscilloscope

Once our CCD sensors were determined to be functional, the ADC circuitry was verified by simply clicking a picture using the camera, shown in Figure 15 for reference. (The focus inaccuracy is a physical limitation.)

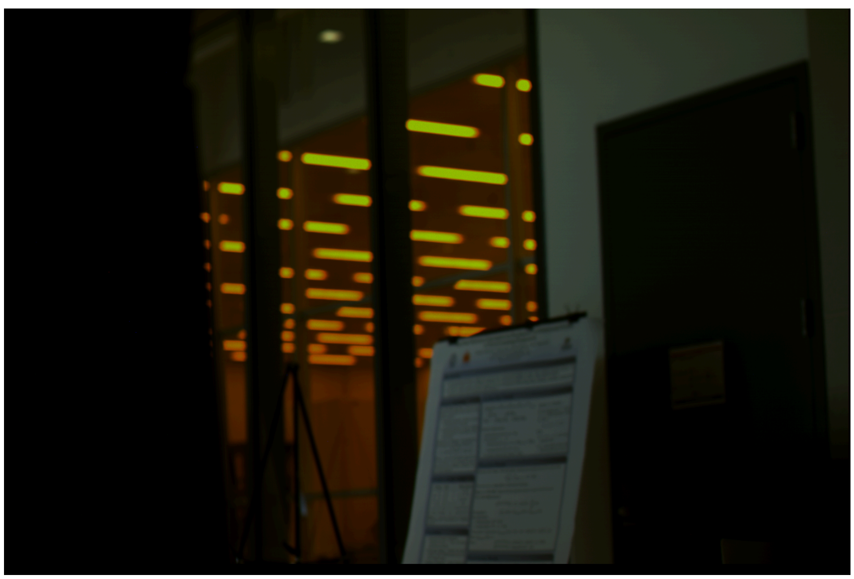

Figure 15: Example photo taken with the camera

4. Costs

4.1 Parts

Reference	Value	Datasheet	Footprint	Qty	LINK	PURCHAS	COST 4PCB
C1,C2,C3,C4,C5,C6,C7	0.1uF	~	Capacitor_SMD:C_0402_1005Metric	50	https://mou.sr/443	200	$3.00
C25,C28,C29,C30,C37,	1uF	~	Capacitor_SMD:C_0603_1608Metric	24	https://mou.sr/43m	100	$8.00
C26,C41	15pF	~	Capacitor_SMD:C_0402_1005Metric	2	https://mou.sr/3FN	10	$0.32
C27	22pF	~	Capacitor_SMD:C_0402_1005Metric	1	https://mou.sr/424	10	$0.21
C31,C32	10pF	~	Capacitor_SMD:C_0402_1005Metric	2	https://mou.sr/4jeR	20	$0.16
C40	1.2nF	~	Capacitor_SMD:C_0402_1005Metric	1	https://mou.sr/3QH	10	$0.31
C43,C56,C61,C68	2.2uF	~	Capacitor_SMD:C_0805_2012Metric	4	https://mou.sr/4kpc	16	$5.25
C44,C52,C57,C62	10nF	~	Capacitor_SMD:C_0402_1005Metric	4	https://mou.sr/4hP	20	$1.56
C45,C47,C69	10uF	~	Capacitor_SMD:C_1206_3216Metric	3	https://mou.sr/3DZ	12	$9.60
C48	4.7nF	~	Capacitor_SMD:C_0402_1005Metric	1	https://mou.sr/4jc3	10	$0.48
C49	68pF	~	Capacitor_SMD:C_0402_1005Metric	1	https://mou.sr/41jY	10	$0.21
C54,C66,C67	22uF	~	Capacitor_SMD:C_1206_3216Metric	3	https://mou.sr/3XI7	12	$4.69
C58,C60,C63	4.7uF	~	Capacitor_SMD:C_0805_2012Metric	3	https://mou.sr/3Fe	12	$7.37
C59,C88,C92	33uF	~	Capacitor_SMD:C_1206_3216Metric	3	https://mou.sr/41C	12	$6.19
C83	10uF	~	Capacitor_SMD:C_0805_2012Metric	1	https://mou.sr/3P4	10	$1.74
D1	ESD5Z12T1G	https://www.on	Diode_SMD:D_SOD-523	1	https://mou.sr/4lk4	10	$0.69
D2,D3	BAT54GWJ	~	Diode_SMD:D_SOD-123	2	https://mou.sr/4ljYr	10	$0.69
DS1	WC1602A	http://www.win	Display:WC1602A	1			
F1	Polyfuse	~	Fuse:Fuse_1812_4532Metric	1	https://mou.sr/4lnC	4	$3.24
FB1,FB2,FB3,FB4	100Î©	MPZ1608S101	Inductor_SMD:L_0603_1608Metric	4	https://mou.sr/3VB	16	$0.83
J1	Conn_01x03	~	Connector_PinHeader_2.54mm:PinHeader	1			
J2	MSD-4-A		Imported_Symbols_Footprints:CUI_MSD-	1	https://mou.sr/43p	4	$1.40
J3,J6	Conn_01x04	~	Connector_PinHeader_2.54mm:PinHeader	2			
J4	Conn_01x14	~	Connector_PinHeader_2.54mm:PinHeader	1			
J5	Conn_01x02	~	Connector_PinHeader_2.54mm:PinHeader	1			
J7	Conn_01x05	~	Connector_PinHeader_2.54mm:PinHeader	1			
L1,L2	8.2uH	7.44E+10	Inductor_SMD_Wurth:L_Wurth_WE-LQS	2	https://mou.sr/43k	8	$13.76
R1,R2,R29,R35,R37,R	100k	~	Resistor_SMD:R_0402_1005Metric	9	https://mou.sr/43x	50	$1.90
R3,R4,R8,R9,R10,R12,	10k	~	Resistor_SMD:R_0402_1005Metric	17	https://mou.sr/3W	100	$1.60
R5,R22,R23,R24,R25,R	47k	~	Resistor_SMD:R_0402_1005Metric	8	https://mou.sr/3Xo	40	$1.52
R6,R7,R61	750	~	Resistor_SMD:R_0805_2012Metric	3	https://mou.sr/41h	15	$0.59
R11	2M	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4c7	10	$0.09
R13	270K	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4ce	10	$0.26
R28	19.6k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4c7	10	$0.19
R30,R40	1.3M	~	Resistor_SMD:R_0402_1005Metric	2	https://mou.sr/3FO	20	$0.16
R31	115k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/42m	10	$0.08
R32,R39,R52	68k	~	Resistor_SMD:R_0402_1005Metric	3	https://mou.sr/4hP	20	$0.36
R34	5.49k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4j2y	10	$0.08
R38	130k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4lKC	10	$0.07
R44,R45	180k	~	Resistor_SMD:R_0402_1005Metric	2	https://mou.sr/4c7	20	$0.16
R47	56k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4j38	10	$0.18
R48	12k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4lM	10	$0.14
R49	27k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4l2l	10	$0.08
R53	22k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/3QR	10	$0.09
R54	49.9k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4j6D	10	$0.19
R55	200k	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/3Y6	10	$0.05
R57,R58	3R0	~	Resistor_SMD:R_0603_1608Metric	2	https://mou.sr/4l0K	10	$0.51
R59	100	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/3FY	10	$0.13
R60	510	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4Uw	10	$0.13
R63	1M	~	Resistor_SMD:R_0402_1005Metric	1	https://mou.sr/4c9	10	$0.07
SW1	SW_RST	~	Button_Switch_SMD:SW_SPST_EVQQ2	1			
SW2,SW4	CJS-1200TB	CJS-1200TB	Imported_Symbols_Footprints:CJS-1200B	2	https://mou.sr/41tJ	10	$8.09
SW3	SW_LED	~	Button_Switch_SMD:SW_SPST_EVQQ2	1			
SW5	SW_UP	~	Button_Switch_SMD:SW_SPST_EVQQ2	1			
SW6	SW_LEFT	~	Button_Switch_SMD:SW_SPST_EVQQ2	1			
SW7	SW_CENTER	~	Button_Switch_SMD:SW_SPST_EVQQ2	1			
SW8	SW_RIGHT	~	Button_Switch_SMD:SW_SPST_EVQQ2	1			
SW9	SW_DOWN	~	Button_Switch_SMD:SW_SPST_EVQQ2	1	https://mou.sr/3E0	30	$6.69
U1,U3,U5,U6,U8,U12,	TPD4E05U06DQA	https://www.ti.c	Package_SON:USON-10_2.5x1.0mm_P0.	12	https://mou.sr/41k	100	$9.90
U2	S70KL1282GABHV020	S80KS5123GA	Imported_Symbols_Footprints:PG-BGA-2	1	https://www.digikey	4	$15.44
U4	STM32H7R3Z8Tx	https://www.st.c	Package_QFP:LQFP-144_20x20mm_P0.5	1	https://mou.sr/4h3	4	$34.04
U7,U9,U10,U11	AXP1T34GWH	AXP1T34GWH	Package_TO_SOT_SMD:SOT-353_SC-70	4	https://mou.sr/4bq	20	$4.92
U18	ADP5070AREZ	https://www.an	Package_SO:ETSSOP-20-1EP_4.4x6.5mm	1	https://mou.sr/43B	4	$35.16
U19	TPS7A39	https://www.ti.c	Package_SON:Texas_S-PVSON-N10	1	https://mou.sr/4ldD	4	$19.00
U20,U23	TPS7A1901DRBR		Imported_Symbols_Footprints:IC_DRV86	2	https://mou.sr/4h7	10	$10.70
U21	TPS7A4901DGNR		Package_SO:HVSSOP-8-1EP_3x3mm_P0	1	https://mou.sr/3EZ	4	$11.12
U22	TLVM23615RDNR	TLVM23615RI	Imported_Symbols_Footprints:QFN-FCM	1	https://mou.sr/4hV	10	$16.90
U24	ADA4800ACPZ-RL	ADA4800ACP	Imported_Symbols_Footprints:CP_6_4_A	1	https://mou.sr/4h8	4	$10.60
U25	AD9826KRSZRL	AD9826KRSZ	Imported_Symbols_Footprints:RS_28_AD	1	https://mou.sr/4kor	4	$63.36
U26	CXD1267AN		Package_SO:SSOP-20_4.4x6.5mm_P0.65	1			
U27	EL7457CUZ-T13	EL7457CUZ-T	Imported_Symbols_Footprints:QSOP16_4	1	https://mou.sr/42e	4	$31.84
U28	ICX453		Imported_Symbols_Footprints:DIP2625W	1			
Y1	XRCGB24M000FFS1DR0	~	Crystal:Crystal_SMD_2520-4Pin_2.5x2.0	1	https://mou.sr/41D	4	$1.84
Y2	ECS-.327-9-34B-C-TR	~	Crystal:Crystal_SMD_3215-2Pin_3.2x1.5	1	https://mou.sr/3F1	4	$2.20

Figure 16: Bill of materials

4.2 Labor

Given our passion for this project, we have gone above and beyond what would be expected for a hobby project of this magnitude. We paid special attention to professional design details such as trace length and impedance matching, noise shielding, power plane noise and current carrying capacity, proper component selection and appropriate derating, and other small details to make sure our first PCB design was also our last PCB design. This resulted in an unusually intensive board development time and cost, but this decision paid off as only a few minor field modifications and no major redesigns of the board were required. The early completion of the board design enabled the board bringup and software work to proceed as quickly as possible, which was necessary as the major subsystems could not be breadboarded due to their highly integrated, extremely EMI sensitive design. Developing the STM32 microcontroller firmware and integrating it with the rest of the board also required monumental time expenditure, as the tight timing and high frequency requirements of the CCD subsystem, PSRAM buffer, and SDcard storage required the correct use of many unforgiving and esoteric hardware features of the microcontroller. As we were all new to STM32 programming, this required days of browsing documentation and trial and error. In general, we have expended exceptional effort in order to make a very compact and efficient solution that should genuinely be consumer-ready on the hardware side, which is beyond the proof of concept needed for this class. As such, our calculated labor costs are unusually high.

Labor cost estimate = $25/hr X 2.5 X (150 hours PCB design + 150 hours board bringup and programming) = $18,750

Total cost ~ $18,750

5. Conclusion

5.1 Accomplishments

Our project accomplishes all of its primary goals, with some firmware modifications. The CCD sensor module is successfully able to save 6 megapixel raw image files. It can save images at a rate of 1 image per second, to a 32 gigabyte microSD card. The module can use a d-pad button configuration to review and delete photos, should the firmware support it. The module's BMS system can charge over USB type C, and prevents overcharging and over discharging.

We additionally added an implementation of the "Gray-World" automatic white balancing algorithm on the CCD sensor module, and a secondary power conversion PCB that enables the camera to be powered over the same battery as the CCD sensor module.

5.2 Uncertainties

The CCD sensor module and PCB has a small handful of hardware limitations, which may limit future growth of the design. One of these limitations is the small size of the PSRAM buffer. Since the buffer is only 16 Megabytes, only one 16-bit per pixel raw image can be stored at a time. This means that bit depth reduction or on-the-fly compression is necessary to buffer additional images for burst image shooting, forcing a quality vs speed tradeoff when programming the camera's firmware.

Another limitation that forces this quality vs speed tradeoff is the sole microcontroller's single-core nature. While our firmware made extensive use of hardware peripherals that required minimal CPU time, the gray-world white balancing algorithm and any other potential image processing steps contend for limited CPU time that is also needed for accessing the SDcard's file system and writing the image files. This contention forces image processing to be minimal or nonexistent for fast image saving, or for image saving to slow down if additional processing steps are conducted on-camera.

A few minor PCB design mistakes were correctable and pose no limitations on future development, but should be fixed prior to any further future production. The TFT LCD screen connector was accidentally reversed, resulting in an awkward user interface. This issue can be corrected with external wiring or housing changes. Additionally, the 3.3V USB power rail on the STM32 microcontroller was left unconnected, resulting in errors when attempting to program the microcontroller. This issue was resolved by soldering an additional wire to the unconnected pin.

5.3 Ethical considerations

Use of Open-Source Work

Our work builds upon a combination of open source projects ported to our specific needs, as such we recognize the ethical responsibility of properly attributing and adhering to licensing terms when reusing such work. In alignment with the ACM Code of Ethics (1.5), which promotes giving appropriate credit and respecting intellectual property rights, we will ensure that all borrowed concepts or code are properly cited and comply with the original licenses.

Reverse Engineering of Sensor Inputs

Due to the limited documentation available for CCD sensors, we may need to reverse-engineer some sensor inputs. We will ensure that this process does not violate proprietary rights or confidentiality agreements. The IEEE Code of Ethics (7.8.I.4) urges engineers to avoid engaging in practices that could be considered unlawful. As such, we will only use legally obtained resources and publicly available data for reverse engineering.

Battery Management and Power Safety

Since our device will utilize Li-ion batteries, we will integrate a Battery Management System (BMS) to mitigate risks such as overcharging, overheating, or short-circuiting. This aligns with industry standards, such as IEEE 1725 for rechargeable battery safety. Furthermore, we will follow proper disposal and recycling guidelines as outlined in environmental regulations, ensuring compliance with both federal and state policies on battery waste management.

Laboratory Safety Compliance

Our development and testing will take place in University of Illinois laboratories, requiring strict adherence to campus safety policies. This includes compliance with electrical safety protocols, proper handling of PCB components, and adherence to lab-specific regulations to minimize hazards.

5.4 Future work

Since our hardware design proved sufficiently robust, our module has multiple avenues for future growth into a unique, marketable product. Many of the software features and niceties of a modern digital camera can be refitted to our design with additional firmware development. Our implementation of a rudimentary white-balance algorithm is a proof of concept for additional image processing steps, such as debayering, upscaling, and image compression. If all of these steps are implemented, a high-quality, ready-to-use, and aesthetically pleasing image can be directly saved to the SDcard. These steps may impact sequential image-taking speed, but enabling or disabling these features can be left as an option for the user. While the extra pinouts reserved for peripherals such as light sensors, GPS modules, and segmented or dot-matrix LCD displays were unpopulated in our design at the time of writing, these pinouts remain available for future quality of life improvements such as ambient light white balancing, geotagging and GPS-based time tagging, and a more complete user interface.

Another possible avenue of development is to adapt the existing hardware to fit a different film camera. The Nikon N90s single-lens reflex camera was used in our implementation as it was available on-hand and its electrical interface was well understood. However, nearly any other film camera that our board can physically fit on can be adapted, so long as a new physical support bracket is constructed and a new electrical interface with the film camera is programmed into the MCU’s firmware. Our module thus contains the potential to adapt plentiful point-and-shoot film cameras into popular and marketable CCD “digicams”. Such an amalgamation can even deliver greater dynamic range and depth of field than commercially available digicams by leveraging its uniquely large CCD image matrix size.

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Appendix A Requirement and Verification Table

Requirement	**Verification**	**Verification Status**
+15V for subsystem 1 <5% variation	Multimeter readout	Y: 14.787V
-8V for subsystem 1 <5% variation	Multimeter readout	Y: -8.087V
+6V for subsystem 1 <5% variation	Multimeter readout	Y: 5.99V
+5V for subsystem 1 <5% variation	Multimeter readout	Y: 4.989V
+5V for subsystem 3 <5% variation	Multimeter readout	Y: 5.065V
+3.3V for subsystem 3 <5% variation	Multimeter readout	Y: 3.247V
LCD image module functions as appropriate a) Successfully turns on b) Image can be drawn c) Image can be redrawn d) Orientation can be changed	Verify first using a development board to test driver code, then when added to the main PCB. Run the driver code on the PCB to perform the same tests.	Y

Figure 17: Requirement and verification table