# ECE 445

Fall 2024

Design Document

# Adaptive Response Digital Guitar Pedal

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# Introduction

## Problem

The original method of guitar amplification used vacuum tubes. While tube amplifiers sound great and are very responsive to the dynamics of the guitar signal (i.e. a quiet note has very little distortion and a loud one is quite distorted), they are heavy and expensive. Modern day solid state amplifiers are not very responsive to the dynamics of the signal, giving the player less flexibility when playing.

## Solution

We propose an adaptive response digital guitar pedal. This pedal would respond to the volume of the note played, and adjust the amount of effect accordingly. This would be a cheap, effective way to give the guitar player the responsiveness of a tube amplifier, without the cost of it. This same principle would be applied to other effects as well, allowing the player to adjust the amount of reverb, chorus, delay, or fuzz just by how lightly they pluck a string. This opens up a world of possibilities for the player, allowing them to adjust their sound on the fly. This effects pedal is mainly for the use of the player, to allow them to change their sound without making any adjustments to their amplifier or effects board. It is not something for the listener to notice. There will also be a compression switch, allowing the user to adjust the effect amount by playing a note at a different volume, but keeping the output volume at the same level.

## Visual Aid

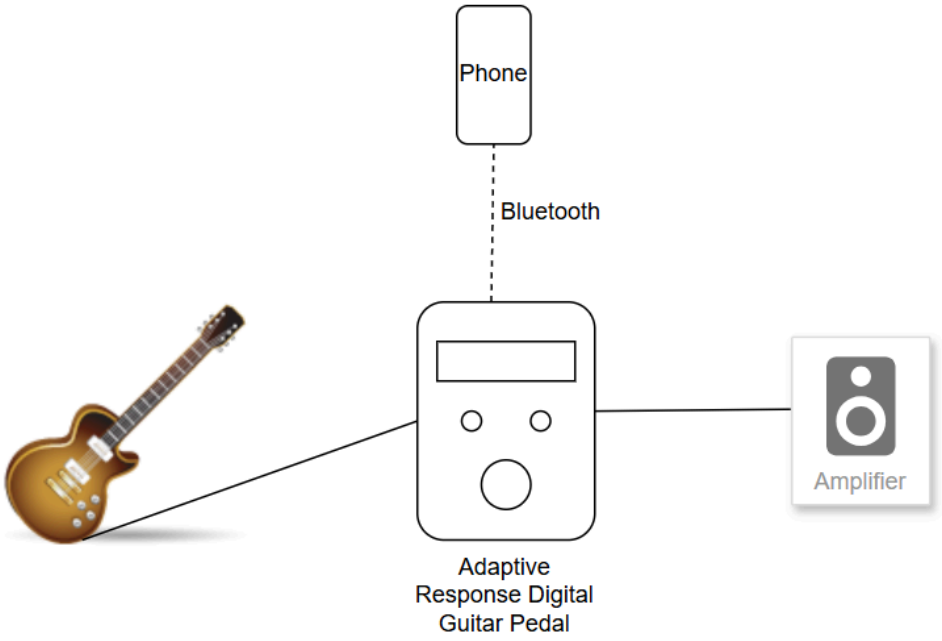


Figure 1: Visual representation of how the pedal fits in a typical guitar setup

## High Level Requirements

For a successful final product, our pedal must fill these three requirements:

Responsive: our unit will need to respond to the volume of the incoming signal to adjust the amount of effect being used

Power: The pedal must be designed to run from a 9V wall plug barrel jack, consistent with common guitar pedal designs (max 2A).

Low Latency: our design must process the guitar signal fast enough so that the player does not notice any delay in the signal. Ideally, the delay will be less than 12ms. [5]

# Design

## Block Diagram

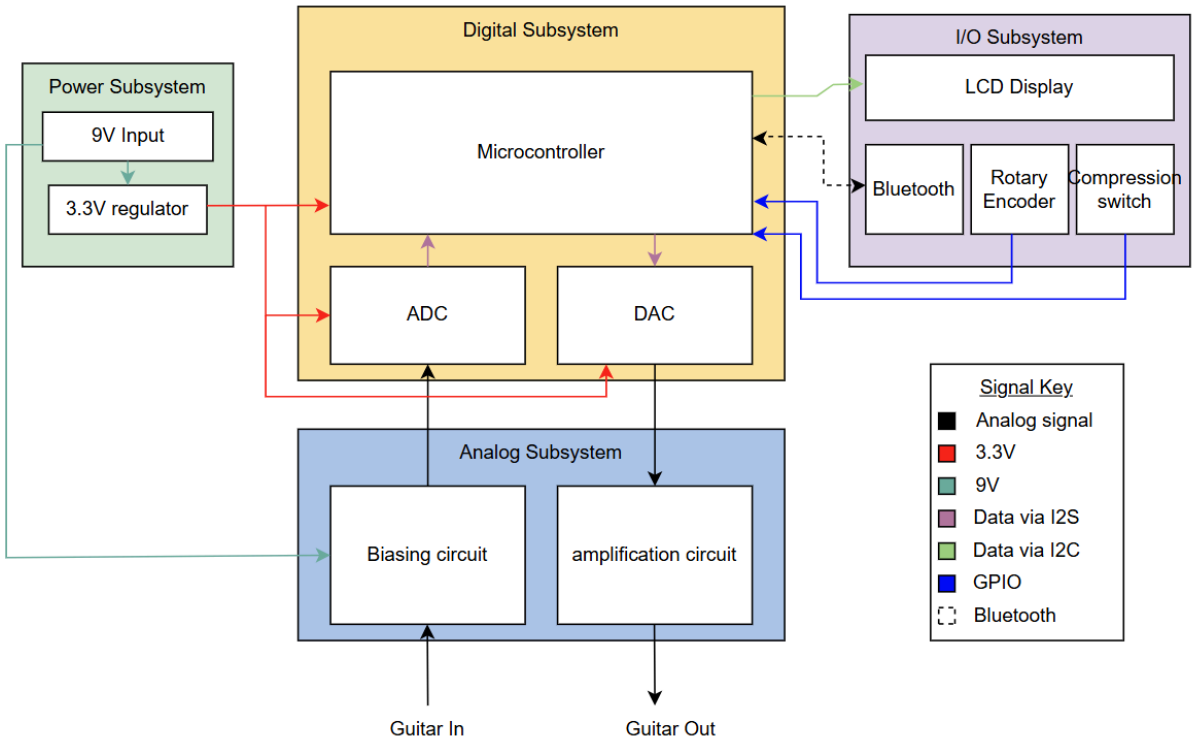


Figure 2: Block diagram showing subsystems and how they interact with one another

## Subsystem Descriptions

Analog Subsystem

The input guitar signal will need to adjusted to the proper voltage level before going into the ADC. It will also need to be amplified after the Digital-to-Analog converter (DAC) and before it is sent out of the pedal. This will be done via analog amplification circuits.

### Digital Subsystem

The microcontroller is what will perform the filtering and processing of the guitar signal. It will also manage the input/output (I/O) of the pedal, including the Liquid Crystal Display (LCD), rotary encoder, and compression switch. The microcontroller being used is the ESP32-S3.

The analog signal coming in must be converted to digital so that the microcontroller can process it. It also must be converted back to analog after the processing is done. We plan to use a 32-bit hardware controlled Analog-to-digital converter (ADC)/DAC to remove some strain from the microcontroller.

### Power Subsystem

The power of this board will come from a 9V wall outlet. We will have a regulator regulate the voltage down to 3.3V for the microcontroller, DAC, and ADC, and likely use the 9V for the digital subsystem.

### I/O Subsystem

The I/O subsystem is the interface that allows the user to control the pedal parameters. It will have a bluetooth interface, rotary encoder, LCD display, and compression switch.

## Subsystem Requirements

### Analog Subsystem

The analog subsystem must amplify the incoming signal and bias it to the voltage that the ADC requires. This will allow us to get the most accurate readings. We also must amplify the outgoing signal so that it is strong enough for the guitar amplifier.

## Digital Subsystem

The microcontroller must be able to run off of 500mA of current. It also must have enough pins to interface with the DAC, ADC, LCD display, rotary encoder, and compression switch. The microcontroller must be able to communicate via Inter-Integrated Circuit Sound (I2S) with the DAC and ADC. This is an efficient and quick way of transferring audio data [2]. It also must be able to communicate via Inter-Integrated Circuit (I2C) for the LCD display.

The ADC and DAC must both be 32 bit resolution and must both be able to sample at 44.1kHz. 32 bits of resolution is necessary for our product to ensure more accurate signals which is vital for music applications where subtle nuances in sound need to be captured. Ideally, they should communicate with the microcontroller via I2S. We must also set the pins of the ADC/DAC such that they have a sample rate of at least 44.1kHz. This is the industry standard sampling rate for audio applications [3].

## Power subsystem

The power subsystem must have separate regulators for the microcontroller, DAC, and ADC to minimize noise. The regulators for the ADC and DAC must be able to supply at least 50mA, and the regulator for the microcontroller must be able to supply at least 500mA. [4]

## I/O subsystem

The I/O subsystem must be able to compress the output volume such that the player can still adjust the amount of effect, but the output volume will be the same. It must also have a rotary encoder that can scroll through effects to select which one is being used. The LCD display must also properly display text

so the user knows which effect is being implemented. Finally, the On/Off switch must turn the effects on or off.

## Subsystem Verifications

### Analog Subsystem

**Input Signal Amplification**: To verify that the analog subsystem amplifies the incoming signal, apply a known input signal and measure the amplified output using an oscilloscope. The output signal must have the correct gain.

**Biasing for ADC Verification**: In order to ensure that the amplified signal is properly biased, measure the DC bias of the amplified signal using an oscilloscope to verify its centered at the correct bias point. The signal must be correctly biased within the ADC's input range to avoid distortion.

**Accuracy of ADC Readings Verification**: Verify that the amplified and biased signal allows the ADC to provide accurate digital readings. The digital output must accurately reflect the input signal.

**Outgoing Signal Amplification for Guitar Amplifier**: Ensure that the outgoing signal is amplified to a level that is strong enough for the guitar amplifier, which can be done by measuring the amplification of the output signal using an oscilloscope. The measured output signal should meet the required voltage level.

### Digital Subsystem

**Microcontroller Power Consumption Verification**: To ensure that the microcontroller operated within the 500mA current limit, measure the current drawn by the microcontroller using a multimeter. The current measured should never exceed 500mA under normal operating conditions.

**I2S Communication Verification for DAC/ADC/LCD**: To verify that the I2S is working for both the DAC and the ADC an oscilloscope can be used to observe the I2S signals between the microcontroller and the DAC/ADC. The communication must be stable, with clock synchronization and the data transmission at a sample rate of 44.1kHz.

**32-bit ADC/DAC Resolution**: To make sure the ADC and DAC operate with a 32 bit resolution, the configuration registers of each component can be inspected to confirm they are set to 32-bit resolution.

**ADC/DAC Sample Rate Verification**: By setting the sample rate to 44.1 kHz in the configuration registers of the DAC and the ADC, an oscilloscope can then be used to check the timing of the I2S signals, which must correspond to 44.1 kHz.

Power subsystem

**Noise Isolation Verification:** To ensure that the voltage regulators for the microcontroller, DAC, and ADC minimize noise, use an oscilloscope to measure the noise on the power lines for each component. The noise for the power lines for each component must be minimal

**Current Supply and Voltage Stability Verification**: To verify that the regulators for DAC and ADC supply at least 50 mA and the microcontrollers regulator can supply at least 500mA measure the current and voltage output of each regulator using a multimeter. Ensure that the current is within the necessary bounds and the voltage is stable with the specified limits.

**Thermal and Load Stability Verification:** To confirm the regulators operate within safe temperature limits and maintain stable output, measure the temperature of the regulators and monitor the voltage stability under different loads. The regulators must stay within safe temperature ranges and provide stable voltage under all load conditions.

I/O subsystem

**Adjustable Effect Verification**: Apply different effects with varying intensities and measure the output volume using an audio meter or oscilloscope. The output volume must remain consistent regardless of effect intensity, but the effect itself must be adjustable by the user.

**Rotary Encoder Functionality Verification:** Rotate the encoder to confirm that the system can cycle through the effects and select the one to apply. Ensure that the correct effects are done for each user input.

# Tolerance Analysis

To meet our goal of less than 12 milliseconds of latency, we need to account for the delays introduced by the ADC, DAC, and the processing on the ESP32-S3. Below is a breakdown of these components and their contribution to the overall latency.

1. ADC/DAC Conversion Latency

Both the ADC and DAC introduce delays in the signal chain. Based on our design, we assume the 32-bit ADC and DAC have a conversion time of 10 microseconds per sample. This results in:

$$\text{Total ADC/DAC latency:} \quad 10\,\mu s + 10\,\mu s = 20\,\mu s$$

2. Signal Processing Time on the ESP32-S3

The ESP32-S3, running at 240 MHz, is responsible for performing digital signal processing operations, including filtering, dynamic response adjustments, and effect modulation. Assuming 1500 clock cycles are used for processing each sample (optimized for low latency), the processing time is:

$$\text{Processing time per sample:} \quad \frac{1500\,\text{clock cycles}}{240 \times 10^6\,\text{clock cycles/sec}} = 6.25\,\mu s$$

This shows that the ESP32-S3 can handle the required DSP efficiently within a low processing time.

3. Total Latency Calculation

The total delay for each sample includes both the ADC/DAC conversion time and the signal processing time on the ESP32-S3:

$$\text{Total latency per sample:} \quad 20\,\mu s + 6.25\,\mu s = 26.25\,\mu s$$

At a 48 kHz sampling rate, the interval between samples is 1/48,000 seconds, or about 20.83 µs. To ensure we stay under 12ms of total latency, we will process a buffer size of 128 samples:

$$\text{Buffer latency:} \quad 128 \times 26.25\,\mu s = 3.36\,\text{milliseconds}$$

4. Conclusion

By optimizing the conversion times of the ADC and DAC to 10 µs and the processing time per sample to 6.25 µs, we can comfortably maintain a total latency of 3.36 milliseconds when using a 128-sample buffer. This is well below our goal of 12 milliseconds, ensuring that the player will not experience any noticeable delay in signal processing during performance.

# Cost and Schedule

## Bill of Materials

| Description | Manufacturer | Quantity | Unit Price | Extended Price | Link | |
|---|---|---|---|---|---|---|
| CONN JACK MONO 6.35MM PNL MNT | Amphenol Audio | 2 | 1.61 | 3.22 | Link | |
| DC Barrel connector | SCHURTER Inc | 1 | 1.64 | 1.64 | Link | |
| 5V wall plug | Triad Magnetics | 1 | 7.04 | 7.04 | Link | |
| 22 AWG wire | TE Connectivity | 5 | 1.17 | 5.85 | Link | |
| Heat Shrink - 1/8" | 3M | 50 | 0.0582 | 2.91 | Link | |
| Rotary Encoder | Bourns Inc | 1 | 1.49 | 1.49 | Link | |
| Knob | APEM Inc | 1 | 2.37 | 2.37 | Link | |
| LCD Display | Sunfounder | 1 | 9.99 | 9.99 | Link | |
| Stomp Switch - effect on/off | Lovermusic | 1 | 6.99 | 6.99 | Link | |
| Toggle Switch - Compression | Adam Tech | 1 | 1.16 | 1.16 | Link | |
| Enclosure | polycase | 1 | 9 | 9 | Link | |
| 4-Pin MTA100 headers | TE Connectivity | 2 | 0.21 | 0.42 | Link | |
| 4-pin MTA100 connectors | TE Connectivity | 2 | 0.38 | 0.76 | Link | |
| 3-Pin MTA100 headers | TE Connectivity | 1 | 0.18 | 0.18 | Link | |
| 3-pin MTA100 connectors | TE Connectivity | 1 | 0.24 | 0.24 | Link | |
| 2-Pin MTA100 headers | TE Connectivity | 5 | 0.17 | 0.85 | Link | |
| 2-pin MTA100 connectors | TE Connectivity | 5 | 0.22 | 1.1 | Link | I/O and misc components |
| ESP32-WROVER-E-N4R8 | Espressif Systems | 1 | 2.8 | 2.8 | Link | MCU and related components |

| | | | | | | |
|---|---|---|---|---|---|---|
| USB to UART converter (3.3V) | DSD Tech | 1 | 12.49 | 12.49 | Link | |
| 4 pin header (for UART programming) | Sullins Connector Solutions | 1 | 0.56 | 0.56 | Link | |
| Resistor - 10k, SMD, 0805 | Susumu | 6 | 0.1 | 0.6 | Link | |
| Button - to boot MCU, reset | C&K | 2 | 0.1 | 0.2 | Link | |
| Capacitor - 22uF - filter b/w power and gnd | Samsung Electro-Mechanics | 1 | 0.11 | 0.11 | Link | |
| Capacitor - 1 uF - Enable pin RC delay | Samsung Electro-Mechanics | 4 | 0.1 | 0.4 | Link | |
| Capacitor - 0.01uF | KYOCERA AVX | 2 | 0.1 | 0.2 | Link | |
| Capacitor - 0.1uF - filter b/w power and gnd | Samsung Electro-Mechanics | 6 | 0.1 | 0.6 | Link | |
| ADC - PCM1809 | Texas Instruments | 1 | 1.29 | 1.29 | Link | |
| DAC - PCM5102A | Texas Instruments | 1 | 4.95 | 4.95 | Link | |
| Resistor - 470 ohm | TE Connectivity | 2 | 0.1 | 0.2 | Link | |
| Resistor - 10k, SMD, 0805 | Susumu | 10 | 0.1 | 1 | Link | |
| Capacitor - 2.2nF | KEMET | 1 | 0.11 | 0.11 | Link | |
| Capacitor - 2.2uF | Murata Electronics | 2 | 0.11 | 0.22 | Link | |
| Electrolytic Capacitor - 1uF | Wurth Electronik | 1 | 0.16 | 0.16 | Link | |
| Electrolytic Capacitor - 10uF | Wurth Electronik | 7 | 0.18 | 1.26 | Link | ADC/DAC and related components |
| 3.3V regulator - 1A, MCU | Texas Instuments | 1 | 0.26 | 0.26 | Link | Power Subsystem |
| Resistor - 100k, SMD, 0805 | YAGEO | 2 | 0.1 | 0.2 | Link | |
| Resistor - 1k | Susumu | 1 | 0.1 | 0.1 | Link | |
| Op Amp | Texas Instruments | 1 | 2.81 | 2.81 | Link | |
| Capacitor - 150nF | KEMET | 1 | 0.22 | 0.22 | Link | |
| Potentiometer - 5k | Bourns Inc | 1 | 1.61 | 1.61 | Link | |

Analog Components

| | | | | | | |
|---|---|---|---|---|---|---|
| Potentiometer - 10k | Bourns Inc | 1 | 1.03 | 1.03 | Link | |
| TOTAL COST | | | | 88.59 | | |

## Schedule

| Week | Task | Person |
|---|---|---|
| 10/6-10/13 | PCB Design/Schematic | Will |
| | PCB Design/Schematic | Arya |
| | PCB Design/Schematic | Jack |
| 10/13-10/20 | Begin Prototyping | Will |
| | Order Parts | Arya |
| | PCB Review/Submission | Jack |
| 10/20-10/27 | Meet with Machine Shop to order enclosure | Will |
| | I/O Software | Arya |
| | DSP Software | Jack |
| 10/27-11/03 | Assemble Board | Will |
| | Assemble Board | Arya |
| | Assemble Board | Jack |
| 11/03-11/10 | Unit Test Power Subsystem | Will |
| | Unit Test Digital/IO Subsystem | Arya |
| | Unit Test Analog Subsystem | Jack |
| 11/10-11/17 | Submit PCB Revisions If Necessary | Will |
| | Program Board/Test with Guitar | Arya |
| | Program Board | Jack |

| | | |
|---|---|---|
| 11/17-11/24 | Mock Demo | Will |
| | Mock Demo | Arya |
| | Mock Demo | Jack |
| 11/24-12/1 | FALL BREAK | Will |
| | FALL BREAK | Arya |
| | FALL BREAK | Jack |
| 12/1-12/8 | Final Demo/Final Report | Will |
| | Final Demo/Final Report | Arya |
| | Final Demo/Final Report | Jack |

# Ethics and Safety

Our design involves digital signal processing and unique control mechanisms based on the dynamic response of the guitar input. To ensure compliance with ethical standards regarding intellectual property, we will conduct thorough research to confirm that our design does not infringe on existing patents or proprietary technologies. This aligns with IEEE's Code of Ethics, which urges engineers to be both forthcoming and fair when referring to available information.[6]

Regarding privacy, while our pedal does not handle personal user data, we still take privacy concerns seriously. For example, if the pedal were to be expanded to include features like Bluetooth connectivity or smartphone app integration in the future, we would ensure that any data collected would be managed with strict privacy protocols. IEEE, for instance, emphasizes the protection of personal information, ensuring that collected data is used solely for the purposes for which it was gathered, in line with applicable regulations and privacy policies [7]. In this way, we would guarantee that no unauthorized data collection or sharing would take place, ensuring the user’s privacy is protected.

Safety is another key consideration in our design. While the pedal operates at relatively low voltage (9V from a standard wall plug), it is still important to protect users from potential hazards. To ensure electrical safety, we will incorporate protective features such as proper insulation and overcurrent protection in the power subsystem. These features will mitigate the risk of electrical faults or short circuits that could harm the user or damage the pedal.

# Works Cited

[1]Sam-SoundGear, “Audio Sample Rate, Bit Depth, & Bit Rate Explained,” SoundGearLab, May 05, 2021. https://soundgearlab.com/learn/audio-sample-rate-bit-depth-bit-rate/ (accessed Sep. 30, 2024).

[2]“I2S Protocol: The Beginner’s Ultimate Guide – Flex PCB,” Flexpcb.org, Jun. 17, 2024. https://flexpcb.org/i2s-protocol-the-beginners-ultimate-guide/ (accessed Sep. 30, 2024).

[3] M. Rabiee, “Analog to Digital (ADC) and Digital to Analog (DAC) Converters.” Accessed: Sep. 30, 2024. [Online]. Available: https://sftp.asee.org/analog-to-digital-adc-and-digital-to-analog-dac-converters.pdf

[4] “Audio Interface 8x Interpolation Filter 32bit ΔΣ Modulator Current Segment DAC Current Segment DAC.” Accessed: Sep. 30, 2024. [Online]. Available: https://www.ti.com/lit/ds/symlink/pcm5102.pdf?ts=1727712486034&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FPCM5102

[5]C. Anderton, “Optimizing Latency with Computer Recording: How to Fix Your Audio Interface’s Delay,” *Reverb.com*, Aug. 18, 2018. https://reverb.com/news/optimizing-latency-with-computer-recording-how-to-fix-your-audio-interfaces-delay#:~:text=Most%20musicians%20would%20likely%20agree%20that%20latencies%20below%205%20ms (accessed Oct. 01, 2024).

[6] "IEEE Code of Ethics," IEEE, [Online]. Available: https://www.ieee.org/about/corporate/governance/p7-8.html. [Accessed: Oct. 3, 2024].

[7] IEEE, "IEEE Security & Privacy," IEEE, [Online]. Available: https://www.ieee.org/security-privacy.html. [Accessed: Oct. 3, 2024].