Gallium Nitride Based Modular DC-DC Converter for Electric Vehicle Auxiliary Systems

FINAL REPORT

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ABSTRACT

This report details the procedures and findings of Team 54 when creating a Gallium Nitride Based Modular DC-DC Converter as a ECE 445 Senior Design Project in Spring 2021. The goal of this project was to solve the efficiency problem that arises when auxiliary system DC-DC converters are run at low power. By having multiple low power converters that can be turned on and off at different times high efficiency at a wide range of powers is achieved. This report discusses the design, construction, testing process of the three main components that make up each converter module, which are the control logic, current sensors, and power converter. A final test was run with all components connected together resulting in efficiencies of above 85% for current draws between 1 A and 5 A. Though the test was run at 80 V, instead of the 400 V the system was designed for, the final result still verifies that such a system is viable. To conclude, a discussion of the ramifications of increasing the input voltage to 400 V discussed and future work that may improve the project is detailed.

TABLE OF CONTENTS

1 INTRODUCTION

1.1 Purpose

Electric Vehicle (EV) auxiliary systems such as air conditioning and heating systems can reduce the range of the vehicle by up to 35 % [1]. Auxiliary systems conventionally get their power from a 12-48 V auxiliary battery. Modern electric vehicles have large propulsion batteries, which power the motors of the electric vehicle. As such, many modern electric vehicles manufacturers opt to use the 200-800 V power supplied by the propulsion battery to power the auxiliary system. However, the voltage needs to be stepped down such that the low voltage (12-48 V) auxiliary systems are not damaged. This requires the use of a DC-DC converter, which changes DC power from an on-board 200-800 V propulsion battery into lower 12-48 V DC voltages to power auxiliary systems such as headlights, interior lights, wiper and window motors, air conditioning fans, heat pumps for the heater, and many other systems that are required within EVs [2] [3]. Most DC-DC converters are rated for high efficiency at high power. This means that they have a sharp drop in efficiency when run at lower power levels [4]. This is illustrated in Figure 1.
Our proposed solution is a modular DC-DC converter which consists of multiple converters that are efficient (> 90 %) at low power bands (60W-1000 W). When more power is required, more converters will be on and when less power is required, less converters will be on. This will allow efficient operation even when some auxiliary systems are idle and will help increase the range of the car. Furthermore, with the use of GaN power switches, a more efficient power converter can be designed which can tolerate higher voltage spikes allowing for a safer operation.

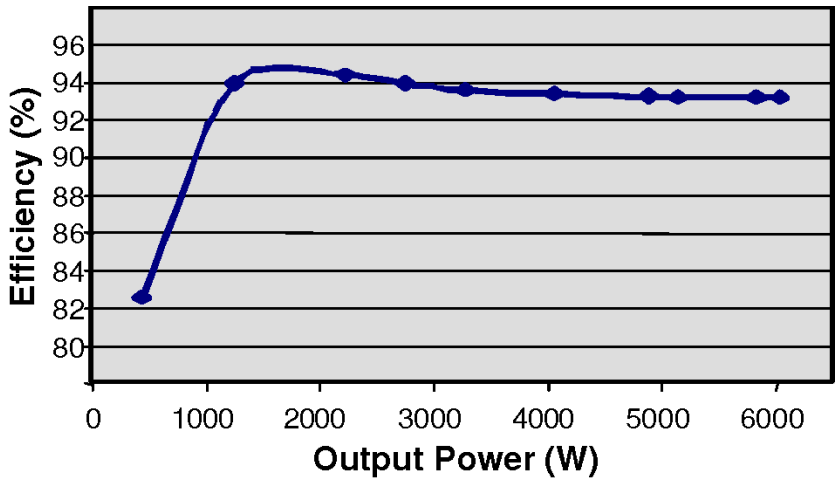

Figure 1: DC-DC Converter Efficiency vs Power Plot [5]

1.2 Functionality

As illustrated in Figure 2, there are 3 main components of the project which are: Current Sensor Units (CSUs), Control Logic, and Power Converter. Since our design is modular and converters need to be turned on/off to ensure high efficiency operation, we needed a way to check if more or less converters are required and then to turn the converters on or off. The CSUs, sense the current output of the converters, communicate to the control if more/less modules are needed. Based on the input of the CSU, the control logic provides the power switches in the converter with the PWM signal to turn the converter on and a ground signal to turn the converter off. Each subsystem has its specific considerations and justifications detailed in Chapter 2.

1.3 Overview

Figure 2 presents the block diagram for the converter system. The primary module is always on to ensure the auxiliary load never loses power and is connected in parallel to repeatable modules, which can be turned on based on the auxiliary load power draw.

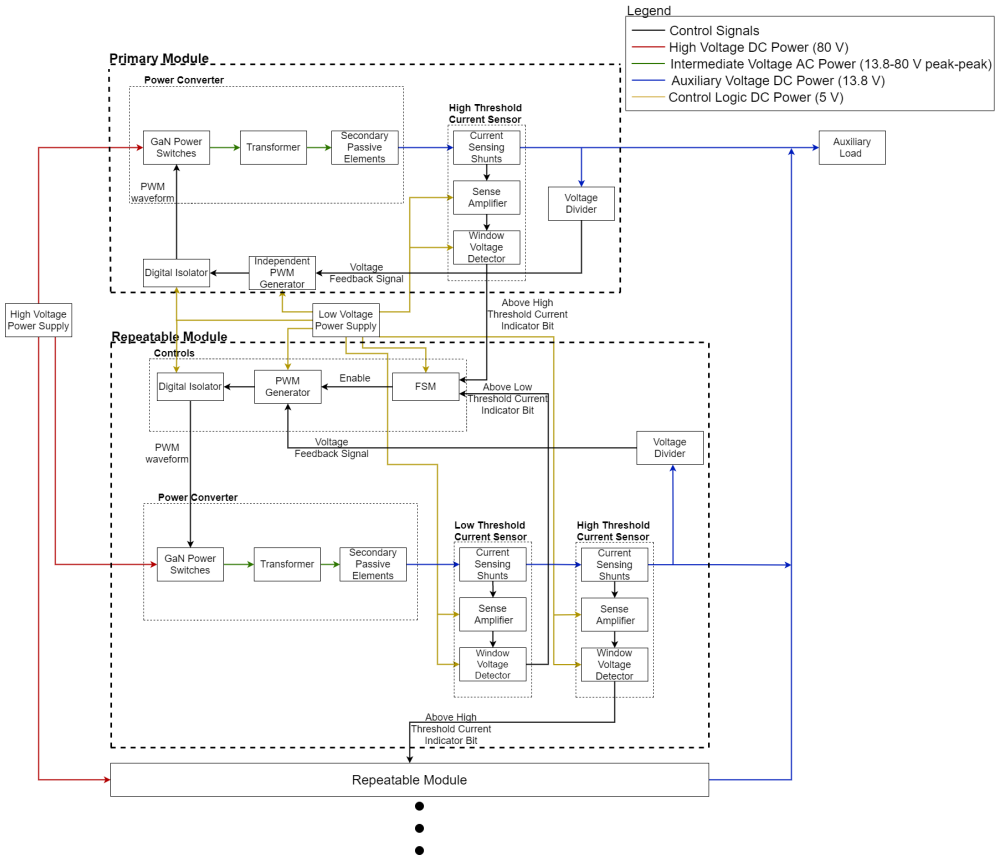

Figure 2: Block Diagram of Modular Converter System

2 DESIGN

2.1 Current Sensor Unit

Additional converter modules turn on when the current through the previous converter gets high enough that having more converters on would increase efficiency. The high threshold current sensor (HTCS), present in all converters, detects the current from the converter and outputs a logic high when the current goes above the threshold (5 A). The output of the HTCS is sent to the control logic of the next converter module to indicate when the next module should turn on. Whenever possible the fewest possible converters will be turned on to maximize efficiency. The low threshold current sensor (LTCS) detects the current coming from the converter and outputs a logic low when the current goes below the threshold value. The output of the LTCS for each module is sent to its own control logic to indicate when this module should turn off. The resulting threshold is illustrated in Equation (1) for the nth converter, where the nth converter is defined as the converter that turns on after (n-1) converters are turned on.

$$I_{low\ threshold} = \frac{(n-1)}{n} \times 5\ A \tag{1}$$

The CSUs use a current sensing shunt, a sense amplifier, and a window voltage detector to operate. The output current of the converter flows through the current sensing shunt, 2-4 mΩ, which is used to ensure that too much power is not consumed and efficiency stays high. The WSB58518 series power resistors were chosen as they can withstand currents above 20 A and have a high temperature tolerance up to 170°C [6]. The resistance value of the current sensing shunt is used to adjust the threshold of the current sensor. Equation (2) is used to calculate the resistance value (R_{SENSE}) given the voltage gain of the sense amplifier (A_v), the window voltage detector's internal threshold voltage ($V_{threshold}$), and the target threshold for the current sensor ($I_{threshold}$).

$$R_{SENSE} = \frac{V_{threshold}}{A_v \times I_{threshold}} \tag{2}$$

The sense amplifier detects the voltage across the shunt and amplifies it. We selected the LMP8640 sense amplifier for its high input resistance of 5 kΩ [7]. This prevents potential damage when high currents flow through the shunt. The sense amplifier output is used as an input to the window voltage detector which provides a logic output of high or low using an

internal threshold. The TPS3700 was chosen for a wide operating input voltage range (-0.3 V to 7 V), allowing for detection of currents up to 20 A [8]. This prevents the chip from being damaged if current spikes occur. Figure 3 presents the CSU schematic.

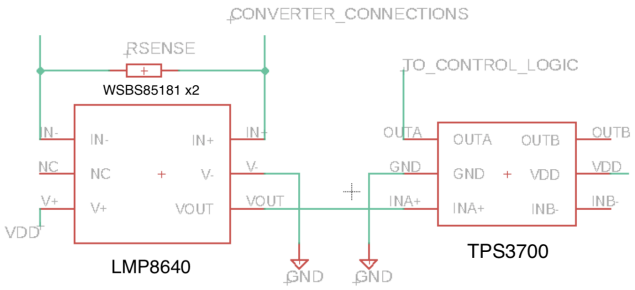

Figure 3: Current Sensor Schematic

2.2 Control Logic

The control logic uses the HTCS and LTCS to dictate if the converter should be on and outputs a PWM signal to the converters. The controls output is fed into the PWM driver on the high voltage converter board to turn on or off the power converter module. A PWM generator with shutdown capabilities is used to generate the PWM signal. FSMs are included in the controls to decide when the converter needs to be on. A synchronous system was chosen to prevent spikes and glitches in the output of the current sensor from reaching the PWM generator, which could lead to erroneous output.

The first FSM outputs the control bit, Converter_State, which indicates when the converter needs to be on (logic high) and off (logic low). The value of Converter_State is calculated using inputs from the previous module's HTCS (SENSE_HP) and this module's LTCS (SENSE_LC). A second FSM Power_Up was implemented to indicate when the converter is done powering up to ensure that the converter powers up fully before the control logic can decide to power it down. Power_Up will hold a logic low value while the system is in the process of powering up and a logic high when it is fully powered or fully powered down. The converter should turn on anytime the previous module's HTCS outputs a logic high signal and should stay on if this module's LTCS outputs a logic high signal or when the converter is still powering up. Figure 4 shows the FSM state diagram. The FSM was implemented using combination logic gates and D-registers. Parts selections and justification for these selections is presented in Table 9 in the Appendix B.

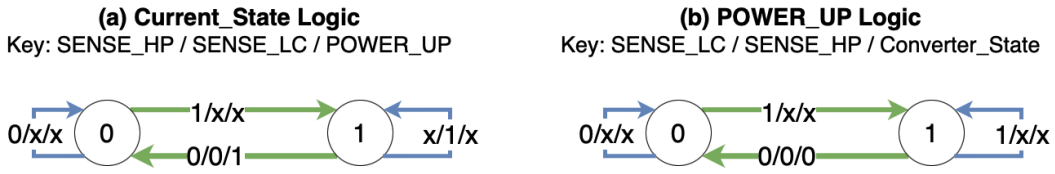

Figure 4: FSM State Diagram of Control Subsystem

The FSM output, Converter_State, is fed to the PWM generator as the ENABLE bit. When ENABLE is high, the PWM generator outputs the PWM signal to turn on the converter. When ENABLE is low the PWM generator will output 0 V to turn off the converter. The SG2524 PWM controller was chosen as it has a maximum duty cycle less than 50 % [9], which is required for a forward converter to prevent transformer core saturation as discussed in Section 2.3.2. Additionally, the SG2524 allows for the duty cycle to be adjusted, based on a voltage feedback signal coming from the output of the converter, to ensure the converter output is 13.8 V [9]. The target PWM waveform output has a frequency of 100 kHz, and a duty cycle of 39 % with adjustments made in accordance with the feedback voltage.

The main challenge faced when designing the control logic was designing the PWM Generator output driver. Figure 5 (a) presents the initial design with a 300 Ω pull up resistor and a pull down BJT as recommended in the data sheet. This design was unable to pull up. This was due to the recommendation in the data sheet assuming the PWM generator is powered using a 13.8 V. Our control board was powered by a 5 V, as such the PWM generator output driving mechanism needed to be adjusted. Both pull up and pull down BJTs were implemented, with complementary inputs into the BJTs. This solved the issue allowing the PWM generator output to be pulled up. The adjusted design is presented in Figure 5 (b).

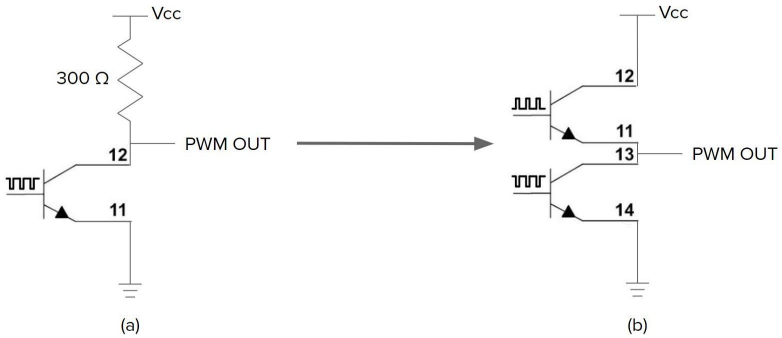

Figure 5: PWM Generator Output Driver

The last component in the design is a digital isolator. The output of the PWM generator is passed through a digital isolator before going to the high voltage converter board. The digital isolator prevents there being a direct electrical path between the high voltage board and the control logic board. This ensures the safety of the user by protecting the control logic from any voltage feedback from the high voltage board.

2.3 Power Converter

The power converter topology for each module is a Two-Switch Forward Converter. This converter is designed for 400 V input, but due to the equipment available in the laboratory we will be testing with 80 V. The output should be a 13.8 V DC signal. This converter topology is selected because of its high conversion ratio and transformer galvanic isolation to prevent a direct path from input to output. Furthermore, when current builds up in the transformer, the core may saturate and cause an increase in current destroying components of the circuit. The topology allows for leakage inductance and transformer current to be reset during the transistor's off-state, preventing transformer saturation. Figure 6 shows the power converter topology, and Appendix C shows the full circuit schematic for the power converter.

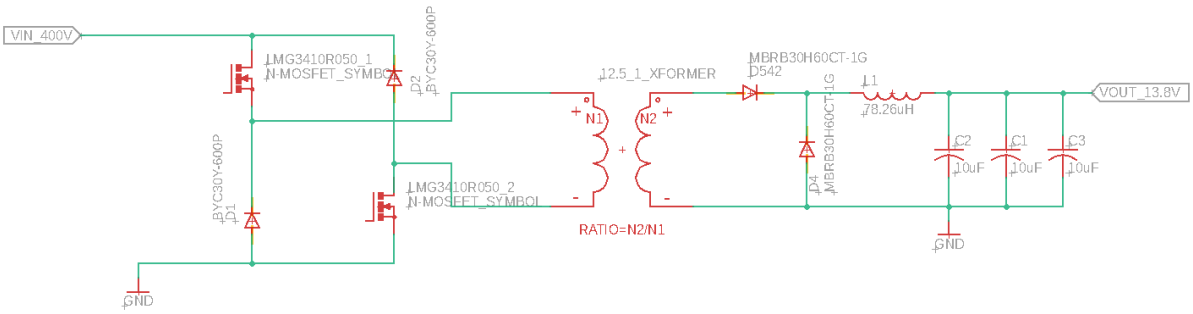

Figure 6: Basic Power Converter Circuit Schematic

2.3.1 *Power FETs*

The GaN FETs are used as our transistors power switches in the primary side of the converter. The TI LMG3410R050 was selected. This transistor was selected due to it's high voltage tolerance of ~600 V, built-in gate driver, and its ability to handle the switching frequency. The switching frequency is set to be 100 kHz to minimize component size. The sizing of passive

components such as inductors and capacitors are inversely related to the switching frequency, and these equations detailed in Section 2.3.3.

There were a couple challenges that arose from using the GaN FETs with integrated gate drivers from TI. The main issue was that there were several pins that needed to be connected properly, and because we misrouted the LPM (low power mode) pin on the chip, the gate driver was constantly in low power mode. This meant that the gate driver was essentially turned off. Cutting traces was difficult and because the pads were all underneath the chip, we designed a new PCB with the proper routing of LPM to 5 V. However, the board arrived much later than anticipated and we used the through-hole G12N60B3 Silicon Carbide (SiC) transistor. Although GaN is better for higher switching frequencies, SiC switches have a higher voltage tolerance (> 400 V) and can handle our selected 100 kHz frequency [10]. In Chapter 3 we show that we still achieve our desired high efficiency converter with SiC switches.

2.3.2 *Transformer*

The transformer is used to convert the higher voltage of 80 V to 13.8 V. The transformer also provides isolation, which ensures no direct path of current from high voltage input to the load. The conversion ratio of our power converter is determined by both the transformer turns ratio (N) and duty cycle (D), which is how long the switch is on per period, as indicated in Equation (3) and Equation (4).

$$\frac{V_{in} \cdot D}{f_{sw} \cdot N_1 \cdot A_c} \leq B_{sat} \tag{3}$$

$$V_{out} = D \cdot \frac{N_2}{N_1} \cdot V_{in} \tag{4}$$

Equation 3 is based off of Prof. Arijit Banerjee's ECE 464 course notes in Appendix D. Equation 4 is derived by manual analysis and is shown in detail in Appendix E. V_{in} is the input voltage, D is the duty cycle of the gate driver, f_{sw} is the switching frequency of the transistor, N_1 and N_2 are the number of turns on the primary and secondary side of the transformer respectively, and A_c is the cross-sectional area of the transformer core. The duty cycle needs to be below 50 % in order for the leakage inductance in the transformer core to be reset and prevent core saturation [11]. Using Equation (4), we decided to choose a turn ratio of 2.5:1, which satisfies our input voltage

(80 V) to output voltage (13.8 V) requirement and allows a duty cycle that is not too low but also below 50 %. If the duty cycle were to be too low, that would mean a longer time where the transistors are in their off state, leading to power loss through the secondary passive components such as the diode and capacitors. Initially, we chose our duty cycle to be 43 % based on these factors.

We decided to use the many selections of cores available in the power electronics laboratory so that we can test and modify the transformer if necessary. We tested using a ferrite core area of $140 \times 10^{-6}\ m^{2}$, with a maximum B_{sat} value of 240 mT [12]. N_1 must be larger than 10 turns in order to avoid magnetic flux saturation of the core. This estimation is derived from Equation (3). Thus, we selected N_1 to be 12, meaning that N_2 would be 6 in order to fulfill the turns ratio of 2:1. This is selected because it would lead to lower copper loss (energy lost as heat from the wire) than a transformer with more windings, which would be bulky on the circuit board, and also avoid core saturation for our selected transformer core.

We also tested our 2.5:1 turns ratio at 43 % duty cycle and the results we received were not desirable as the output was at 17.2 V, much higher than 13.8 V. After experimentation, we noticed that a 2:1 turns ratio resulted in better results and a 13.8 V output, and doing so also required our duty cycle to be reduced to 39 %. Figure 7 (a) shows our transformer and output voltage waveform at 2.5:1 ratio, and Figure 7 (b) shows our waveforms at 2:1 ratio.

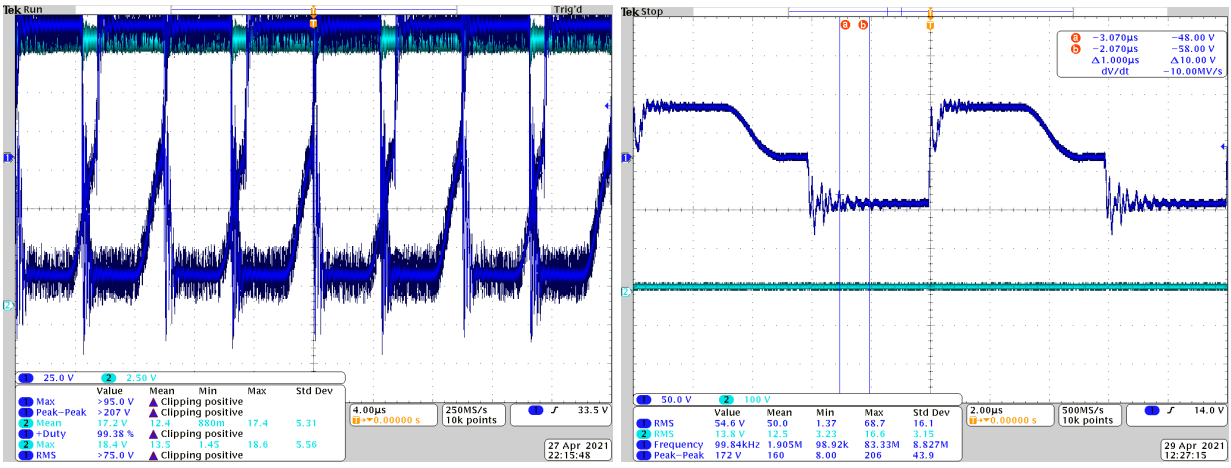

Figure 7: Transformer output and converter output with turns ratio of (a) 2.5:1 (b) 2:1

2.3.3 *Secondary Passive Components:*

Secondary passive components include the output capacitors, power diodes, and inductor. Equation (5) is used to determine the values of our output capacitor for our selected two switch forward converter topology [11].

$$C_{out} > \frac{\Delta I_{out}}{2 \cdot \pi \cdot f_{sw} \cdot \Delta V_{out}} \tag{5}$$

ΔI_{out} describes the maximum load current at the output, f_{sw} is the switching frequency, and ΔV_{out} is the ripple voltage across the output load. When putting our values of 10 A max current, 100 kHz switching frequency, and a ripple voltage that is 5 % of the desired 13.8 V output (0.69 V), we see that the output capacitance must be larger than 23 **µ**F. Therefore, we placed three 10 uF capacitors in parallel and also to decrease the equivalent series resistance of those components. For our inductor, Equation (6) was derived through our own calculations and referenced from the ECE 464 course notes, detailed in Appendix F. Using Equation 6, and applying our duty cycle D, N2/N1 turns ratio, and 100 kHz switching frequency, we decided to use a 78 uH inductor so that we can achieve a ripple current Δi_L of around 1 A.

$$\Delta i_L = \frac{(\frac{N2}{N1} \cdot V_{in} - V_{out}) \cdot D}{L \cdot f_{sw}} \tag{6}$$

The STPS30L30DJF power diode is selected for the output diodes D3 and D4. It has a 30 V reverse breakdown rating and supports up to 30 A of average forward current, more than the 10 A needed [13]. Moreover, this diode has a low forward voltage drop of 0.35 V. This means that the average power used will be approximately 10 A x .35 V, or 3.5 W. The diodes on the primary side of the converter, D1 and D2, support over 400 V of reverse voltage. The forward voltage of the diode had to be minimal because the power dissipated is the product of the average forward voltage and current. The Wolfspeed CSD01060E SiC diode, which supports up to 600 V of reverse voltage, is used [14]. This diode has a higher forward voltage of 1.6 but it is lower than most 600 V diodes needed for a 400V input. Furthermore, it also has a very small junction capacitive charge of 3.3 nC [14], so that there is not a long period to charge allowing faster switching without wasting energy. This is lower than most 600 V diodes.

3 DESIGN VERIFICATION

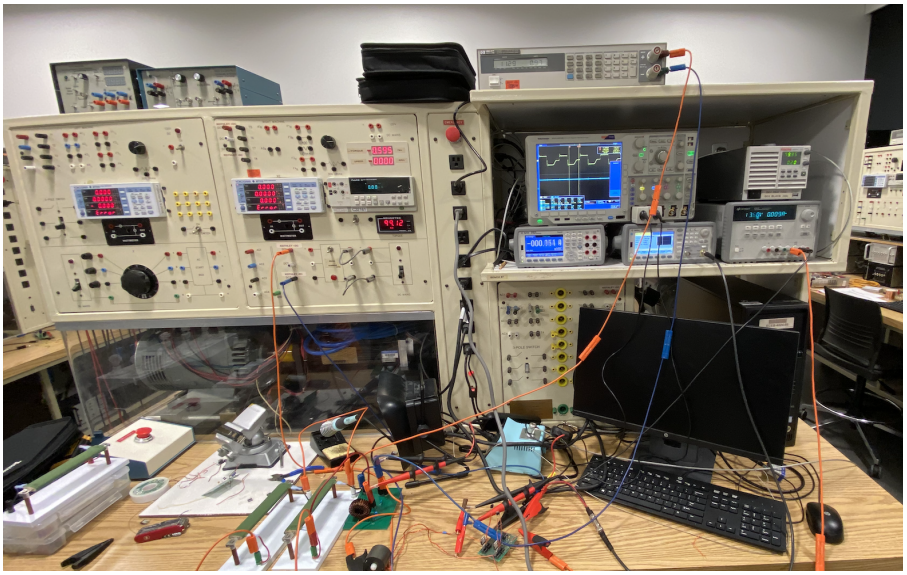

Figure 8: Setup in ECEB 4024

For the subsystem verification, we used an oscilloscope, multiple differential probes to probe the power converter, a multimeter for the CSUs, 5 V power supply which is use, 13.8 V power supply, 80 V power supply, and an electronic load to simulate the auxiliary load. Figure 8 shows the setup used for the verification in ECEB 4024.

3.1 Current Sensor Unit Verification

The main requirements for the CSU are as follows:

1. Outputs logic high within 10 % of the calculated threshold value (in our test case 5 A)
2. Current sensing shunt temperature remains below 170 ℃

Table 1 illustrates the results we measured during the testing phase for the CSU. The LMP8640 and the TPS3700 were powered using the 5 V supply. The shunt was connected in series with the electronic load to set the input current to ensure we do not damage the board. The output of the TPS3700, also the output of the CSU, was connected to a multimeter to measure the output voltage obtained at different current draws. It was crucial for us to ensure that the output of the CSU would be greater than the nominal high (3.8 V) and lower than the nominal low (1.6 V) required by the control to attain proper functionality [15].

Table 1: CSU Functionality

Input Current (A)	Output Voltage (V)	Temperature of Shunt (℃)
0.5	0.0095	27
1.0	0.0094	27
4.0	0.0095	30
4.5	0.0091	32
5.0	0.0095	33
5.1	0.0096	33
5.2	0.0096	34
5.3	4.910	35
5.4	4.950	35

From Table 1, we see that the CSU output is a logic low when the input current through the shunt is lower than 5.3 A. For input current higher than 5.3 A, we see a logic high. Therefore, our experimentally obtained HTCS threshold is ~5.3 A, which gives a 6 % difference from the theoretical 5 A. Hence, we are within the required 10% tolerance. We also see that the temperature of the shunt is well below the 170 ℃ as required. Figure 9 shows the HTCS board. For the LTCS board, we damaged the LMP8640 while soldering, hence, we ordered the parts when we realized this. However, the part did not arrive in time for us to solder, test, and verify. Nevertheless, the only difference between the HTCS and LTCS is the current sensing shunt. Given that both have the same functionality, and the HTCS works as expected means that our design is verified. Therefore, we can claim that the CSU works as expected.

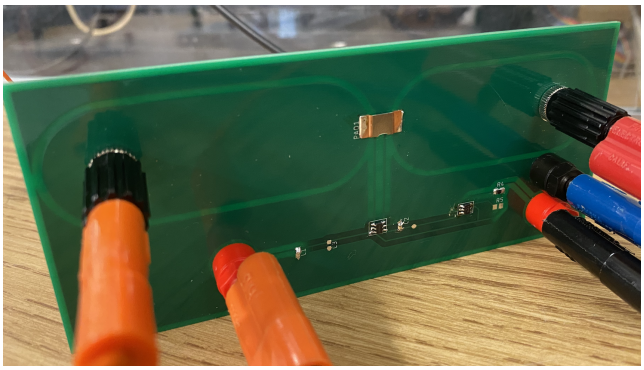

Figure 9: HTCS PCB board

3.2 Control Logic Verification

The main requirements for the control logic are as follows:

1. Proper operation of Converter_State based on inputs from the current sensors
2. Proper operation of Power_Up based on inputs from the current sensors
3. The PWM controller outputs a 90-110 kHz waveform with a maximum of 39 % duty cycle only when Converter_State is high

3.2.1 FSM Verification

Table 2 illustrates the results we measured during the testing phase for the FMS of the control logic subsystem. The inputs of the controls, SENSEhp and SENSElc, were simulated using pull up switches and all components used were powered using the 5 V power supply. The entire power up and power down cycle was used to verify the outputs of the FSM, Converter State and Power Up simulated by the values of SENSEhp and SENSElc. The results in Table 2 show full functionality of the FSM. This test was repeated and all results remained identical.

Table 2: FSM Functionality

Inputs (V)		Measured Outputs (V)	
SENSEhp	SENSElc	Converter State	Power Up
0.160	0.160	0.240	5.2
5.2	0.160	5.14	0.210
0.160	0.160	5.2	0.210
0.160	5.2	5.13	5.17
0.160	0.160	0.210	5.2

3.2.1 PWM Generator Verification

The PWM Generator was then tested with the FSM and powered using 5 V power supply. Figure 10 shows the oscilloscope screen capture of our results for the testing phase for the PWM Generator. When Converter_State is low the PWM Generator output is ground, as presented in Figure 10(a). However, when Converter_State is high the output is a 108 kHz PWM wave with a

maximum duty cycle of 39.07 % and a peak to peak of 5 V, as presented in Figure 10(b). This in conjunction with the previous test verifies the full functionality of the control logic board.

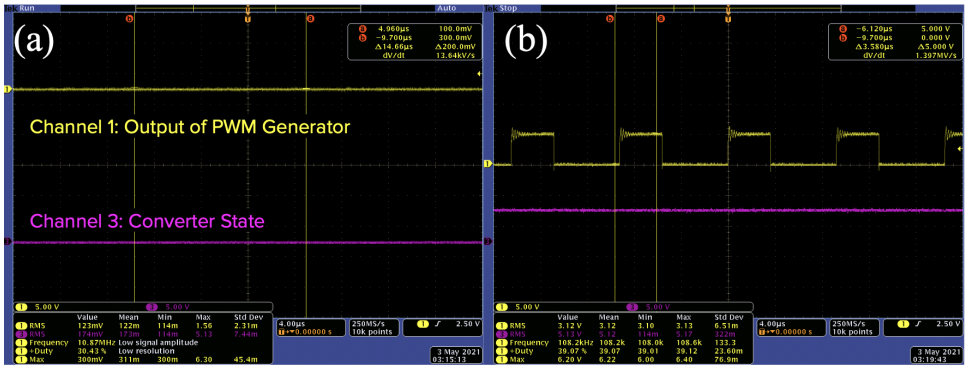

Figure 10: PWM Generator Outputs when (a) Converter State is Low (b) Converter State is high

3.3 Power Converter Verification

The main requirements for the power converter are as follows:

1. Transformer Turn Ratio is approximately 2 : 1 (1.9-2.1 : 1)
2. Output RMS voltage of the power converter should remain within 10 % of the desired 13.8 V at a 1 A current draw.
3. Output RMS voltage of the power converter should remain within 10 % of the desired 13.8 V at a 5 A current draw.
4. The power efficiency of the converter is above 85 % at 2 A and above 90 % 5 A.

3.3.1 Transformer Verification

Figure 11 shows the transformer we wound for use in the converter. We tested using a ferrite core area of140 mm^2, with a maximum B_{sat} value of 240 mT.

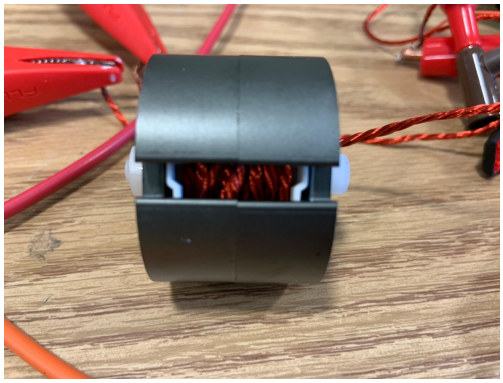

Figure 11 : Physical Construction of the Transformer

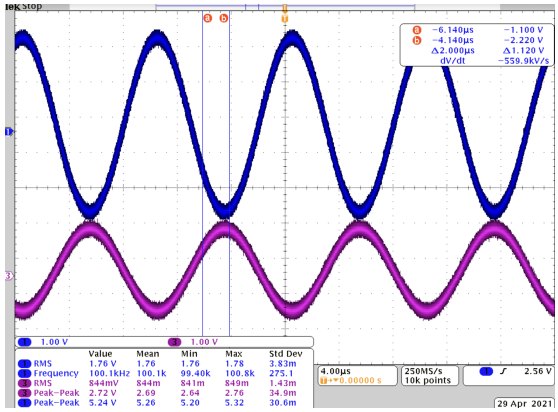

Figure 12: Transformer output, bottom waveform, when waveform generator is used for input, top waveform

To test the transformer, initially, we used the function generator probed across the primary side, connected a resistive load across the secondary and measured the waveform across the load using an oscilloscope. The input to the primary side was a 5.24 V peak-peak sine wave with an offset of 2.62 V with a frequency of 100 kHz from the function generator. Figure 12 shows the input. We see that the output waveform is sine wave which has a peak-peak voltage of 2.72 V and a frequency ~100 kHz. Therefore, the turns ratio we achieved was 1.93 : 1, which is within the tolerance set.

3.3.2 Power Converter Output Verification

Figure 13 shows the primary and secondary side of the converter PCBs soldered and tested.

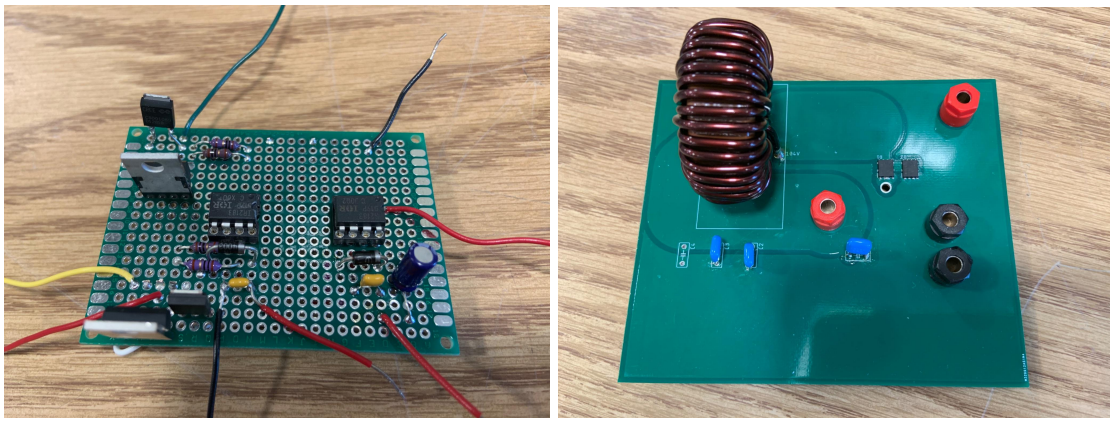

Figure 13: Power Converter primary side (left) and secondary side (right)

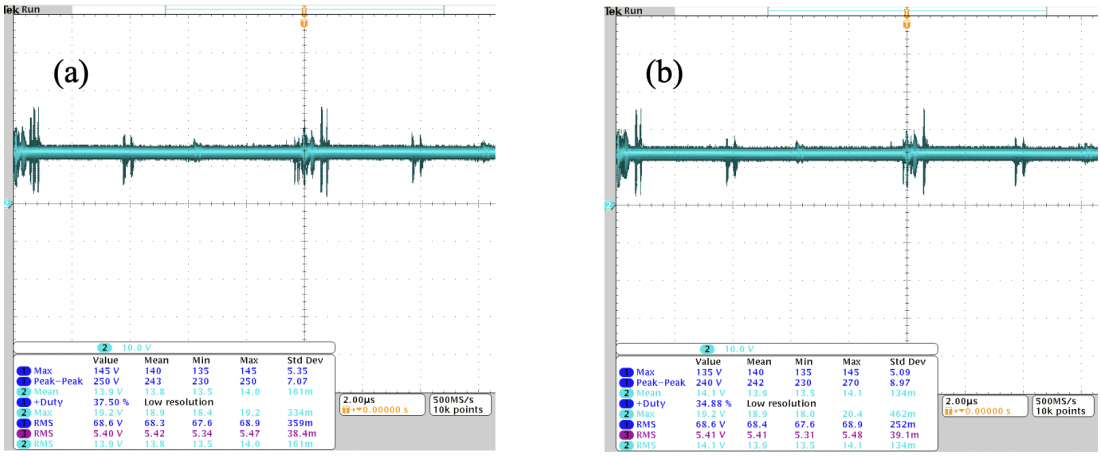

Figure 14: Power Converter Output when output current is (a) 1 A (b) 5 A

For the verification of the converter, we initially connect a waveform generator PWM to the gate drivers for the power switches. After the controls PWM generator was verified, the PWM generator we designed was connected to the power converter module and the output voltage at 80 V input is shown in Figure 14. Figure 14a shows a 13.9 RMS voltage at 1 A current draw by the load, and Figure 14b shows a 14.1 RMS voltage at 5 A of current draw. This is within the ten percent variation of the desired 13.8 V, so this requirement is verified.

3.3.2 Power Converter Efficiency Verification

Efficiency data was collected from current draws ranging from 1 A to 5 A. Figure 15 and Table 3 show the results of converter efficiency. For testing, we used the voltage and current data provided by the 80 V power supply and the 13.8 V power supply to calculate the input power. For the output, we used the electronic load to simulate the auxiliaries and set the maximum current draws from 1 A to 5 A and measured if the output voltage was stable around 13.8 V.

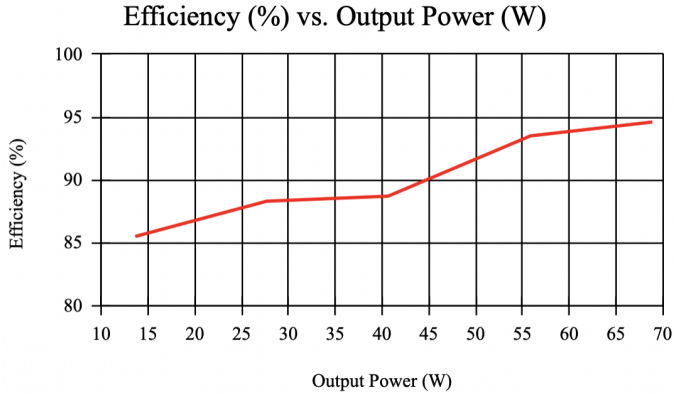

Figure 15: Power Converter Efficiency vs Output Power graph

Table 3: Power converter efficiency at different current draws

Input Voltage (V)	Input Current (mA)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency (%)
79.98	199.6	15.96	13.8	0.99	13.65	~85.5
79.99	391.3	31.32	13.9	1.99	27.66	~88.3
80.03	572.7	45.82	13.6	2.99	40.64	~88.7
79.98	747.2	59.76	14.0	3.99	55.86	~93.5
80.01	916.5	71.31	13.8	4.99	68.85	~94.6

From the data provided above, we see that our results verify the required efficiency as stated in the introduction of Section 3.3.

4 COST AND SCHEDULE

4.1 Cost

Table 4 shows the costs of the components used in the project. Our fixed development costs are estimated to be $53/hour, 8 hours/week for 3 people. We consider 70 % of our final design completion this semester (15 weeks), neglecting the operations using an actual EV. The resulting cost is presented in Equation (7) and the total development cost in Equation (8).

$$3 \cdot \$53/hour \cdot 8\,hours/week \cdot 15\,weeks/\,0.7 = \$27,257 \quad (7)$$

Table 4: Converter System Cost Analysis

Component	**Cost (prototype)**	**Cost (bulk)**
GaN FETs (Texas Instruments, LMG3410R150)	$22.32 (x2)	$14.23
1mΩ resistor (Vishay/Dale, WSBS85181)	$14.59 (x1)	$5.68
Current Sense Amplifier (Texas Instruments, LMP8640)	$2.36 (x2)	$1.04
Window Detector (Texas Instruments, TPS3700)	$1.79 (x3)	$0.79
Transformer (self-winded with litz wire on ferrite core provided by power electronics lab)	$9.00	$6.00
Logic ICs, inductors, and capacitors (digikey, mouser, etc.) Inductors: HHBC24N-2R3A0104V Capacitor: KTD500B106M55A0T00	$12.00 (total)	$0.30
High Voltage Side Power Diode (Wolfspeed CSD01060E)	$0.96 (x2)	$0.75
Low Voltage Side Power Diode (ON MBRB30H60CT)	$1.71 (x2)	$0.85
Low Voltage Side Power Diode (STPS30L30DJF)	1.12 (x4)	
PCB (PCBway, FR4, 3oz, 8 mil min spacing)	$39.60 (x1)	$7.75
Component	$135.26	$37.40

$$TOTAL\,COST = \$27,257 + \$135.26 \times 2 = \$27,527.52 \quad (8)$$

4.2 Schedule

Table 5 shows the schedule we followed.

Table 5: Project Schedule Breakdown

Week	Tony Xu	Sanat Pandey	Marwan Eladl
02/08	Converter topology research	Modular design research	Component Research
02/15	Converter research	CSU design and Footprint layout on Eagle	Current Sensor Unit Design
02/22	High-side converter design	Eagle schematic for CSU	Control Logic Design
03/01	Low-side converter design	CSU PCB layout	Control Logic Design
03/08	Power electronics lab visit and transformer winding design	Power electronics lab visit and transformer winding design	Control Logic PCB Layout
03/15	Finalized power converter PCBs on Eagle	High Voltage side of converter PCB layout completed	Control Logic Re-Design and PCB Layout To Solve Issues
03/22	Transformer design and test	Parts List Finalization and Purchase	Parts List Finalization and Purchase
03/29	High voltage PCB solder and test	Soldered CSU components and low voltage PCB	Soldering of Control Logic Board
04/05	Debugging the high voltage converter board	Tested CSU and designed new high voltage PCB	Testing Control Logic
04/12	Perfboard design of high voltage converter, debugged gate driver circuitry	Test of power converter combined with control logic and current sensor	Debugging PWM Output Driver Issue
04/19	Connected power converter modules with the other boards to debug transformer and gate driver signals. Improving efficiency with change in components and passives.	Connected power converter modules with the other boards to debug transformer and gate driver signals. Improving efficiency with change in components and passives.	Connected power converter modules with the other boards to debug transformer and gate driver signals. Improving efficiency with change in components and passives.
04/26	Work on Final Paper	Work on Final Paper	Finalizing Demo
05/03	Presentation	Presentation	Presentation

5 CONCLUSION

5.1 Accomplishments

This project addressed and attempted to provide a possible solution to the issue of inefficient DC-DC converter for EV auxiliaries for low power bands (0-1000 W). The modular design is a compact solution which allows the customer more ways of modifications. The DC-DC converter designed showed over 90 % efficiency for power draws above 50 W with the power switches being driven by the PWM of the controls. The converter and controls worked seamlessly as shown in Chapter 3. Moreover, the CSU design was verified by the functionality of the HTCS: a logic high and low was received at the output when required and satisfied the nominal voltage requirements of the controls. Even though there were certain components such as the GaN chip which had an unforeseen issue, and the transformer output which had ringing common in an experimental setting, a 13.8 V voltage was maintained at the output without a compromise in efficiency. Therefore, the project is considered a success as the concept of having modular DC-DC converters proved to have high efficiency at low power bands.

5.2 Uncertainties

One uncertainty of our project is that we do not know exactly how the circuit will behave at 400 V, and what the efficiency plot at 400 V input will look like. Although we designed our circuit to be able to handle 400 V, we do not have equipment such as a 400 V DC power supply to test the design. However, there are some methods to predict what kind of efficiency values we might be able to see at 400 V. One main area that would cause a decrease in efficiency is the switching transistors. Switching losses are a major cause for inefficiencies in DC-DC power converters and arise when the transistor is turning on or off [16]. Equation 9 describes what causes switching losses in the transistor.

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot f_{sw} \cdot \frac{Q_{GD}+Q_{GS2}}{I_G} \quad (9)$$

P_{SW} describes the power lost due to switching, V_{IN} is the voltage across the drain and source of the transistor, f_{sw} is the switching frequency, Q_{GS} and Q_{GD} depend on the times that the transistor takes to turn on or off, and I_G is the current through the gate of the transistor. Because the voltage

across the drain and source of the transistors would be significantly higher at 400 V, the losses from switching would be proportional to the increase in input voltage.

Another issue with the power converter was that our transformer waveform contains some distortion. Although the waveform still had the correct duty cycle and peak-peak voltage, the waveform can be improved to avoid component failure after extended use. Figure 7 (b) shows that there are ringing effects at the edges of the waveform, and a non-flat peak voltage. Prof. Arijit Banerjee suggested that the ringing is likely caused by the non ideal switching from the transistors, and the non-flat peak of the transformer waveform could be caused by the turn on and off time of the diodes. This waveform can be improved if we used MOSFET switches instead of an IGBT. Placing all the components tightly together on a single PCB would also help negate the parasitic effects and ringing present on the transformer waveform.

5.3 Future Work

The use of microcontroller, which allows for redundancy and customization for both customer and engineer, instead of custom controls is suggested. For the primary side of the converter, an isolated gate driver and separate power switches are recommended to avoid the issues faced while using the GaN chip with the integrated gate driver. An IC or a separate can be used for the CSU, which uses two separate chips on a PCB, for a more compact design. This would allow for the initially aimed single PCB for a single converter module as illustrated in Figure 21 in Appendix G. This design is more practical and compact for usage in an actual EV.

5.4 Ethical Considerations

The first rule in the IEEE Code of Ethics #1 is: to hold paramount the safety, health, and welfare of the public[11]. That being said, there are safety hazards for our project while in use. If the converter stops operating, essential auxiliary systems like the headlights and power steering could fail which can lead to the loss of vehicle control. The design ensures safety measures are in place by using components that are designed for automobile and high power applications, as verified by the datasheet. More protective measures include galvanic isolation that prevents a direct path of current from the high voltage power source to the 13.8V that the user will be using in the auxiliary unit. Furthermore, there is a FAULT signal planned to be incorporated into the

controls. This is for the case of converter failure in an on-road EV, another additional converter will be turned on to ensure auxiliaries are powered.

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APPENDIX A: Requirement and Verification Tables

Table 6: CSU RV Table

Requirements	Verification	Status
1. The current sensing shunt maintains a temperature below 170°C , when the current through it is up to 5 A, to ensure there is no change in its resistance value. A change in the resistance value would alter the current through the sensors leading to faulty operations which needs to be prevented.	1A. Attach a high current power supply set to 13.8 V across the current sensing shunt in series with a variable load (simulating the auxiliary load). 1B. Adjust the electronic load to adjust the current through the current sensing shunt. 1C. Using an infrared thermometer measure and note down the temperature at different current levels between 1 A and 5.5 A.	Verified
2. The output of the sense amp should be 400mV (window detector threshold) when the current through the current sensing resistor is within a 10% tolerance of threshold of each current sensor (dependent on the type of current sensor and which converter module it is on as discussed in the introduction to section 2.2).	2A. Attach a high current power supply set to 13.8 V across the current sensing resistor in series with a variable load (simulating the auxiliary load). 2B. Adjust the variable load to adjust the current through the current sensing shunt so that it is within the tolerance range around the current threshold. 2C. Using a multimeter measure and note down the voltage at the output of sense amplifier when referenced to ground at different current levels.	Verified: The CSU will not operate if this is not achieved. The CSU design is functional. We probed the output and the value on the multimeter was 399 mV.
3. The window voltage detector outputs a high value when the current through the current sensing resistor is above threshold of each current sensor with a 10% error tolerance.	3A. Attach a power supply across the current sensing shunt in series with a variable load (simulating the auxiliary load). 3B. Adjust the variable load to adjust the current through the current sensing shunt. 3C. Using a multimeter measure and note down the voltage at the output of the window voltage detector when referenced to ground at different current levels between 1 A and 5.5 A.	Verified

Table 6 is the RV table for the CSU.

Table 7: Control Logic subsystem RV Table

Requirements	Verification	Status
1. FSM holds the correct Converter_State based on SENSE_HP and SENSE_LP. This is critical to ensure that the correct ENABLE bit is input to the PWM generator to avoid abrupt on and off of the GaN power switches.	1A. Use a power supply set at 5V and mechanical switches to emulate the inputs coming from the control sensors. Additionally power the FSM with the power supply. 1B. Using an oscilloscope probe the Converter_State output of the FSM with reference to ground to view correct switching.	Verified
2. FSM holds correct Power_Up based on SENSE_HP, SENSE_LP, and Converter_State. This is to ensure that the additional converter can power up such that the correct inputs are available for the control logic before and when it decides to turn the converter off. This is critical to avoid erroneous operations.	2A. Use a power supply set at 5V and mechanical switches to emulate the inputs coming from the control sensors. Additionally power the FSM with the power supply. 2B. Using an oscilloscope probe the Power_Up output of the FSM with reference to ground to view correct switching.	Verified
3. The PWM controller outputs a 100 ± 10 kHz waveform with a 39% duty cycle when ENABLE is high.	3A. Use a power supply set at 5V and mechanical switches to emulate the inputs coming from the control sensors. Power the FSM with the power supply. 3B. Set the input values of the FSM such that outputs a logic high output for Conveter_state output which is the ENABLE signal for the PWM controller. 3C. Using an oscilloscope probe the output of the PWM controller with reference to ground to view the waveform of the output.	Verified

Table 7 is the RV table for the control logic subsystem.

Table 8: Power Converter RV Table

Requirements	Verification	Status
1. The transformer should have a step down ratio of 2:1 (1.9-2.1 : 1) at 100kHz.	1A. Wind the transformer with a minimum of 10 turns on the primary side and ensure that the turns ratio is 2:1. 1B. Attach the waveform generator across the primary side of the transformer and input a 5 V peak-peak sine wave input at 100 kHz. 1C. Attach an oscilloscope using differential probes across the secondary side of the transformer and measure the output.	Verified
2. Voltage measured across the secondary side of the transformer which the output voltage of the converter should be 13.8 V.	2A. Power the primary side of the converter using the 80 V power supply and use the waveform generator for the PWM. 2B. Attach a resistive and electronic load, in series, across the output of the converter, and vary load starting at 1 A. 2C. Attach an oscilloscope across the secondary side of the converter and measure the output voltage.	Verified
3. The efficiency of a single converter needs to be above 85 % for current draws at 1 A and above 90 % for current draws at 5 A.	3A. Repeat 2A, 2B, and 2C. 3B. Measure the current draw from the power supplies and measure the voltage and current output of the converter. 3C. Calculate power efficiency by dividing output power over the input power at each load interval.	Verified

Table 8 is the RV table for the power converter subsystem.

APPENDIX B: Control Logic Parts

Table 9: Control Logic Parts Selection and Justification

Part Function	Part Number	Reason
AND	SN74LVC1G08DBRV	Low propagation delay, which allows for the FSM to run at high speed. This will allow the control subsystem to turn on and off converter modules quickly to keep efficiency high [17]
OR	SN74AHC32D	Low propagation delay [15]
NAND	SN74AHC00D	Low propagation delay [18]
D-Flip Flop	SN74AHCT74DR	Low propagation delay. Large noise margins which make the FSM more stable and less prone to errors [19]
Clock Generator	LTC6900IS5	Easy of controlling output clock frequency with a single resistor [20]
PWM Controller	SG2524D	Easy of controlling the output PWM frequency using a single resistor and capacitor. Voltage feedback functionality available through an error amplifier, which allows for the output duty cycle to be adjusted based on feedback voltage. A maximum duty cycle less 50%, which prevents the transformer from reaching its saturation flux and damaging circuit components [21]
Digital Isolator	ISO7710FQD-Q1	High surge voltage protection. Can operate at 100 kHz (PWM signal frequency) [22]

APPENDIX C: Full High Voltage Side Power Converter Schematic

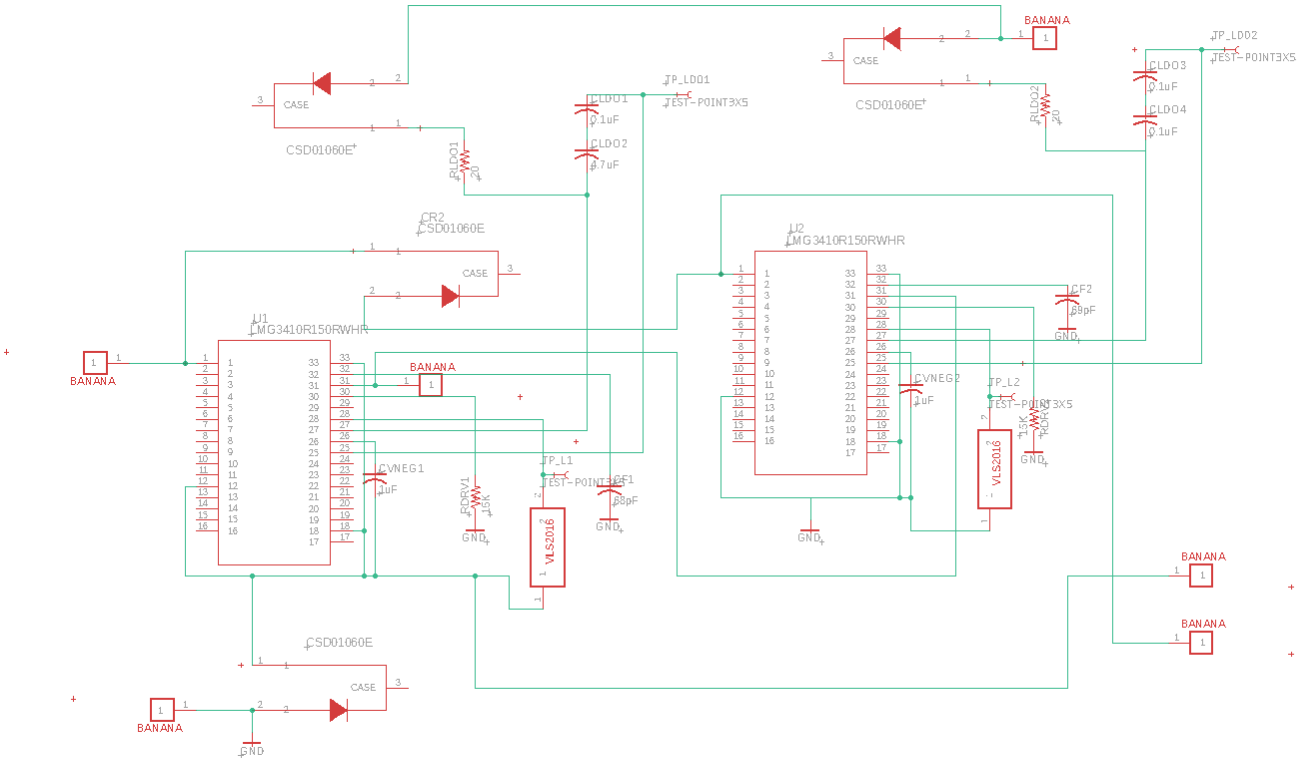


Figure 17: High Voltage Side Power Converter Schematic

APPENDIX D: Derivation for Equation 3 from Professor Arijit Banerjee

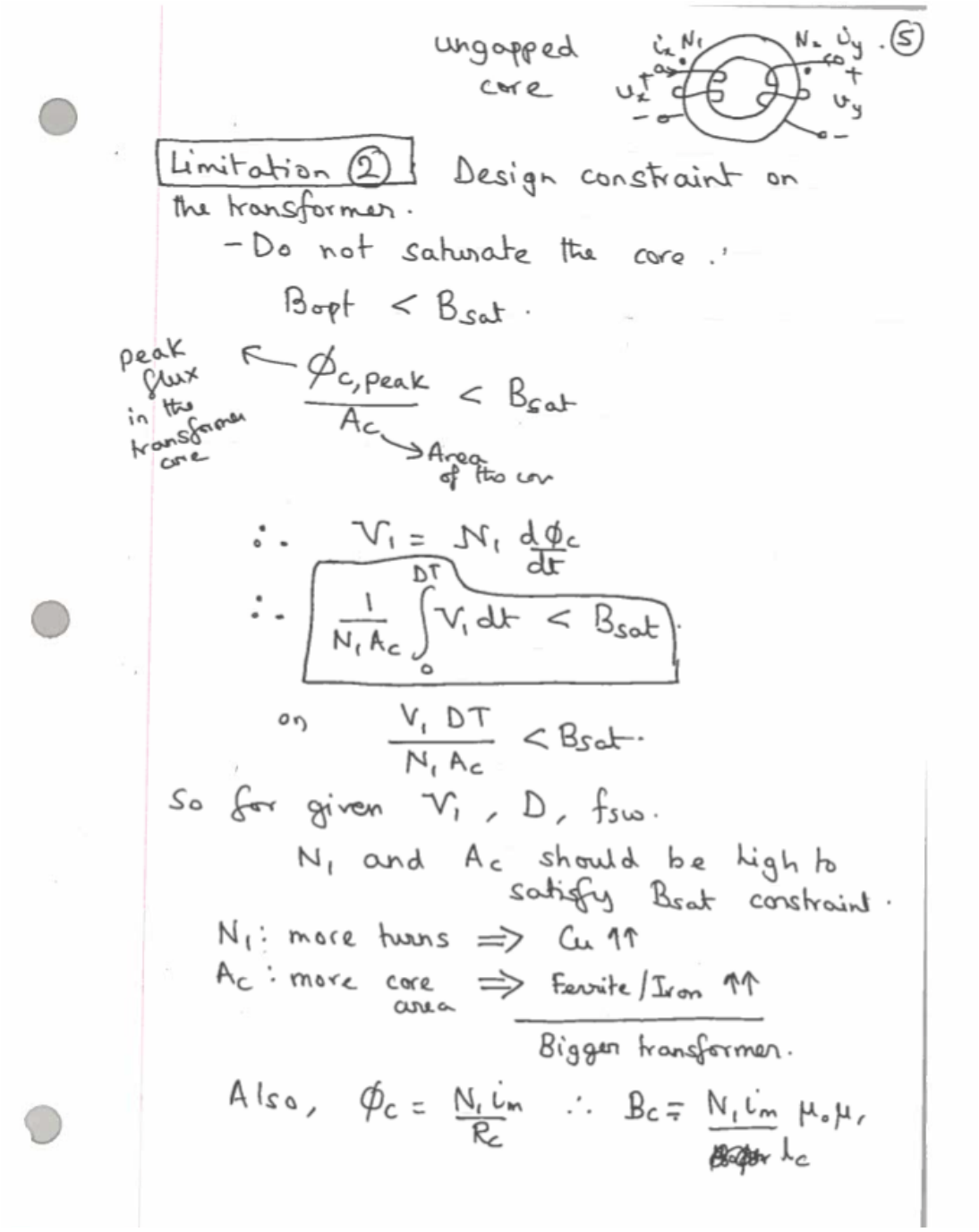


Figure 18: Derivation for Core Saturation of Transformer

APPENDIX E: Derivation for Equation 4

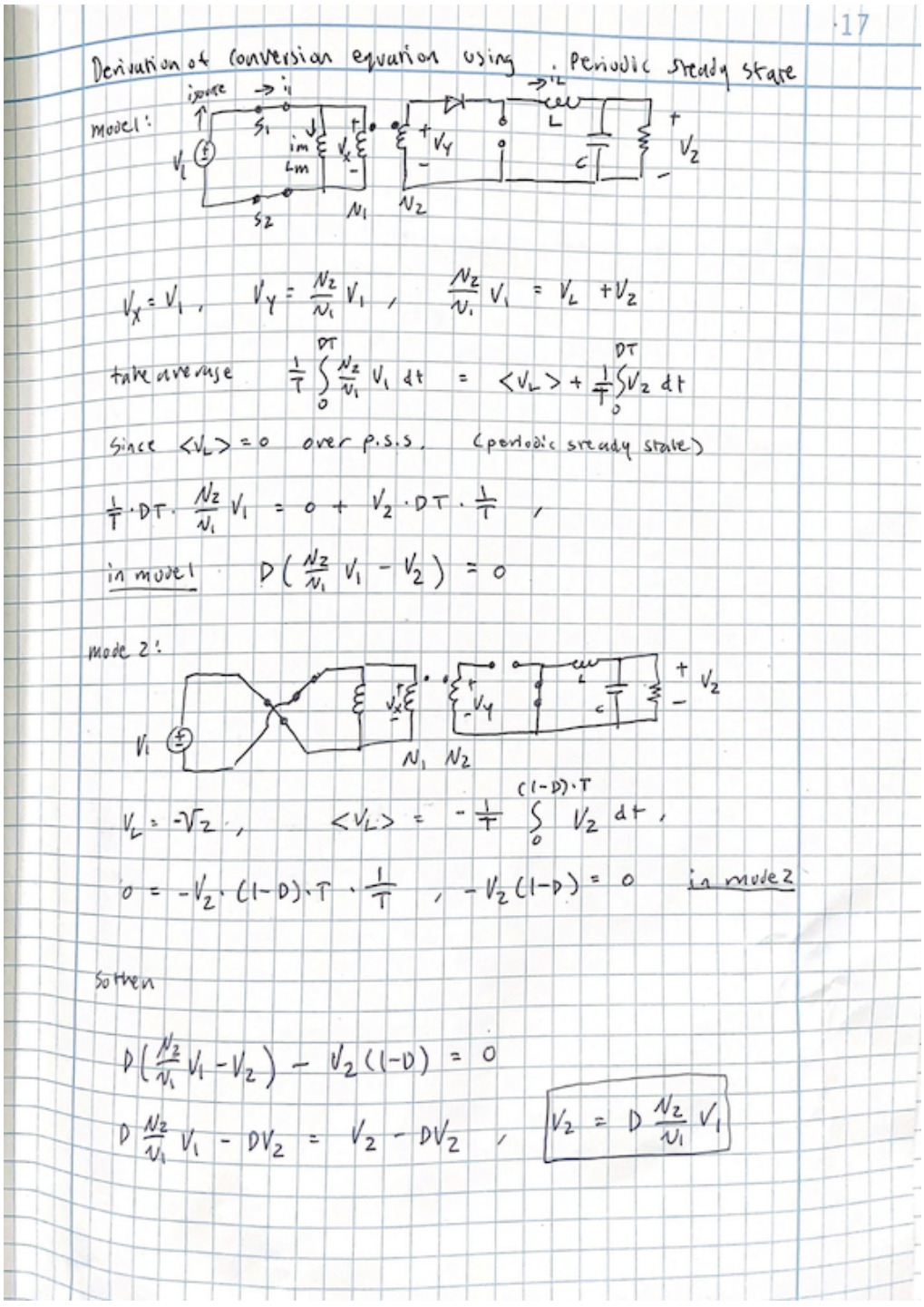
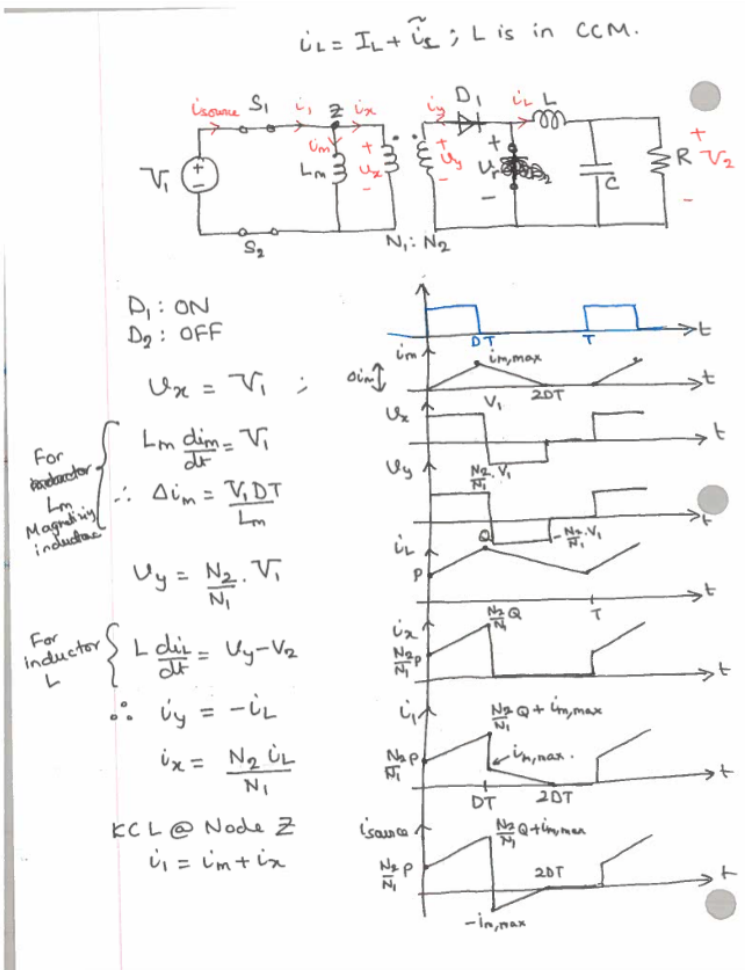


Figure 19: Derivation for Output Voltage Conversion Equation

APPENDIX F: Derivation for Equation 6



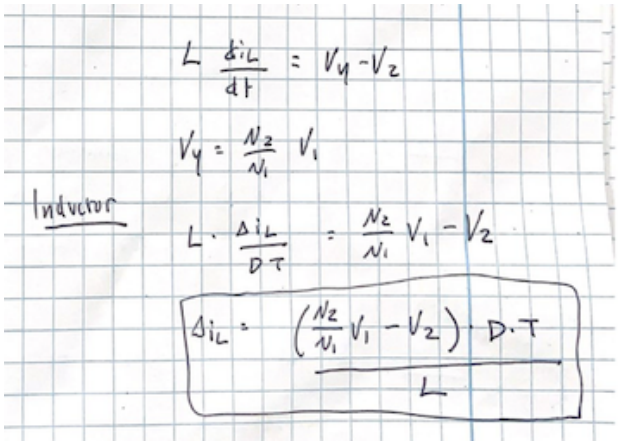


Figure 20: Derivation for Inductor Sizing Equation

APPENDIX G: Aimed Physical Design

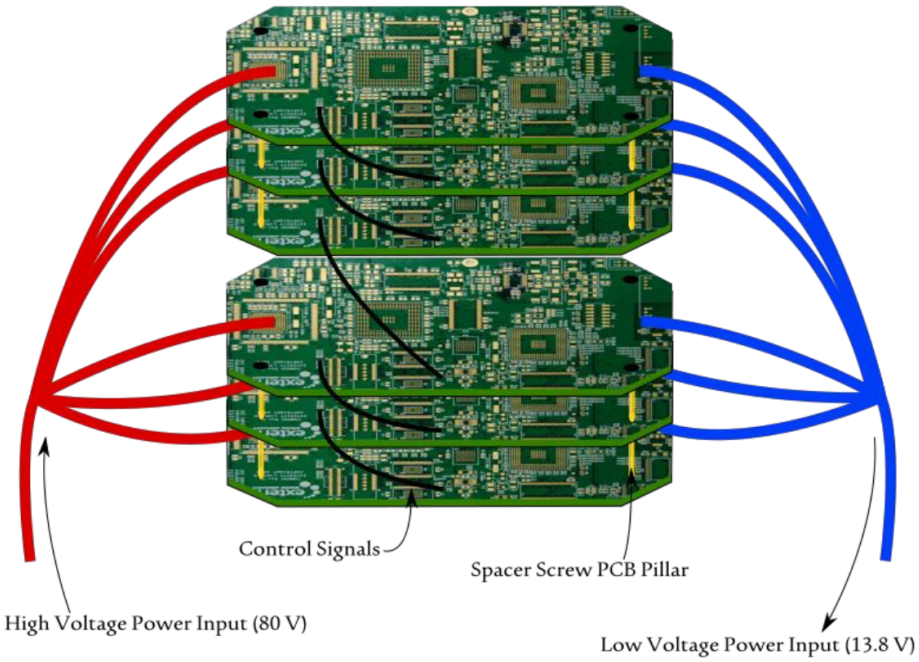


Figure 21: Physical design of single PCB converters stacked for use in EVs