ACTIVE CELL BALANCING FOR SOLAR-VEHICLE BATTERY PACK

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Abstract

This project aims to demonstrate the functionality of a custom active-cell-balancing architecture for future use in a solar-vehicle battery pack. In the absence of a method for balancing cell voltages in a battery pack, the pack capacity is limited to that of the lowest capacity module. By redistributing charge from higher-capacity to lower-capacity battery modules, our design can increase the amount of usable charge in a battery pack. In this report, the design, verification, and results of our project are detailed. Apart from some minor shortcomings, we achieved a fully functional proof-of-concept design. Our design allows for fast balancing with a standard efficiency of charge transfer across any modules in the battery pack. This project was sponsored and developed by members of the Illini Solar Car Team.

Contents

1 Introduction

1.1 Background

Solar-vehicle racing is an engineering-based competition where university teams compete to design, build, and race the best car powered only by the sun. These competitions are 2,000-mile endurance races that take place on public roads and highways over the course of many days. The primary goal is to build a reliable car that can maximize efficiency in order to travel the greatest distance during the event.

In solar vehicles, charge is collected via a solar array and stored in a battery pack. Illini Solar Car (ISC) utilizes a lithium-ion battery pack with 28 series modules of 15 parallel cells each. The nominal voltage of the battery pack is 100.8 V, and the maximum voltage is 117.6 V. In order to ensure safe operation, each battery cell must remain in its safe voltage operating range (2.5-4.2 V). When any single module leaves the safe operating range, the entire pack must stop charging or discharging.

1.2 Motivation

During testing and competition, ISC has observed a voltage imbalance between the 28 modules that make up the battery pack. The battery is considered to be unbalanced when the voltages of parallel sets of cells, called modules, differ in voltage. This occurs because lower-capacity modules will charge and discharge faster than higher-capacity modules. As this occurs, the effective capacity of every module in the pack decreases to that of the weakest module. Once one module reaches 2.5 V, the battery pack can no longer be used even if energy remains in other parts of the pack. In previous competitions, this has rendered as much as 5 % of the total energy in the pack unusable. Figure 1 shows how the imbalance in battery modules during the final portion of ISC's most recent race resulted in shutoff of the car while some cells had a significant amount of charge remaining.

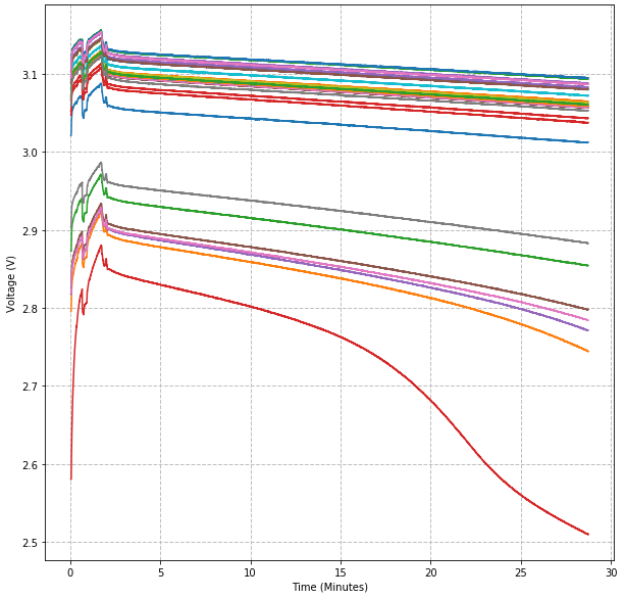

Figure 1: Module voltages during the last 30 minutes of the race. Each color represents a different battery module.

1.3 Objective

To combat any loss in state of charge (SoC) due to module imbalance, we propose the addition of a balancing system to ISC's battery pack design. In order to fully utilize the charge in the battery pack and travel the greatest possible distance, we believe a custom-designed active-balancing system to be the best choice. In a passive-balancing system, charge is dissipated from cells with higher voltages such that they are all discharged to the same voltage. Although it is a less complex design, passive balancing does not increase the amount of usable charge in a battery pack as active balancing does. Figure 2 further demonstrates the advantages of active balancing over passive balancing.

Our active-balancing system redistributes charge from modules with more charge to modules with less charge. This design allows for the full capacity of each module in the pack to be utilized to power the car, rather than charge being left unusable in the pack. Additionally, our custom architecture offers benefits that are not available in off-the-shelf, active-balancing controllers. Our design allows for fast, direct, and bidirectional charge transfer between any modules in the pack. Furthermore, our design is modular and easily scalable to battery packs of different sizes.

As a first revision in a new custom design, we believed that assessing the potential of the design was most important. Therefore, our high-level requirements reflect the goals of having a simple proof-of-concept design that future revisions will expand upon. The proof-of-concept design operates on a battery pack with four modules in series, and each module will have three cells in parallel. We developed the following high-level requirements in order to access the success of our design.

- The active-balancing circuit must be able to redistribute energy from the top module to the bottom module with > 50 % efficiency.
- Over the course of 30 minutes of balancing, modules more than 0.2 V away from the average pack voltage must see their voltage move towards the pack average by at least 0.1 V.
- Individual module voltages must remain between 2.5 V and 4.2 V for the entire duration of a 30-minute balancing test.

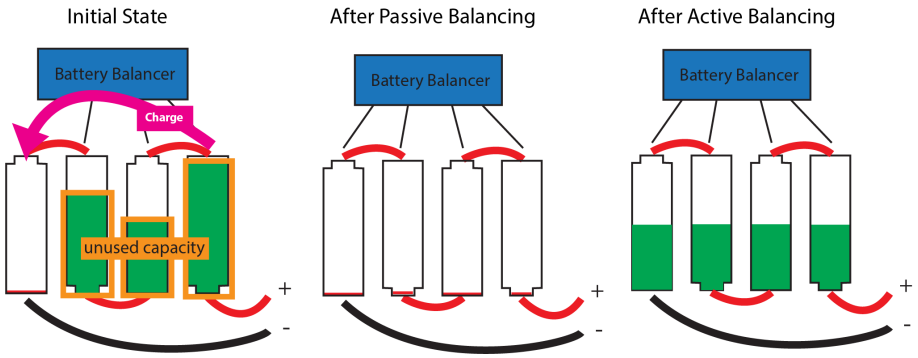

Figure 2: High-level system objective

1.4 Subsystem Overview

The intent of our custom active-balancing architecture is to transfer energy in both directions between the battery modules and a supercapacitor storage element. A balancing control unit uses voltage and current feedback to set the transfer ratio of a series of isolated, bidirectional converters, labelled as balancing units. Each module is paired with one balancing unit. This transfer ratio determines if the corresponding module is charging from or discharging into the shared bus. Thus, individual modules can be charged and discharged to maintain balance in the pack.

The block diagram for this project is difficult to digest without first understanding the high-level organization of the design. Therefore, Figure 3 shows the general energy transfer path and the control loop for each DC/DC converter.

Figure 4 shows the full implementation of our architecture as a block diagram. The main energy transfer objective of the design is identical to Figure 3; however, the control and drive of the converters are explained in more detail. Each balancing unit is made up of an isolated, bidirectional DC/DC converter and an isolated gate driver. These are controlled via pulse width modulation (PWM) signals from the control unit. The feedback loop used to determine the transfer ratios goes through existing voltage sensing hardware on the battery management system (BMS) and is transferred to the control unit on a controller area network (CAN) bus. Feedback on the supercapacitor side for current and voltage is measured as analog voltages by the microcontroller. The microcontroller also enables a precharge resistor between the converter and the supercapacitor to limit the initial inrush current on start-up.

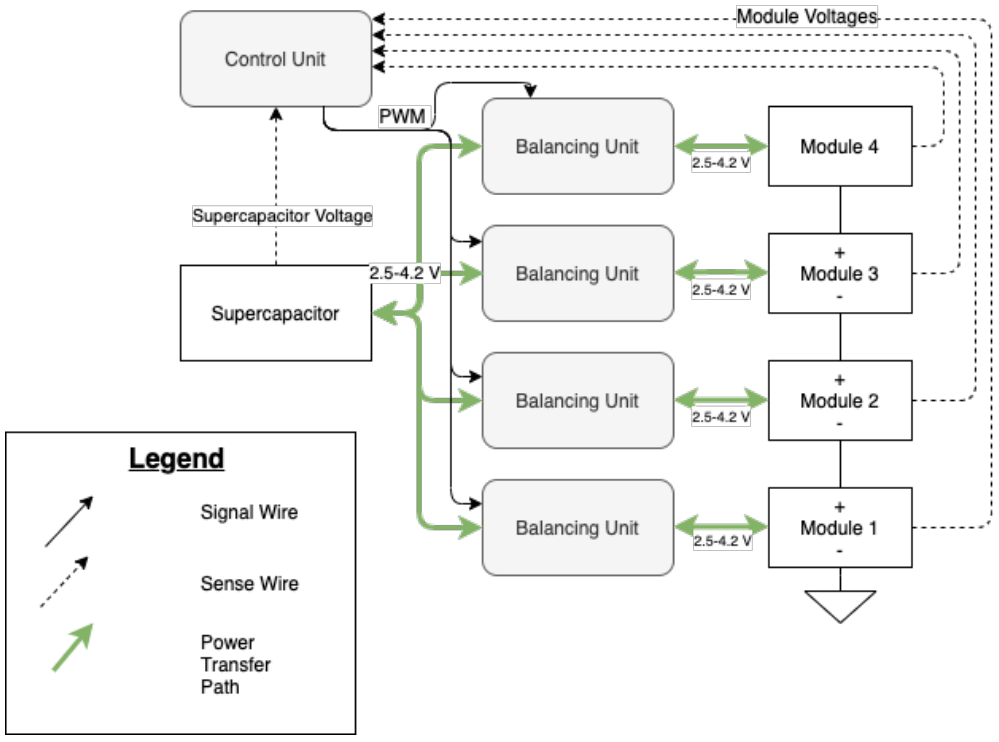

Figure 3: High-level architecture of active-balancing system with energy transfer and control loop

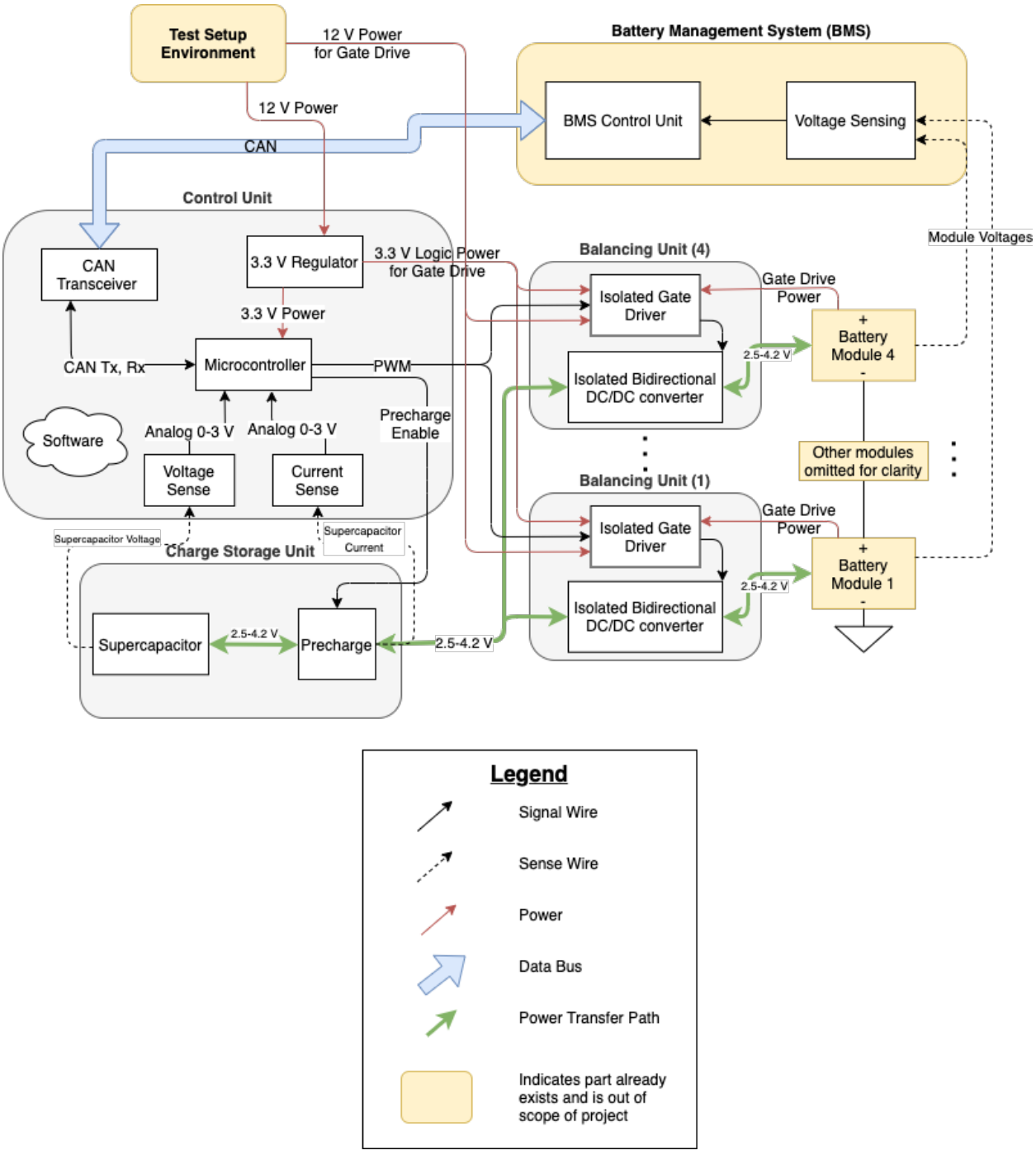

Figure 4: Full block diagram of active-balancing design

2 Design

Our design consists of three main components: the control unit, the balancing units, and the charge storage unit. We also created a small-scale battery pack and utilized ISC's existing BMS to test our design.

2.1 Control Unit

The control unit is responsible for driving each of the isolated DC/DC converters to transfer charge between the battery modules and the supercapacitor bus. The supercapacitor voltage and current are measured directly from the supercapacitor system as analog readings, while the module voltages are received from the BMS via CAN. The balancing control then uses the respective voltages and currents to make decisions about driving each balancing unit using a PWM signal.

2.1.1 3.3 V Regulator

The 3.3 V regulator converts 12 V bus power to 3.3 V. This 3.3 V power is used to supply logic power to the control unit and each of the balancing units. The microcontroller draws on the order of 100 mA during active operation, with a maximum of about 300 mA, and each gate driver draws a maximum of 10 mA from the 3.3 V input. With four gate drivers, and allowing for headroom, we determined that the 3.3 V regulator must be able to supply at least 500 mA. We therefore chose the Recom R-78E3.3-1.0 DC/DC converter. The implementation of this component can be seen in Figure 13 in Appendix B.

2.1.2 Microcontroller

The microcontroller in the control unit receives all auxiliary measured inputs and generates PWM outputs that drive balancing via a control algorithm discussed in Section 2.1.6. Therefore, the microcontroller must include a CAN interface for communication with the BMS, analog inputs for current and voltage measurement, digital outputs for debug LEDs and enable signals, and state configurable timers (SCT) for high-speed PWM control. On ISC, the use of NXP LPC15XX series microcontrollers is standard. We chose to use the NXP LPC1549JBD48 microcontroller for our design. It includes all previously mentioned features. The 48-pin microcontroller has sufficient PWM outputs for a test case, but we would need to use a 100-pin version of the same microcontroller to implement a full pack balancing system. We chose the a 48-pin microcontroller because it was more cost effective and will require only minimal adjustment to scale to a full pack controller [1]. The implementation of this component can be seen in Figure 14 in Appendix B.

2.1.3 Voltage Sense

In order to ensure safe operation and determine the transfer ratio of the converters, we decided to continuously monitor the voltage of the supercapacitor. We have implemented this using a simple resistor divider of two 100 kΩ resistors with 1 % tolerance. This halves the voltage range of the supercapacitor to an analog voltage range that can be read by the microcontroller. The entire supercapacitor circuit is shown in Figure 20 in Appendix B. The node labelled VSupercap Sense is connected to an analog-to-digital converter (ADC) pin on the microcontroller.

When testing this block, we received results that differed from our design expectations that effected our overall accuracy. These findings are discussed in Section 3.1.2.

2.1.4 Current Sense

A measurement that is critical to our balancing control software is the current to and from the supercapacitor to each of the modules. With this measurement, we can monitor the balancing currents and get more accurate readings of the voltage of the modules, independent of the voltage caused by their internal resistances. Our maximum current measurement was initially designed to be 10 A in either direction. Per our requirements, we would like these measurements to be accurate to ± 50 mA.

We have implemented this design by passing the connection from the supercapacitor to each module through a shunt resistor. The voltage across the shunt resistor is then amplified by an op-amp and the amplified output is read as an analog voltage value by the microcontroller's internal ADC. The supercapacitor current sense circuit is shown in Figure 15 in Appendix B. The output of each op-amp, labelled as a Curr[0..3], connects to four ADC pins on the microcontroller.

Equation 1 displays the expected mathematical relationship between the input current, I_{module}, and the output voltage, V_{out}, to be read by the microcontroller. We have chosen Texas Instrument's INA199 for the current sense amplifier which has a gain of 100 V/V and a 1 mΩ shunt resistor. We have also used a 1.5 V voltage reference to allow for bidirectional current measurement [2]. Equation 2 displays the same relationship with the values of the parts chosen. These selections allow for the required accuracy while minimizing losses across the shunt resistor.

$$V_{out} = (I_{module})(R_{shunt})(A_v) + V_{ref} \tag{1}$$

$$V_{out} = (I_{module})(1\ m\Omega)(100\ V/V) + 1.5\ V \tag{2}$$

With our selections, we expected the range of -10 to 10 A to be output as 0.5 to 2.5 V. This is an acceptable range to be read by the microcontroller. However, when testing this block, we received results that differed from our design expectations and reduced the practical range we can measure. These findings are discussed in Section 3.1.3.

2.1.5 Can Transceiver

The CAN transceiver is responsible for converting the differential wire pair from the CAN bus to transmit and receive lines that the microcontroller is able to interpret. The CAN transceiver provides isolation between the board and the CAN bus to protect the CAN bus from noise and voltage spikes. It also converts 5 V logic power to 3.3 V. A fully functional CAN transceiver allows the control unit to send and receive messages from a connected CAN bus. Per standard use on ISC, we have chosen the ISO1042DW isolated CAN transceiver. The implementation is shown in Figure 16 in Appendix B.

2.1.6 Software

Overall, the purpose of the control software is to keep the system in a safe state and to determine the control signals to balance the batteries. We implemented this control software with the control loop shown in Figure 5. This allows external control of balancing by checking if balancing is enabled based on received CAN messages. The software also ensures that balancing is only enabled when safe to do so by regularly checking the battery voltages.

When considering how to best determine the control signals to provide to the converter modules we considered many different options. We considered always providing a 50 % duty cycle, varying the duty cycle based on measured current, and controlling the duty cycle based on the measured voltage. Ultimately, we chose to use a simple open-loop control that decides to charge and discharge modules based on an estimated real voltage. This is advantageous over a simple constant 50 % duty cycle as it allows much faster energy transfer for closely balanced cells. Using the estimated real battery voltage instead of the measured voltage is advantageous as it prevents oscillation between charging and discharging that can occur when the measured voltages are used and the cell voltages are near the average.

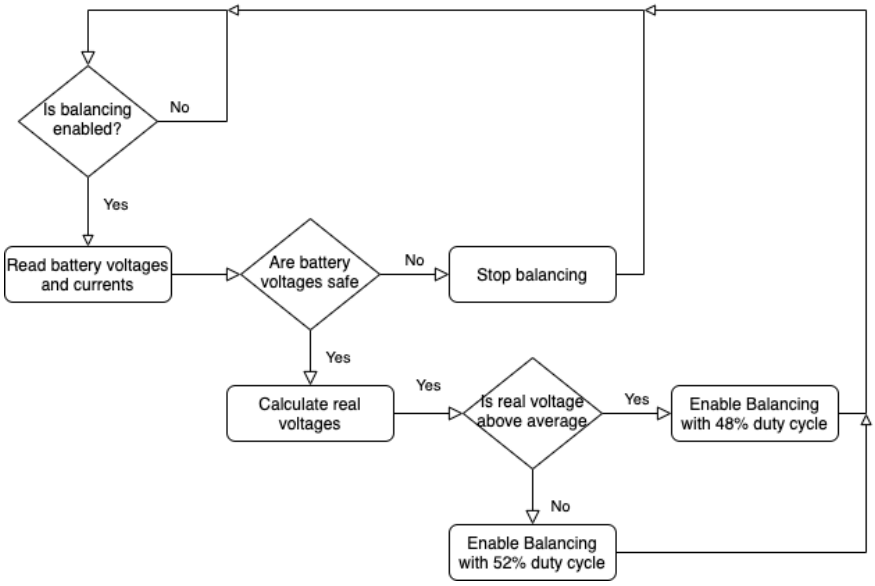

Figure 5: Balancing control algorithm

In order to calculate the real voltages of the batteries, first we characterized the equivalent series resistance (ESR) of the battery modules. This was done by connecting a power resistor to the battery and then calculating the current and measuring the voltage. From this, it was found that the ESR was approximately 0.4 $m\Omega$. With this information, the software can then easily calculate the real battery voltage ε from the measured voltage $V_{measured}$, measured current into the battery i and ESR $r_{internal}$ using Equation (3). The real voltages are then averaged, and the modules above average are discharged, and the ones above this average are charged.

$$\varepsilon = V_{measured} + i * r_{internal} \tag{3}$$

The final step of this control is to generate the PWM signals that will result in the charging and discharging. In order to generate the high frequency PWM signals the state configurable timer (SCT) of the microcontroller has to be configured with a faster clock than the default system clock. To do this a phased-locked loop is used. The SCT is configured with four outputs all with the same frequency and variable duty cycle. The duty cycle is controllable with precision of 0.33 %. Every loop the duty cycle is then set to either 48 % or 52 % to either discharge or charge the module.

2.2 Balancing Unit

The balancing unit is what we have termed the converter block that attaches to each module in the battery pack and connects it to the shared supercapacitor bus. Using control signals from the control unit the balancing unit drives current either charging or discharging the respective module. This subsystem consists of the DC/DC converter block, which follows a flyback topology; and the isolated gate driver block, which uses the control enable and PWM signal to drive the primary and secondary side switches.

2.2.1 Isolated, Bidirectional DC/DC Converter

The isolated DC/DC converter block is the topology that converts each module voltage into the voltage of the supercapacitor on the shared bus and drives current from or to each battery module. The converter is implemented using a flyback topology with a synchronous secondary switch. The NVTFS5C478NL MOSFETs are ideal switches because they have a small package, very low gate charge of 8 nC, and a minimal on state resistance of 11.5 $m\Omega$. In addition, the flyback converter utilizes an RCD snubber circuit as shown in figure 6, which should clamp the voltage on the MOSFET drain in the case of large leakage inductance on the transformer. Equation (4) from [3] shows the determination of the clamping resistor for the snubber circuit.

$$R = \frac{2v_x T_s(v_f + v_x)}{LI_p^2} \tag{4}$$

The switching period, T_s, is 4 µs, the blocking voltage, v_x, is 8.4 V, and the peak primary current, I_p, is 8 A, as determined by simulation. The maximum leak inductance, L, is 0.13 μF. A common peak ringing value is approximately 1.5 times the blocking voltage [3], so I selected a blocking voltage of approximately 15 V, which can be accomplished with a 100 Ω resistor. In the future, an active snubber is an alternate solution that will recover energy stored in the leakage inductance to improve overall efficiency. However, the active snubber requires more control signals, thus increasing complexity beyond what we could accomplish in a semester. The flyback converter we designed is shown in figure 17 in Appendix B.

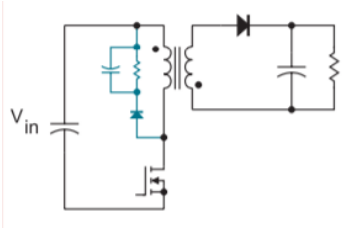

Figure 6: Schematic for an RCD snubber on a flyback converter

2.2.2 Isolated Gate Driver

In order to drive the secondary side switch, we needed to use an isolated gate driver. The SI8274GB1 isolated gate driver IC operates an isolated primary gate drive and an isolated secondary gate drive in complement based on a control PWM and an enable signal. The isolated primary and secondary gate drives each require their own power source. On the supercapacitor side, the gate drive power is the 12 V bus. On the secondary side, a voltage doubler IC, the LM2766, doubles the battery module voltage to create the required voltage for gate drive power. Additionally, a series combination of the connected battery module and the battery module above it in the pack can also be used for secondary gate drive power. The implementation of the

isolated gate drive and voltage doubler are shown in figures 18 and 19 in Appendix B.

2.3 Charge Storage Unit

The charge storage unit consists of two main components: the supercapacitor and the precharge circuit. Each battery module is connected to the shared supercapacitor bus through the balancing units. The charge storage unit temporarily stores charge in the supercapacitor from the modules of higher voltage to be redistributed back to the modules of lower voltage. Instead of a precharge circuit, we considered using the control to slowly ramp up the supercapacitor voltage and limit the inrush current. This is also an acceptable method, that could reduce loss, but transfers complexity and safety responsibility to the firmware. A precharge circuit was included because it simplifies the control firmware and is more stable than a firmware solution.

2.3.1 Supercapacitor

The supercapacitor stores and releases charge to enable the redistribution of charge between any sets of modules. The supercapacitor also regulates the voltage on the shared primary power bus. The supercapacitor voltage can range anywhere from 0 V when completely discharged and 4.2 V, the max voltage of the battery modules. We have chosen to use an AVX supercapacitor, SCMR18F105PRBA0. It's max voltage of 5.5 V and capacitance of 1 F is suitable for our application.

2.3.2 Precharge

On start-up, the supercapacitor can be susceptible to initial current spikes which can damage the system components. A simple hardware solution is to use a precharge circuit. The full circuit implementation of the supercapacitor precharge circuit can be seen in Figure 20 in Appendix B. The node labelled Supercap splits and connects to each of the modules. This circuit increases the resistance between the supercapacitor and the battery modules during precharging to limit the current.

We implemented this functionality by connecting a power resistor of 0.75 Ω between the supercapacitor and the battery modules. This will limit initial current to 5.6 A. Precharge is enabled and disabled by a signal sent via the microcontroller. When the supercapacitor voltage is below 2 V, precharging is enabled. When the supercapacitor voltage is above 2 V, a MOSFET connected in parallel with the power resistor is turned on. This reduces the resistance significantly and disables precharge because the parallel resistance of the power resistor and $R_{ds(on)}$ of the MOSFET is small.

2.4 Battery Modules

The battery modules are important part of the test setup that allow us to verify that the system works with real batteries similar to those found within a solar vehicle. The test battery pack consists of 4 parallel sets of 3 batteries in parallel. 18650 battery cells are used because they are the same cells used in ISC's solar vehicles and are common in many applications.

The mechanical construction of this battery pack is held together by two plastic pieces that sandwich aluminum bus bars that connect the sets of parallel batteries together. These aluminum bus bars have mounting holes which allow for the connection of wires to ever set of parallel cells. Additionally, the modules are held together with spot welding which provides strength and low resistance electrical connections.

3 Design Verification

The design verification section outlines how we determined the partial and full functionality of each system block. At a high level each subsystem was fully functional as were the full system tests. The testing and results for each block are outlined in the subsequent sections. A full list of requirements and detailed verification procedures for each block can be found in Appendix A.

3.1 Control Unit

Apart from some minor shortcomings in regard to the accuracy of the supercapacitor voltage measurement and the range of the current sense circuit, our control unit proved to meet the requirements we laid out in our design. The following sections detail the specific verification tests and results.

3.1.1 Microcontroller

There were four main functionalities that we verified for the microcontroller: CAN communication, analog inputs, digital outputs, and SCTs.

We tested the functionality of the microcontroller's CAN communication directly with the CAN Transceiver block. See Section 3.1.4 for more details; we were able to confirm full functionality. To verify the analog inputs of the microcontroller, we used our voltage sense and current sense blocks directly. The specific data collected during these tests can be seen in Sections 3.1.2 and 3.1.3. The microcontroller produced functional digital outputs which we've used to power debug LEDs and enable and disable precharging. Lastly, we verified the microcontroller's ability to generate PWM signals through its SCTs. The results of programming it to send a 240 kHz PWM signal with a duty cycle of 50 % are shown in Figure 7.

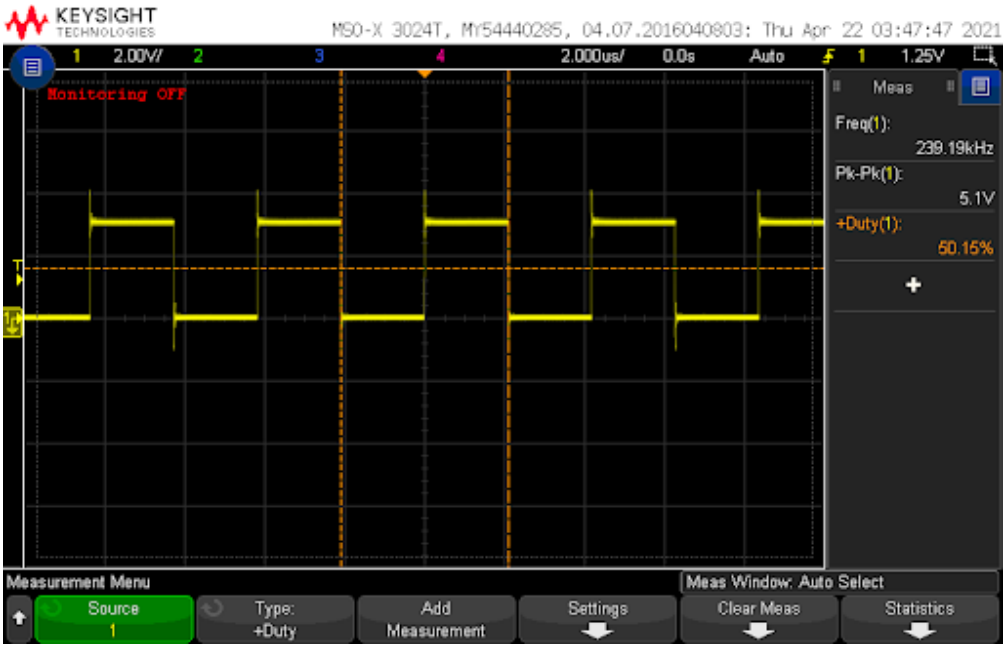

Figure 7: Oscilloscope capture of PWM output

3.1.2 Voltage Sense

The verification of the voltage sense block was a straightforward process of comparing an applied voltage to the measured voltage from the microcontroller. The results are shown in Table 1.

The results of this verification did not meet our requirement of having an accuracy ± 10 mV from 0 to 5 V. We believe that we could improve this accuracy by using lower tolerance resistors in the divider circuit. If this does not improve the accuracy enough, in future designs we could also use an ADC external to the microcontroller to read the analog voltage.

Table 1: Actual and measured supercapacitor voltages

Actual Voltage [V]	Microcontroller Read Voltage [V]
0.000	0.001
1.000	0.982
2.000	1.954
3.000	2.947
4.000	3.933
5.000	4.896

3.1.3 Current Sense

To verify the current sense circuits and the microcontroller readings of these analog voltages, we ran a series of different currents through the shunt resistor and read the voltages from the microcontroller via CAN. We expected to see a gain of 100 V/V through the amplifier as this was specified in the current sense amplifier datasheet; however, we saw a gain that was much closer to 200 V/V. We believe this may have been a result of being sent the incorrect part. Regardless, we collected a series of data points so we could use the multiplier exemplified by the circuit. Figure 8 displays the linear relationship between the actual current and measured voltage of the current sense block for module one. We ran a linear regression to determine the actual slope and intercept and used these values in our software calculations. A similar procedure was run for the remaining three current sensing circuits for battery modules 2, 3, and 4. The results of the calibration can be seen in Table 2. Our requirements specified that the accuracy of each current sensor be within ± 50 mA, which we achieved.

One important note is that due to the larger gain of 200 V/V that we measured, the measurable current range decreased as the microcontroller we used has an analog voltage input range of 0 to 3 V. 10 A of current in either direction through a 1 mΩ shunt resistor would translate to a necessary measurement range of at least 4 V rather than the 2 V we had initially planned for. We did not find this to be a significant issue to the overall system performance because we determined that a current range of -3 A to 3 A was sufficient for the speed of balancing we would like to achieve.

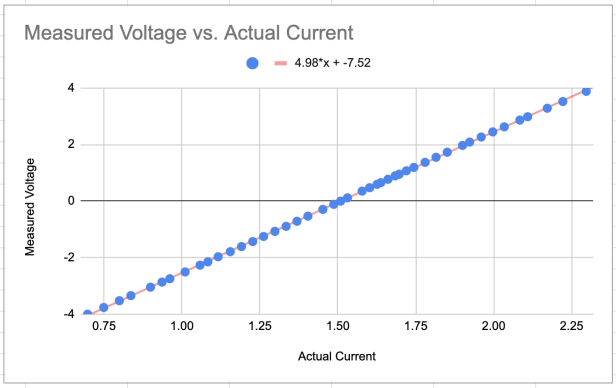

Figure 8: Linear regression of measured voltage versus actual current of current sense circuit for module 1

Table 2: Actual current and measured currents for current sense blocks 1 to 4

Actual Current [A]	Current 1 [A]	Current 2 [A]	Current 3 [A]	Current 4 [A]
3.024	3.022	3.014	3.006	3.026
2.008	1.991	1.986	1.970	1.998
1.052	1.034	1.030	1.024	1.045
0.000	-0.026	-0.004	0.013	0.000
-1.052	-1.070	-1.046	-1.050	-1.040
-2.008	-2.028	-2.002	-2.000	-1.991
-3.024	-3.058	-3.028	-3.020	-3.020

3.1.4 CAN Transceiver

To verify the functionality of the CAN transceiver, we programmed the microcontroller to blink an on-board LED when sending messages and blink another on-board LED when receiving messages. We then set up the microcontroller to send a heartbeat message and receive several status messages from the BMS. After connecting the board to the CAN bus, we verified that both the LEDs were blinking when messages were being sent and received, respectively. Furthermore, we verified that the microcontroller was sending messages by connecting the CAN bus to a computer to view all the messages being sent and received. This block proved to be fully functional.

3.1.5 Software

The precharge software was tested by varying the input supercapcitor voltage and simultaneously measuring the output enable signal. This test was performed multiple times and it was found that every time precharge was disabled above the 2 V threshold.

The disabling of balancing if the battery voltages exit the safe range was tested by supplying out of range voltage signals. For all inputs outside of the range 2.5-4.2 V the balancing enable signals were measured to be off.

To verify the PWM generation, the control board was provided voltage measurements over the CAN bus. The PWM signals were then probed using an oscilloscope. The measured duty cycles matched the desired

48 % and 52 %. Additionally, by varying the voltages provided in the CAN messages, we confirmed that the modules below the average will always be provided a 52 % duty cycle and those above always provided a 48 % duty cycle.

To verify the real voltage estimation, the balancing was switched on and off while observing the battery voltages. Because the real voltage does not change quickly, the initial voltages are considered to be the real voltages to compare the estimations from. After balancing was enabled the estimated values were sent on the CAN bus to the telemetry application where they were recorded. In this testing the estimate values were all within 0.1 V of the real voltages measured with no current flowing. A significant amount of the inaccuracies of the estimation in this test can be attributed to the fact that the original microcontroller's ADC was broken, and an external microcontroller was used to measure the current sense signals with less accuracy. An additional error is introduced because we are only measuring the current on the supercapacitor side of the DC/DC converter and not the module-side current. Overall, however, the accuracy of this estimation was sufficient to perform and demonstrate balancing of the battery cells.

3.2 Balancing Unit

We found the overall functionality of the balancing unit to completely meet our requirements. The following sections detail the specific verification results as well as overall converter performance.

3.2.1 Isolated Gate Driver

To confirm the functionality of the isolated gate driver, we measured the primary and secondary output using an oscilloscope while applying logic and gate drive power. We found that for the entire gate drive voltage range tested (5-12 V) the gate drive circuit produced the expected drive signals on primary and secondary side. An example oscilloscope capture for the gate drive outputs is shown in Figure 9.

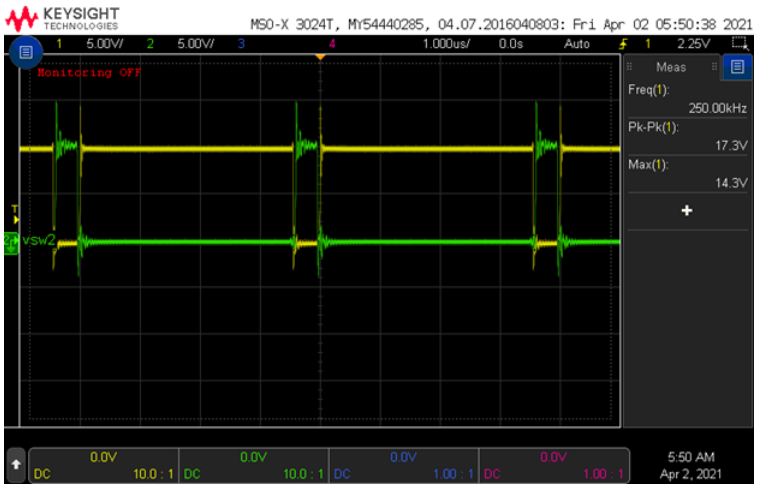

Figure 9: Oscilloscope capture of gate drive outputs

3.2.2 Isolated, Bidirectional DC/DC Converter

The flyback converter needed to operate between 2.5 and 4.2 V on both the input and output for our functionality. We also determined that the converter needed to handle up to 3 A of current in either

direction. To test the range functionality, we tested the extreme conversion ratios at a nominal load. Table 3 evidences the conversion verification results.

Table 3: Input and output voltage based on duty ratio for 7.5 Ω load

V_{IN} $[V]$	V_{OUT} $[V]$	Duty Cycle
2.49	4.19	67 %
2.49	2.46	52 %
4.19	2.52	39 %
4.19	4.32	52 %

We were able to simultaneously confirm the full current operation and characterize the converter efficiency in both directions. The efficiency was tested for a 3.5 to 3.5 V conversion ratio because that is the nominal use case for pack balancing. The characterization results demonstrate both full functionality and high efficiency for the converter module as shown in Figure 10.

The last verification on the flyback converter was to ensure that the peak drain voltage on the secondary side did not exceed the MOSFET rating of 40 V with the inclusion of the snubber circuit. In experimental verification we found almost no drain voltage overshoot when we were expecting about 8 V of additional voltage spike. This is likely because the true leakage inductance of the transformer was much less than the datasheet specification. Figure 11 gives an example scope capture of the drain voltage, which shows almost no overshoot.

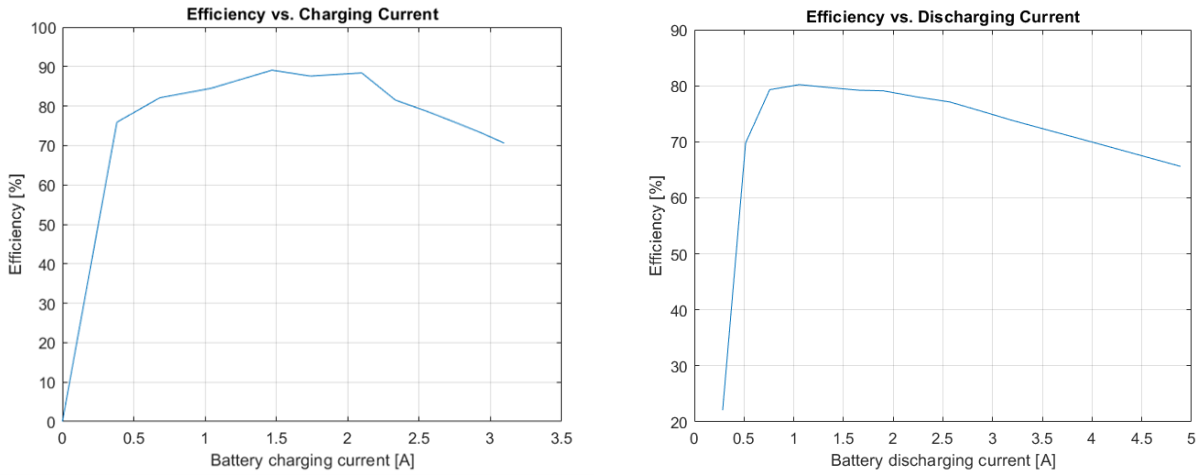

Figure 10: Efficiency characterization for flyback converter

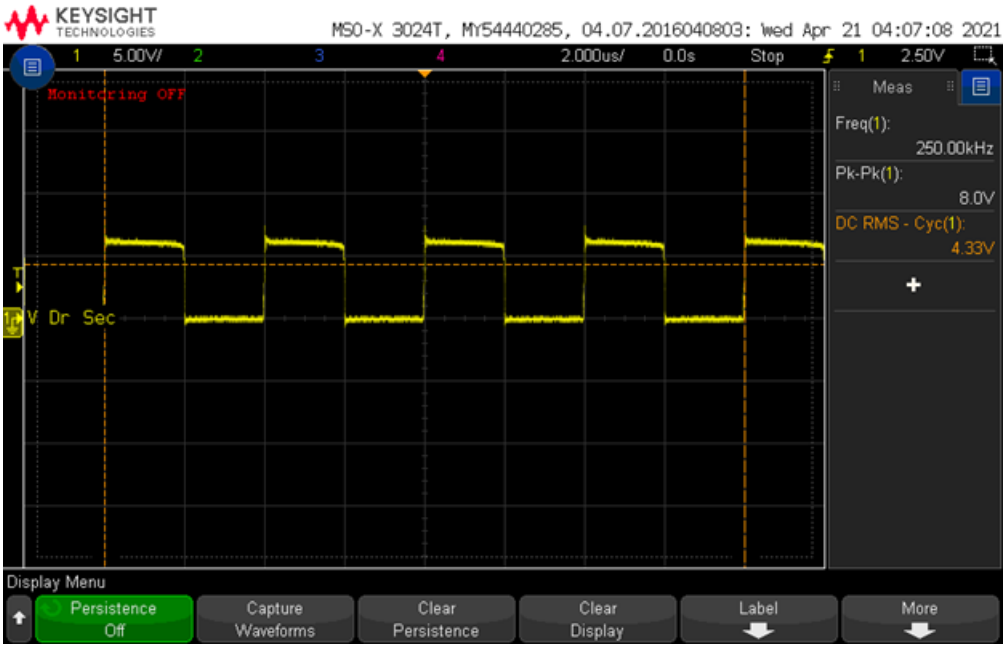

Figure 11: Oscilloscope capture of secondary drain voltage for 3.5 to 3.5 V conversion at 1.5 A load

3.3 Charge Storage Unit

We found the overall functionality of the charge storage unit to completely meet our requirements. The following section details the specific verification tests and results.

3.3.1 Precharge

We verified our precharge circuit by measuring the resistance between the supercapacitor and the modules across the power resistor. The circuit schematic can be seen in Figure 20 for reference. We expected to see a resistance close to 0.75 Ω when precharge was enabled as this is the value of our power resistor. We expected to see a much lower resistance when precharge was disabled as the MOSFET labelled Q4 has a $R_{ds(on)}$ much lower than 0.75 Ω. The results of this test are shown in Table 4.

Table 4: Resistance between supercapacitor and battery modules with precharge enabled and disabled

Resistance [Ω]	Precharge Status
0.824	Enabled
0.132	Disabled

As displayed, the precharge circuit behaved as intended and is therefore fully functional. One note is that the resistance when precharge is disabled is still quite high. In future designs, we will chose a MOSFET with a lower $R_{ds(on)}$ such that this resistance is lowered and we do not incur as many losses across this component.

4 Cost and Schedule

4.1 Cost

This project is only intended for use on Illini Solar Car; therefore, a bulk pricing estimate is not applicable to our use case. Additionally, many components used were donated to the team or already part of the ISC stock, which reduced the actual cost to the project compared to a retail estimate. In total, the labor and parts yield a total cost of $ 67,770.77 for the design and manufacture of this project.

4.1.1 Labor

Our project team consists of two electrical engineers and one computer engineer. Based upon our post-graduation salaries, we estimate the average price of our labor to be $50 per hour. We estimate that this project involved 20 hours of work per person over 9 weeks. A multiplier of 2.5 accounts for overhead costs.

$$(\$50/hr)(20\,hr * 3\,people * 9\,weeks)(2.5) = \$67,500 \tag{5}$$

As shown in Equation 5, the total labor costs for our project sum to $67,500.

4.1.2 Parts

A breakdown of part costs for our project is shown in Table 5. The last column shows the costs incurred towards the project budget when accounting for donations and previous stock.

Table 5: Cost breakdown of required components

Part	**Part Number**	**Qty**	**Retail Cost**	**Actual Cost**
Microcontroller	LPC1549	1	$ 6.67	Donated
3 V Regulator	R-783.3-1.0	1	$ 7.08	Donated
CAN Transceiver	ISO1042DWVR	1	$ 3.94	ISC stock
Supercapacitor	SCMR18F105PRBA0	1	$ 3.38	$ 3.38
Isolated Gate Driver IC	Si8274	4	$ 9.68	$ 9.68
Transformer	PA6605-AL	4	$ 68.60	Donated
Power MOSFET	NVTFS5C478NL	8	$ 5.76	$ 5.76
Lithium-Ion Battery	18650 GA	12	$ 60.00	ISC Stock
Passive Components	n/a	100	$ 10.00	$ 10.00
Connectors	Molex KK series	15	$ 15.00	Donated
Rectifier Diode	SS8P3L-M3/86A	8	$ 5.16	$ 5.16
12 : 3.3 V Converter	R-78E3.3-0.5	1	$ 2.85	Donated
Current Sense Amplifier	INA199B2DCKR	4	$ 2.56	$ 2.56
Filtering Capacitors	n/a	8	$ 40.00	$ 40.00
PCB Manufacture	n/a	1	$ 30.00	Donated
		Total Cost	$ 270.77	$ 76.54

To build all the components of our four-module, active-cell-balancing design, we estimate a cost of $ 270.77 not including donations. If accounting for parts we were to use from previous ISC stock and donations, the

total materials cost is $ 76.54.

4.2 Schedule

Our project schedule is broken down by group member as shown in Table 6.

Table 6: Schedule overview of all project team members broken down by week

Week	**Tara D'Souza**	**John Han**	**Rohan Kamatar**
3/8	Design balancing control schematic	Create high-level design for software to generate PWM signals for balancing control	Design balancing unit schematic
3/15	Design balancing control PCB layout	Spot weld batteries into modules for testing, cycle battery modules	Design balancing unit PCB layout
3/22	Finalize and order PCB components	Program PWM control	Program PWM control
3/29	Conduct basic testing for balancing control PCB, make appropriate revisions	assist with PCB assembly and testing	Conduct basic testing for balancing unit PCB, make appropriate revisions
4/5	Complete second revision of balancing control PCB and send for manufacturing	program balancing algorithm and additional diagnostics	complete second revision of balancing unit PCB and send for manufacturing
4/12	Perform complete assembly and hardware testing of balancing control PCB	perform full system testing with software	perform complete assembly and hardware testing of balancing unit PCB
4/19	Conduct full system testing	Conduct full system testing	Conduct full system testing
4/26	Final Demonstration	Final Demonstration	Final Demonstration
5/3	Final Paper and Final Presentation	Final Paper and Final Presentation	Final Paper and Final Presentation

5 Conclusion

5.1 Accomplishments

In this project we successfully created a proof-of-concept for a new balancing architecture that could potentially be used on an Illini Solar Car battery pack. Over a 30-minute balancing test, the balancing system was able to bring three modules close to their average voltage by charging modules below the pack average and discharging modules above the pack average. Figure 12 shows the measured currents on each balancing unit in amps and voltages of each module in a units of 0.1 mV for a 30-minute test. This measurement confirms the balancing functionality of the project.

The architecture choice also ensures a standard efficiency between balancing for any two modules. Characterization of the efficiency of the converter shows that the overall balancing efficiency will exceed the 50 % threshold and can reach a peak of more than 70 %. Characterization of efficiency from module to module includes system losses such as the module resistance, and thus was not an accurate measure of the performance of our system.

We were also only able to test three functional balancing units at a time because in the testing process we broke a fourth unit and did not have time to make a replacement; however, three functional units are enough to fully prove the capabilities of the architecture.

Figure 12: Telemetry capture of balancing currents and voltages during a 30 minute balancing test

5.2 Uncertainties

While the system is fully functional, there are still uncertainties that remain to be investigated in future testing and revisions of this project. We did not have time to implement closed-loop current control on the modules, thus we could not implement the fastest balancing possible, and we have yet to see how the entire system behaves under a maximum load. The components on the balancing unit and control board were unit

tested to rated current load, so we do not expect any issues on the whole system.

Another uncertainty that remains in that the project is the behavior of the balancing system for very small balancing currents when the pack is nearly balanced. A potential issue here is that the controller estimate of state of charge could be inaccurate and cause charging of the wrong battery. We plan to rectify this uncertainty with a better state of charge estimation and refinement of our balancing algorithm with more testing.

5.3 Future Work and Alternatives

While our proof-of-concept design proved to be fully functional, there still remains work to be done before our system is suitable for use in ISC's solar vehicles. Our current design only measures currents on the supercapacitor side of the isolated DC/DC converter. In the future, we would add current monitoring on the battery side as well. This would give us better measurements for the calculation of actual battery voltages independent of ESR. This information is useful to ensure that battery currents and voltages are all in safe ranges and allow for improved closed-loop current-based control in our balancing algorithm.

Secondly, there are improvements and adjustments we will have to make before this design is scaled to a large battery pack. We would like to reduce the weight and size of the design. Each balancing unit in our current design weighs 50 g. Since our design requires 28 balancing units, one for each module, this would amount to 1.4 kg added to our battery pack. This, with the addition of the control unit and wiring, would add a significant amount of weight to our car. We would also need to make some revisions to our control unit such that it would be able to monitor 28 currents and generate 28 PWM signals. Our current microcontroller of 48 pins does not have enough I/O for this. We could switch to the larger package of LCP1549 microcontroller that has 100 pins or we could consider using an FPGA instead.

5.4 Ethical Considerations and Safety

This project deals with the significant danger of Lithium-ion batteries. Lithium-ion batteries pose a risk due to their high energy density and instability. In a 5-year period over 25,000 overheating and fire incidents involving lithium ion batteries were reported. However, this risk is only significant when the batteries are damaged or utilized outside of their specified operating conditions [4]. The safe operation of lithium-ion batteries is well defined by the American Solar Challenge regulations [5] under which ISC designs its vehicles. These regulations require active protection of overvoltage, undervoltage, over current and over temperature where active protection means that the system will shut off automatically in any of the above fault conditions. In the design of our project, we have implemented these safety measures and verified their functionality.

While working with these dangers it is also important to minimize danger and risk to the public. The IEEE Code of Ethics states that it is our responsibility "to hold paramount the safety, health, and welfare of the public" [6]. We ensure this through safe storage of our batteries, isolation of high voltage, and clear labeling of enclosures to protect the public from the dangers of our project. Our batteries are stored in a fire cabinet while not in use and are always stored at safe charge levels. Additionally, the battery pack is only operated under supervision of our team members.

Furthermore, the team is versed in the Division of Research Safety guidelines in the case of an accident [7]. This includes always being prepared with proper safety equipment such as fire extinguishers and sand. The risk of thermal runaway of damaged batteries is also be mitigated through discharge in a saltwater solution.

While batteries can be dangerous, with proper procedures and design, these risks can be mitigated allowing us to create a safe and functional system.

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[1] "Lpc15xx," Apr 2015. [Online]. Available: https://www.nxp.com/docs/en/data-sheet/LPC15XX.pdf

[2] "Ina199 26-v, bidirectional, zero-drift, low- or high-side, voltage-output, current-shunt monitor," Feb 2017.

[3] R. Ridley, "Flyback converter snubber design," *Switching Power Magazine*, 2005. [Online]. Available: http://www.ridleyengineering.com/images/phocadownload/12_flyback_snubber_design.pdf

[4] "Preventing fire and/or explosion injury from small and wearable lithium battery powered devices," Jun 2019. [Online]. Available: https://www.osha.gov/sites/default/files/publications/shib011819.pdf

[5] "American solar challenge 2021 regulations release a," Oct 2020. [Online]. Available: https://www.americansolarchallenge.org/ASC/wp-content/uploads/2020/10/ASC2021-Regs-EXTERNAL-RELEASE-A.pdf

[6] "Ieee code of ethics." [Online]. Available: https://www.ieee.org/about/corporate/governance/p7-8.html

[7] "Battery safety," Apr 2020. [Online]. Available: https://drs.illinois.edu/Page/SafetyLibrary/BatterySafety

Appendix A Requirement and Verification Tables

Table 7: Microcontroller Requirement and Verification Table

Requirement	Verification	Results
1. Microcontroller must transmit and receive messages on CAN bus.	1. Program microcontroller to send a CAN message and blink an LED when receiving a CAN message. Connect microcontroller to CAN bus through the CAN transceiver. See that messages are received on the CAN bus and that the LED blinks when messages are sent.	Yes
2. Microcontroller must read analog inputs with accuracy of ± 10 mV from 0 to 3 V.	2. Connect the analog input to a potentiometer and measure the voltage of the potentiometer with a multimeter. Send measurements via CAN. Verify that measured values are accurate to multimeter reading within ± 10 mV.	No, less accuracy was achieved
3. Microcontroller must generate 4 PWM signal with frequency of at least 250 kHz.	3. Write code to generate 4 PWM signals and probe their outputs with a oscilloscope. Verify that the signals have defined minimum frequency.	Yes
4. Microcontroller must generate digital output signals.	4. Write code to blink an LED at 1Hz. Verify visually that LED connected to the output pin blinks. Connect output from microcontroller to oscilloscope to verify blinking is at a frequency of 1Hz.	Yes

Table 8: Voltage Sense Requirement and Verification Table

Requirement	Verification	Results
1. Voltage sense must output an analog voltage between 0 and 3 V that can be read as a voltage value with accuracy of ± 10 mV from 0 to 5 V.	1. Connect a voltage source to the resistor divider circuit. Set the output of the voltage source from 0 to 5 V in 0.25 V increments. Connect the analog output of the resistor divider circuit to a multimeter. Verify that the output of the resistor divider circuit remains between 0 and 3 V and varies linearly with the input.	No, less accuracy was achieved

Table 9: Current Sense Requirement and Verification Table

Requirement	Verification	Results
1. Current sense must output an analog voltage between 0 and 3 V that can be read as a current value in both directions with accuracy of ± 50 mA from -10 A to 10 A.	1. Connect a voltage source across the shunt resistor. Vary current from -10 A to 10 A at 0.5 A increments and measure output voltage signal using multimeter attached between the current sense output pin and ground. Calculate current from voltage measurement using Ohm's Law. Confirm that the measurements are within the specified accuracy.	No, smaller current range was achieved

Table 10: CAN Transceiver Requirement and Verification Table

Requirement	Verification	Results
1. CAN transceiver must relay messages on the CAN bus in a readable format for the microcontroller.	1.1. Program microcontroller to send heartbeat message via CAN once every second. Attach a CAN bus analyzer to the CAN bus and use it to provide CAN power. Read CAN messages in software to determine if heartbeat message is sent from the balancing microcontroller. 1.2. Program microcontroller to blink an LED on the receipt of a certain CAN message. Connect the CAN bus analyzer and supply CAN power. Send designated message using CAN bus analyzer and confirm that an LED blinks on the board.	Yes

Table 11: Software Requirement and Verification Table

Requirement	Verification	Results
1. The software must enable precharging whenever the supercapcitor's voltage is below 2 V.	1. Connect a voltage source to the supercapcitor voltage sense input on the microcontroller. Based on supercapacitor's resistor divider circuit, provide voltage inputs to the microcontroller corresponding to supercapcitor voltages from 0 V to 4.2 V. Measure the precharge enable output with a multimeter and see that it enabled when the supercapcitor voltage is below 2 V.	Yes
2. The software must disable all isolated gate drivers when in safe state.	2. Connect a power supply configured to output 4.3 V in place of one module. Measure with a multimeter that the enable digital output from the microcontroller is disabled. Perform the same procedure for a 2.4 V input.	Yes
3. The software must be able to identify modules above and below pack average and generate PWM signals to drive the redistribution of charge such that the identified modules approach pack average.	3. Provide voltage readings with a voltage source such that one module is above average and one is below average. With an oscilloscope, probe the output signals. Verify that PWM signals are generated for the high and low modules.	Yes

Table 12: Isolated, Bidirectional DC/DC Converter Requirement and Verification Table

Requirement	Verification	Results
1. Converter must be able to sink or source at least 3 A of current on the secondary side.	1.1. Connect a power supply at 3 V to the supercapacitor side of the converter and a 1 Ω power resistor to the module side. Attach a function generator set to a 250 kHz 0-3.3 V PWM wave to the gate drive circuit. Also connect a Yokogawa power meter to measure output voltage and current into the load resistor. 1.2. Ramp up the duty cycle of PWM signal and measure output RMS voltage and current on the load using a Yokogawa power meter. Ensure that RMS output current reaches 3 A on the load and the converter remains functional at this current draw for at least 1 minute.	Yes
2. Converter must have an adjustable input and output range of 2.5-4.2 V.	2.1. With a function generator, create an input supply of 4.2 V. With a multimeter measure the output voltage and adjust the input duty cycle until the output voltage is 2.5 V. 2.2. While changing the PWM duty cycle on the function generator to keep output voltage at 2.5 V, lower the input voltage to 2.5 V. 2.3. Keep the supply voltage constant and adjust duty cycle until the output voltage is 4.2 V. 2.4. Increase the supply voltage to 4.2 V while using the duty cycle to maintain a 4.2 V output.	Yes
3. Converter must be capable of bidirectional power transfer.	3. Turn off the supply move the power supply to the module side of the transformer and the load resistor to the secondary side. Repeat the above verifications with input and output reversed.	Yes

Table 13: Isolated Gate Driver Requirement and Verification Table

Requirement	Verification	Results
1. Gate driver must transfer a logic side PWM to the primary drive pin output and an inverted signal with deadtime to the secondary drive pin output.	1. Supply logic power at 3.3 V and power each gate drive at 3.5 V using a power supply. Apply a PWM input to the logic side and probe the voltage on each gate drive pin using a differential oscilloscope probe. Ensure that the duty cycle for the input and primary-output are the same and that the secondary-side drive is inverted.	Yes

Table 14: Supercapacitor Requirement and Verification Table

Requirement	Verification	Results
1. Precharge circuit must limit inrush current to at most 10 A, beyond which the transformer is likely to saturate.	1.1. Connect a power supply to the input of the precharge circuit and the supercapacitor to the output. Set up current measurement using an oscilloscope on the supercapacitor power supply input leads. Ensure that the supply current limit is at least 10 A. 1.2. Step up the supply voltage to 4.2 V. Confirm that current on input does not exceed 10 A as measured on the oscilloscope.	Yes

Appendix B Circuit Schematics

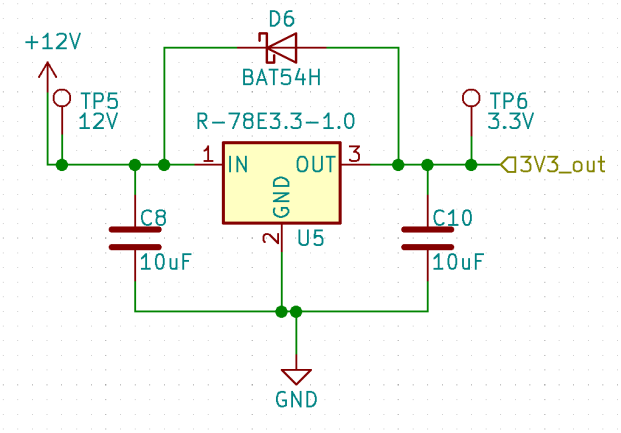

Figure 13: 3.3 V DC-DC converter schematic

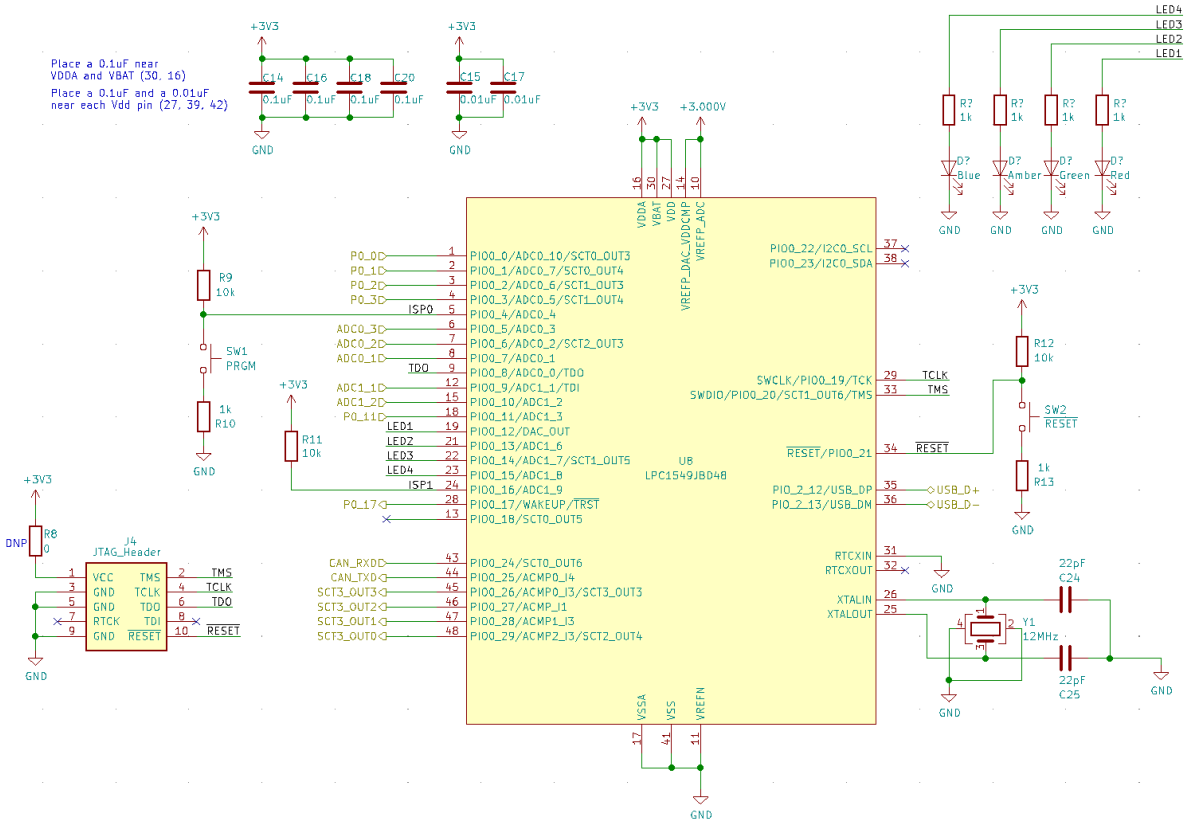

Figure 14: Schematic of microcontroller implementation

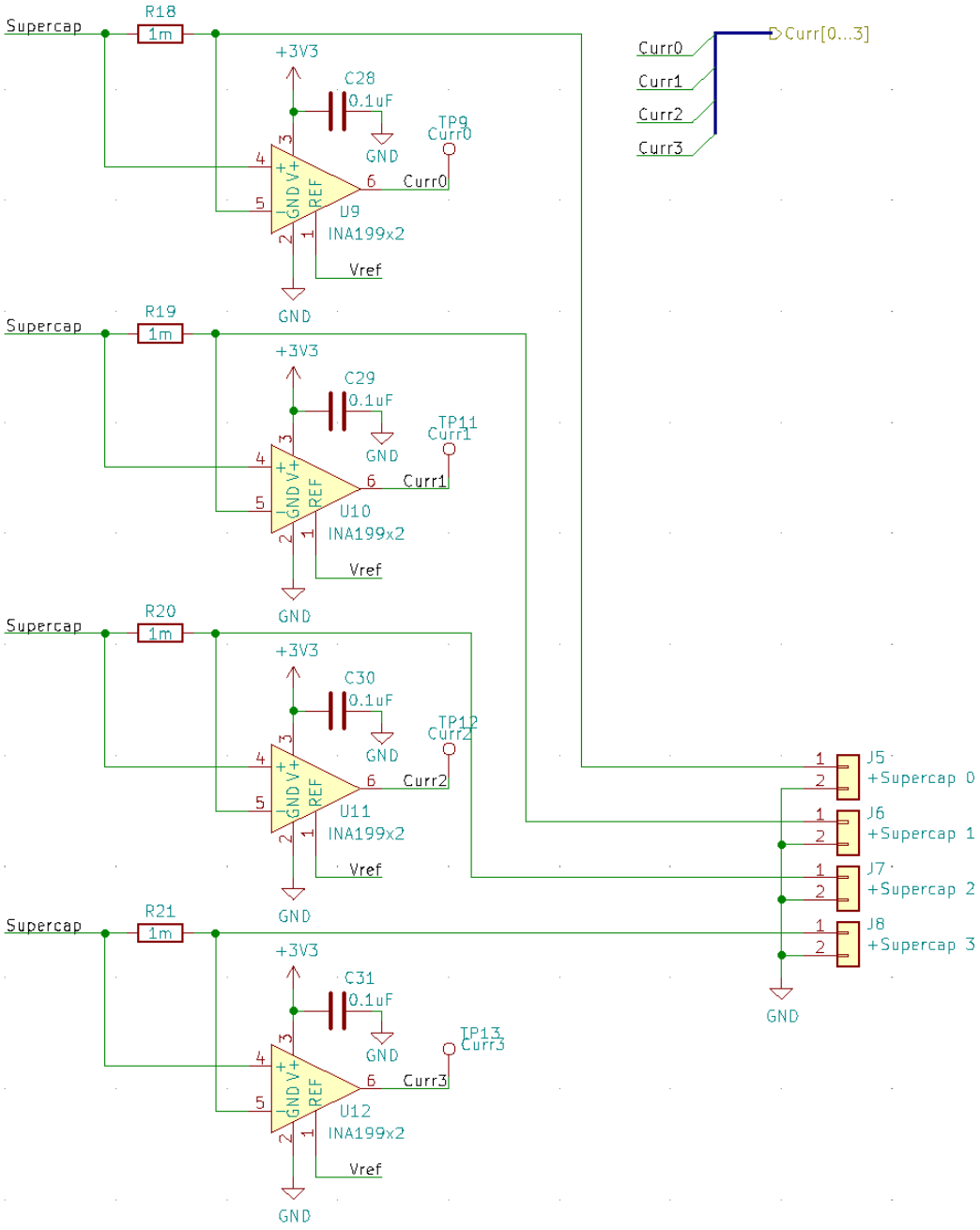

Figure 15: Schematic of current sense circuit

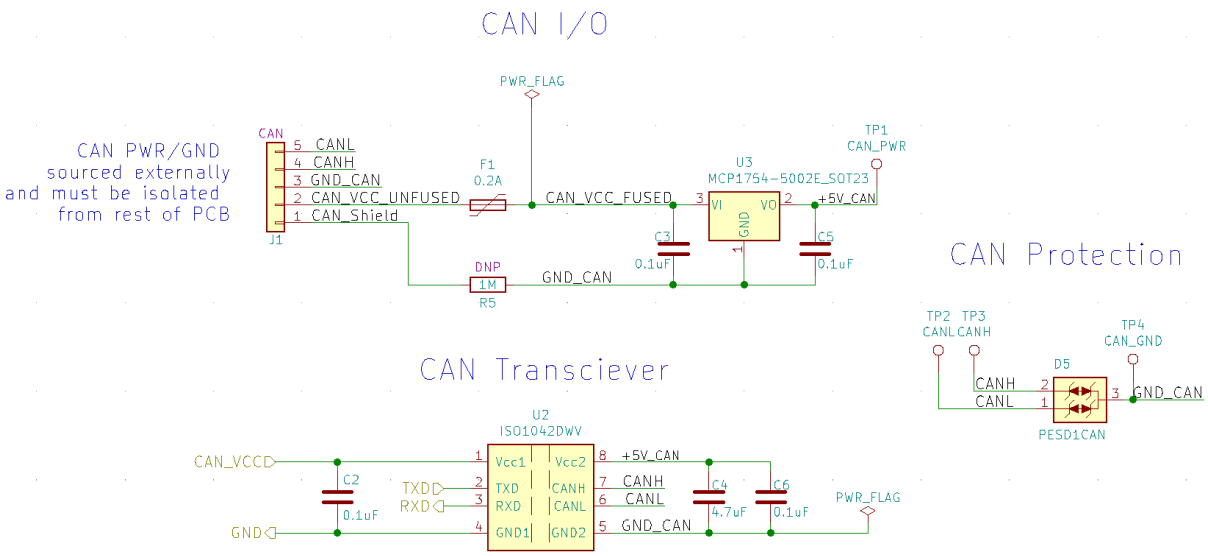

Figure 16: Schematic of CAN transceiver, input and output, and protection

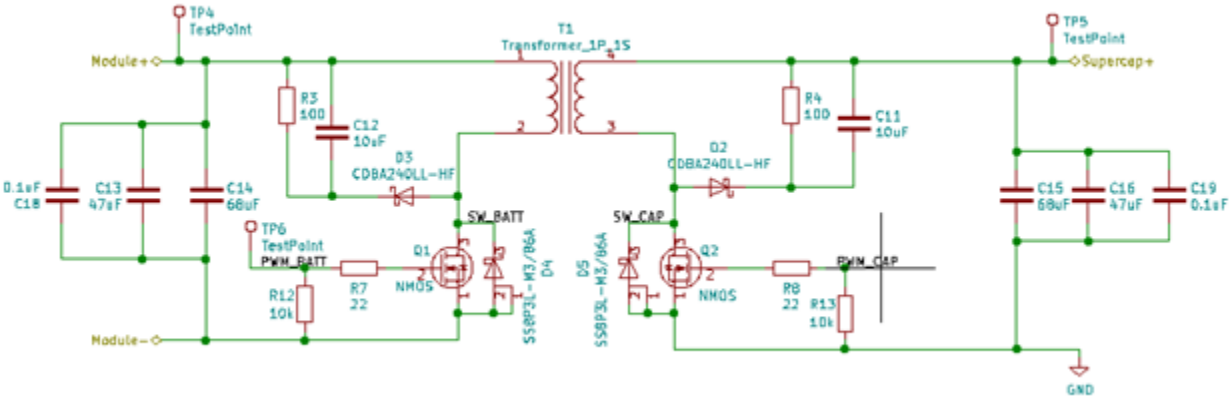

Figure 17: Full schematic of flyback converter

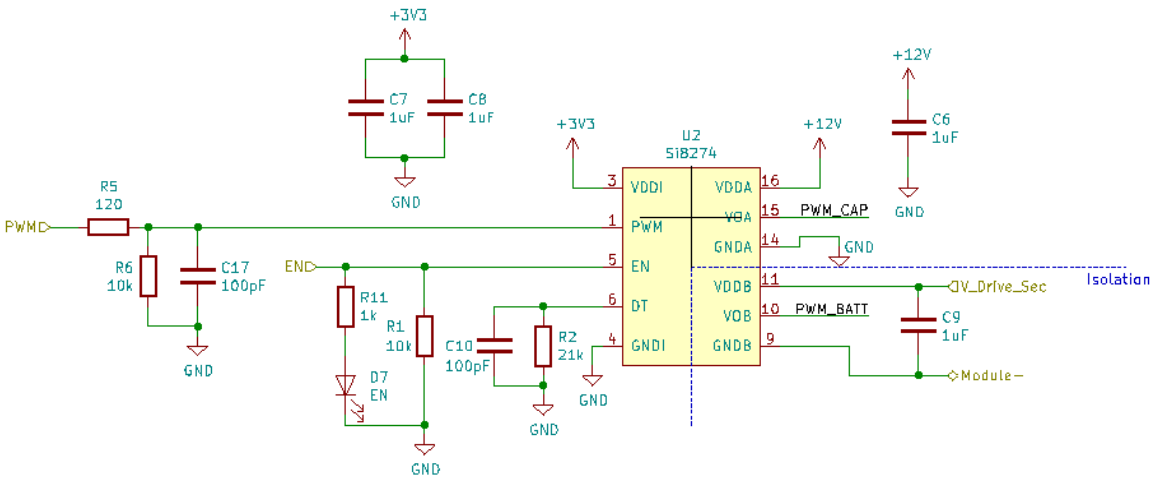

Figure 18: Schematic of gate driver circuit used for flyback converter

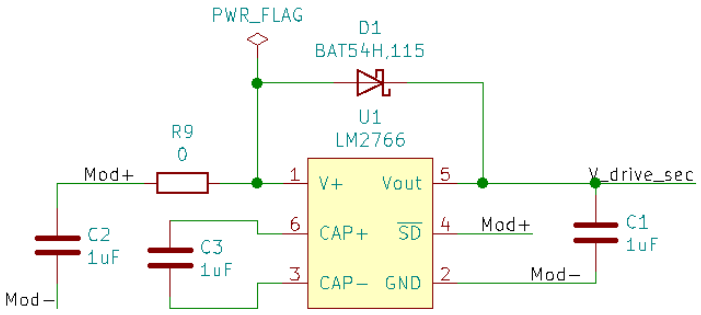

Figure 19: Schematic of voltage doubler circuit for secondary gate drive power

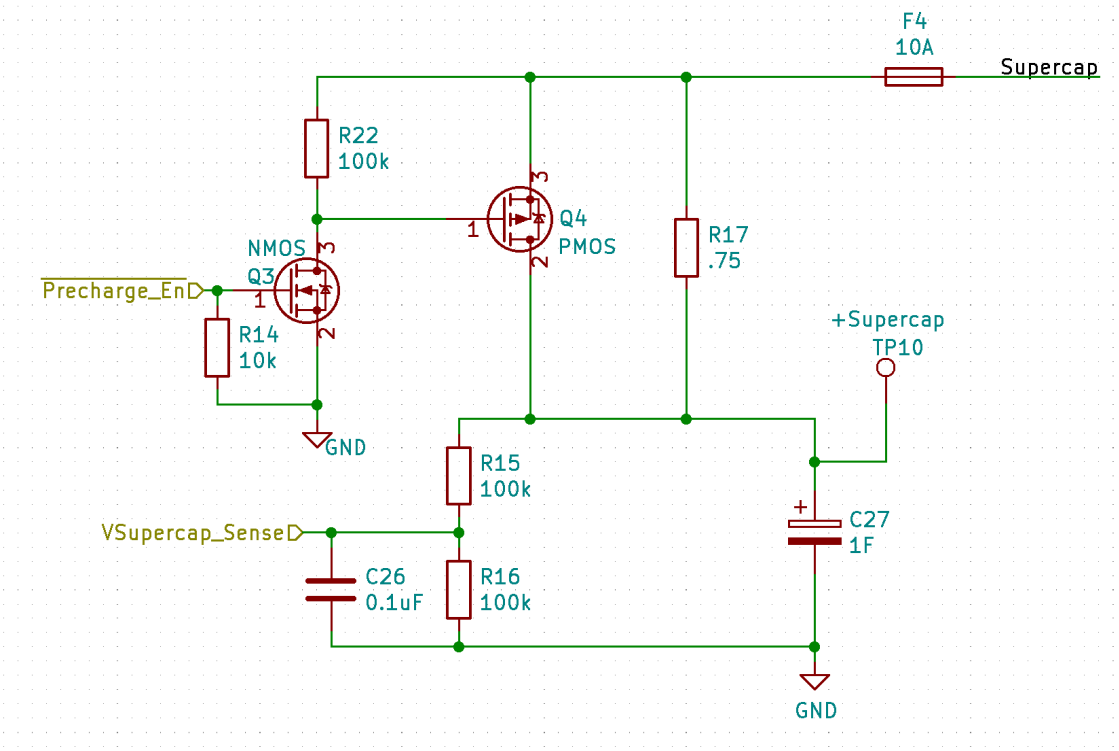

Figure 20: Schematic of precharge, supercapacitor, and voltage sense circuit