

Gallium Nitride Based Modular DC-DC Converter for Electric Vehicle Auxiliary Systems

DESIGN DOCUMENT

Team 54: Tony Xu, Marwan Eladl, Sanat Pandey

ECE 445 - TA: Chaitanya Sindagi - 02/25/2021

1 INTRODUCTION

1.1 Objective

Electric Vehicle (EV) auxiliary systems such as air conditioning and heating systems can reduce the range of the vehicle by up to 35% [10]. Auxiliary systems conventionally get their power from a 12-48V auxiliary battery. Modern electric vehicles have large propulsion batteries, which power the motors of the electric vehicle. As such, many modern electric vehicles manufacturers opt to use the 200-800V power supplied by the propulsion battery to power the auxiliary system. However, the voltage needs to be stepped down such that the low voltage (12-48V) auxiliary systems are not damaged. This requires the use of a DC-DC converter, which changes DC power from an on-board 200-800V propulsion battery into lower 12-48V DC voltages to power auxiliary systems such as headlights, interior lights, wiper and window motors, air conditioning fans, heat pumps for the heater, and many other systems that are required within EVs[2][3]. Most DC-DC converters are rated for high efficiency at high power. This means that they have a sharp drop in efficiency when run at lower power levels[6]. This is illustrated in [1, fig.1].

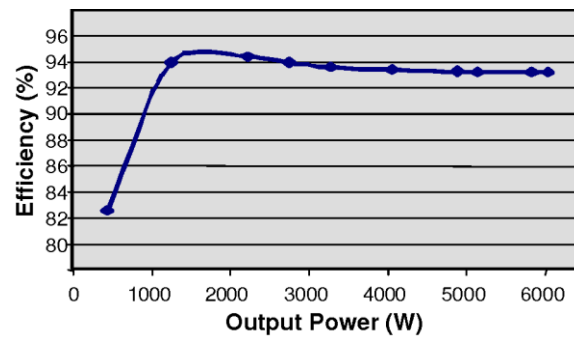


Figure 1: DC-DC Converter Efficiency vs Power Plot [20]

Additionally, [1, fig.1] illustrates how there is a range of power levels at which efficiency is maximized and outside this range the efficiency drops. EVs have different auxiliary system power demands ranging from 60W for headlights and sensors to 1.2 kW for the heater's heat pump [1]. Therefore, the DC-DC converters used have large efficiency drops when low power is being drawn by the auxiliary systems, such as when the air conditioning and heating systems are idle. Additionally, premade DC-DC converters for EVs do not have a wide selection of power ratings [7]. For example, Power Stream only sells 60 A and 100 A rated DC-DC converters for the 13.8V auxiliary systems [7]. This means that if you were to require 70A you would have to buy a 100A rated converter, which would physically be larger than required and would be run at

a lower efficiency when run at 70A [7]. Hence, car manufacturers either use pre-existing high-power converters at lower powers, which is inefficient [6], or they must design their own converters. A modular design would require a single module to be designed for most customers. These modules can then be stacked into a configuration to achieve the power needed depending on the customer's requirement. This would also reduce the expenses for and time required to prepare a customized design for each customer.

Our objective is to design and build a modular Gallium Nitride (GaN) DC-DC converter system that has high efficiency across the full power range of EV's auxiliary systems. Our design will consist of a primary converter module and additional converter module connected in parallel to the primary converter. The primary converter will always be on to ensure power always reaches the auxiliary systems. The additional converter modules will be turned on and off based on the current-draw of the auxiliary systems to ensure that the converters are always running within a current range around the max efficiency point, as illustrated in [1, fig.1]f. This design will improve upon existing solutions as it will have high efficiency across a wide power range, in contrast to existing DC-DC converters, which only have high efficiency for a small range of powers. Our design is applicable to a wide range of applications and could potentially be used as a universal DC-DC conversion system.

1.2 Background

DC-DC converters heavily rely on semiconductor field effect transistor (FET) switches for their conversion process. The current state of art is Silicon and Silicon Carbide FETs [9]. GaN power switches have smaller on-resistance than standard switches due to their high electron mobility, which leads to lower switching losses especially at low power operations [23]. Therefore, we obtain a higher overall converter efficiency. The tradeoff for using GaN power switches is that their suggested maximum operating voltage is 480 V[24]. This limits our design to EV's powered with 200-480 V propulsion batteries, which still applies to many EVs.

The use of a modular design allows for smaller passive components to be used in each converter module as the power requirement for each is smaller. This is essential in creating a more efficient converter because a single converter rated for the highest power would require much larger

components such as a larger inductor, transformer, and capacitor. These components would be inefficient due to excess heat loss when the auxiliary systems are using lower current levels, such as in the case where only headlights or the entertainment system is on. The use of smaller components leads to reduced losses and higher efficiencies up to 97 percent [16].

1.3 Functional Overview

Each module will be on a separate board. Modules will be physically stacked on top of the primary board as elaborated in Section 1.4. When used in an EV, the power inputs from the propulsion battery will be connected to each board in parallel and the outputs of each board will be connected in parallel to the auxiliary systems. When more current is drawn by the auxiliary systems, the control logic will switch on additional converter modules until enough converters are on to adequately convert the larger amount of power needed. Similarly, when less power is needed for conversion, some power converters will be turned off to ensure the converters are running at maximum efficiency.

In this design we will be using 13.8V as our auxiliary voltage output of the converters. Due to the lack of very high voltage supplies at our disposal and safety concerns, we will be limited to a 80V power supply to simulate our EV propulsion battery for testing purposes and are limited to testing a stack of two converter modules. However, we will still be designing for 400 V. As such, when testing the output auxiliary voltage will be reduced. As the output to input conversion ratio for the design is $13.8/400 = 0.0345$, the output voltage during testing will be $0.0345 \cdot 80 = 2.76$ V.

Each converter will be designed to have an efficiency greater than 90% at output current levels between 4 and 10 A. The maximum current draw of our design is limited by the current rating of the passive components in each converter. Each converter will be able to handle a maximum of 20 A. This is so the primary converter can handle the additional current being drawn by the auxiliary systems while additional converters are turning on. Very large spikes in the current drawn by the auxiliary system will not pose an issue due to the inductors included in the power converters. Overall, a stack of converter modules will be able to provide high efficiency auxiliary

power at current draws greater than 4 A (55W), which should be able to efficiently provide the required auxiliary power for an EV.

1.4 Physical Design

The converter modules will be stacked on top of each other using spacer screw PCB pillars. Additionally, multiple board stacks can be placed side by side. This allows the customer to reconfigure the dimensions of the converter system so they can fit it where they need to go in the vehicle. A single control signal that indicates when the previous converter module's current has exceeded 10A is routed between boards. A pictorial representation of how the boards are stacked and where the DC/DC converters generally fit in an electric vehicle is illustrated in [4, fig. 2].

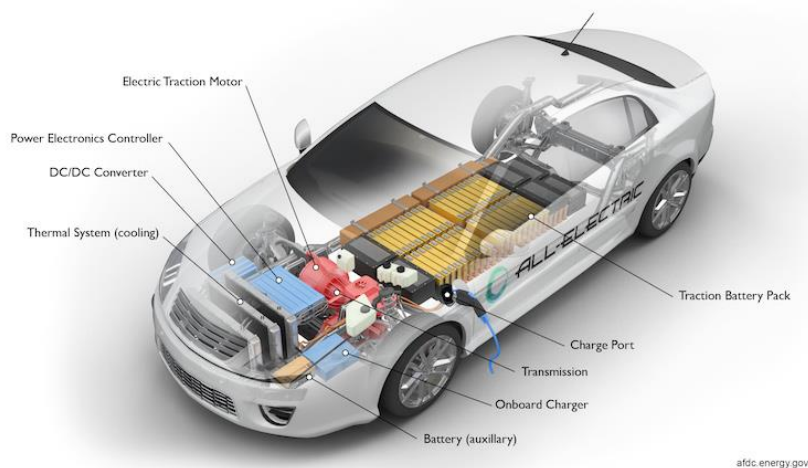
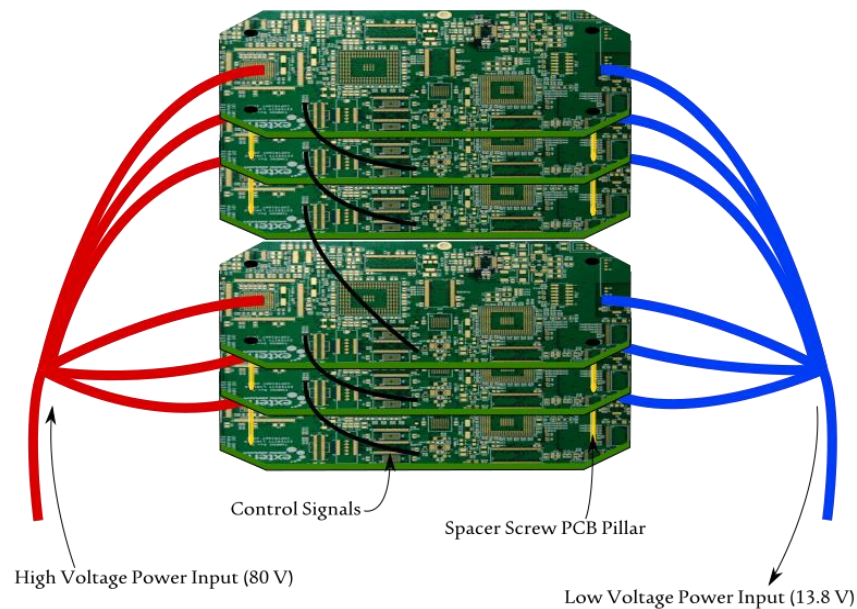


Figure 2: Physical Design [14]

1.5 High-Level Requirements

- At least one power converter module is on at all times so auxiliary systems do not lose power, to ensure the safety of the passengers.
- The full converter system operates at efficiencies higher than 90% at all operating points greater than a 4 A output so that it can be cooled with a passive heat sink and does not require liquid cooling. This will make the design compact and more easily integrated into the EV design as it does not require coolant tubing to be attached for liquid cooling.
- Additional modules are activated within 5% tolerance of the 10A threshold required by the high current threshold sensor, to ensure that converter modules stay within the high efficiency current range.

2 DESIGN

2.1 Block Diagram

There are three main sections of each converter module: the DC-DC power converter, the current sensors, and the control logic. First a power converter is required to convert the 80 V high voltage input of the propulsion battery to 13.8 V for the auxiliary systems. Second, two current sensors are required to determine how much current is being pulled by the load. Lastly, control logic is required to take the signals for the current sensors and output the PWM signals to turn on and off specific converters. All power converters will be identical to the repeatable module shown in the block diagram below, except for the primary converter module. The primary converter module is required to always be on; therefore, it will have an independent PWM generator that is always on regardless of the control signals. Additionally, a low threshold current sensor is not required for the primary converter module as regardless of how low the current gets the primary converter will always be on.

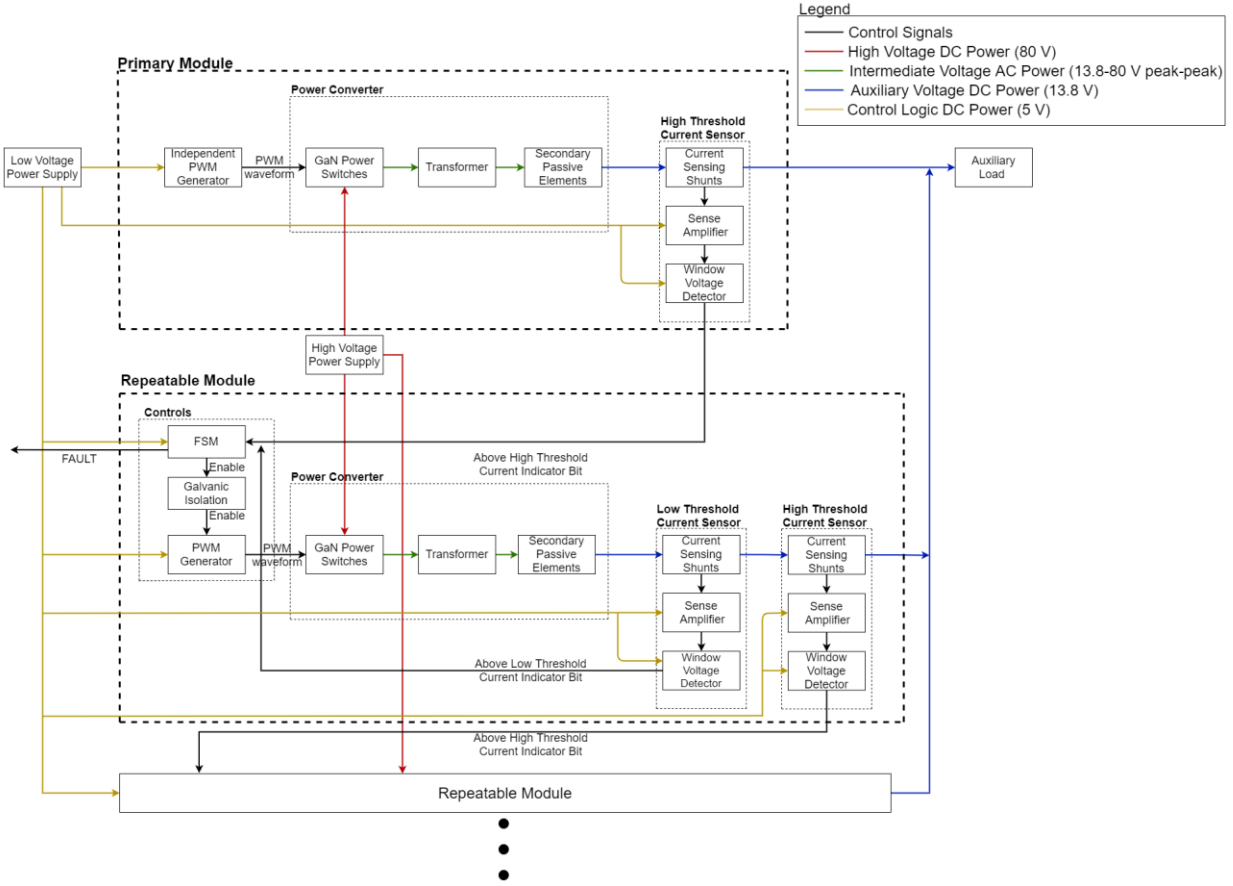


Figure 3: Block Diagram

2.2 High and Low Threshold Current Sensors

Additional converter modules turn on when the current through the previous converter module gets high enough that having more converters on would increase efficiency. The high threshold current sensor (HTCS), present in all converters, detects the current from the converter and outputs a logic high when the current goes above the threshold (10 A). The output of the HTCS is sent to the control logic of the next converter module to indicate when the next module should turn on. All converter modules, except the primary converter module, also turn off when the current flowing through them gets low enough that having less converters on would increase efficiency.

The low threshold current sensor (LTCS) detects the current coming from the converter and outputs a logic low when the current goes below the threshold value. The output of the LTCS for each module is sent to its own control logic to indicate when this module should turn off. By

using both the HTCS and LTCS, the required data can be sent to the control logic so that the right number of converters is turned on to maximize efficiency. The HTCS and LTCS will be identical, with the exception of their threshold values, which will be adjusted by changing the resistance value of the current sensing shunt. Additionally, they consist of a sense amplifier and a voltage window detector. All HTCSs will have a threshold current of 10 A as the converters will be designed to have high efficiency up to 10A. Whenever possible the fewest possible converters will be turned on. This is because with less converters on, the current will be flowing through few passive components, which will reduce losses maximizing efficiency. As such, the threshold for the LTCS will be set for each converter module such that if that converter module is turned off the remaining converter modules that are on will be providing 10 A each. Accordingly, the thresholds of the LTCSs in each converter module is dependent on how many other converters are on. The calculation of the threshold current for the LTCSs is detailed in [32 (appendix), fig. 12]. The resulting threshold is illustrated in [7, eq. 1] for the n th converter, where the n th converter is defined as the converter that turns on after $(n-1)$ other converters are turned on.

$$I_{threshold} = \frac{(n-1)}{n} \times 10 \text{ A} \quad (\text{Eq. 1})$$

2.2.1 Current Sensing Shunt

The current sensing shunt is used to create a small voltage difference that is proportional to the current coming from the converter. The WSB58518 series power resistors were chosen as the current sensing shunt as they can withstand currents above 20 A. This is to ensure that too much power is not consumed, and efficiency stays high. They are sold in small resistance increments to allow for fine tuning of the resistance values, which is critical for high accuracy thresholds for the current sensors. They also have a less than 1% change in resistance value when heated up 170°C, which is important to ensure the current sensor's threshold level does not change if the board heats up. The resistance value of the current sensing shunt is used to adjust the threshold of the current sensor. This resistance value (R_{SENSE}) is calculated using [7, eq.2], using the voltage gain of the sense amplifier (A_v), the window voltage detector's internal threshold voltage ($V_{threshold}$), and the target threshold for the current sensor ($I_{threshold}$).

$$R_{SENSE} = \frac{V_{threshold}}{A_v \times I_{threshold}} \quad (\text{Eq. 2})$$

2.2.2 Sense Amplifier

The sense amplifier detects the voltage across the current sensing shunt and amplifies it. The amplified voltage is fed to the window voltage detector. The LMP8640 sense amplifier was chosen for its high input resistance of 5 k Ω . This will prevent it from being damaged when high currents are flowing through the current sensing shunt, as when the current splits only a small amount of current will flow into the sense amplifier. With 20 A maximum current flowing through the current sensing shunt 0.8 μ A will flow through the sense amplifier, which is less than its maximum current input of 21 μ A. Furthermore, it has a wide operating input voltage range (-6 V to 6 V), which will allow for the detection of currents up to 20 A without the sense amplifier being damaged.

2.2.3 Window Voltage Detector

The window voltage detector takes the output from the sense amplifier as an input and digitizes it as a one bit value. It does so by using an internal threshold voltage. When the voltage input to the window voltage detector is above the internal threshold it will output a logic high value. When the input is below the internal threshold it will output a logic low value. This output value is fed to the control logic. The TPS3700 window voltage detector was chosen for its accurate threshold voltage with very little deviation from chip to chip, as it will allow for the current threshold of the current sensors to be set precisely. It also has a wide operating input voltage range (-0.3 V to 7 V), which will allow for the detection of currents up to 20A without the window voltage detector being damaged.

2.2.4 Current Sensor Schematic

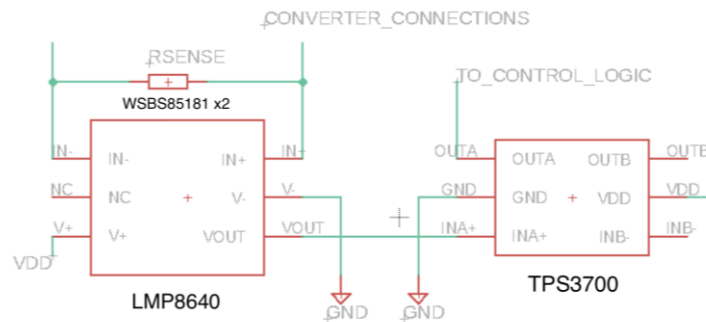


Figure 4: Current Sensor Schematic

2.2.5 Current Sensor Requirements

Requirements	Verification
1. The current sensing shunt maintains a temperature below 170°C , when the current through it is up to 20 A, to ensure there is no change in its resistance value. A change in the resistance value would alter the current through the sensors leading to faulty operations which needs to be prevented.	1A. Attach a high current power supply set to 13.8 V across the current sensing shunt in series with a variable load (simulating the auxiliary load). 1B. Adjust the variable load to adjust the current through the current sensing shunt. 1C. Using an infrared thermometer measure and note down the temperature at different current levels between 4A and 20A in 4A increments. 1D. Plot a graph of temperature vs current level through the current sensing resistor to present the results.
2. The output of the sense amp should be 400mV (window detector threshold) when the current through the current sensing resistor is within a 2.5% tolerance of threshold of each current sensor (dependent on the type of current sensor and which converter module it is on as discussed in the introduction to section 2.2).	2A. Attach a high current power supply set to 13.8 V across the current sensing resistor in series with a variable load (simulating the auxiliary load). 2B. Adjust the variable load to adjust the current through the current sensing shunt so that it is within the tolerance range around the current threshold. 2C. Using a multimeter measure and note down the voltage at the output of sense amplifier when referenced to ground at different current levels within the tolerance range around the current threshold in 1% increments of the 2D. Plot a graph of the sense amplifier's output voltage vs current level through the current sensing resistor to present the results
3. The window voltage detector outputs a high value when the current through the current sensing resistor is above threshold of each current sensor with a 2.5% error tolerance (dependent on the type of current sensor and which converter module it is on as discussed in the introduction	3A. Attach a high current power supply set to 13.8 V across the current sensing resistor in series with a variable load (simulating the auxiliary load). 3B. Adjust the variable load to adjust the current through the current sensing shunt. 3C. Using a multimeter measure and note down the voltage at the output of window voltage detector when referenced to ground at different current levels between 4A and 20A in 4A increments.

to section 2.2).	3D. Plot a graph of the window voltage detector's output voltage vs current level through the current sensing resistor to present the results
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2.3 Control Logic

The control logic for each module takes in the output of the HTCS of the previous module and the output of its own LTCS. The control logic uses these signals to decide whether the converter should be on and outputs a PWM signal to the power converters. The output of the control logic will be fed into the GaN power switches inside the power converter. An FSM is included in the control logic design to synchronize this process to reduce the likelihood of spikes and glitches in the output of the current sensor from affecting the output of the control logic. This is crucial as repeatedly and abruptly turning on and off the power switches can lead to erroneous characteristics for the converter and can damage circuit components. Additionally, a PWM generator with enable/disable capabilities will be used to generate the PWM signal required for the power switches.

2.3.1 FSM

The FSM holds the state of the control bit `Converter_State`, which indicates when the converter is on by holding a logic high value and when the converter is off by holding a logic low value. Two additional registers are used to synchronize the inputs from the previous module's HTCS (`SENSE_HP`) and the inputs from this module's LTCS (`SENSE_LC`). An additional state `Power_Up` is added to indicate when the converter is done powering up to ensure that the converter powers up fully before the control logic can decide to power it down. `Power_Up` will hold a logic low value while the system is still powering up and a logic high when it is done. The converter should turn on anytime the previous module's HTCS outputs a logic high signal and should stay on if this module's LTCS outputs a logic high signal or when the converter is still powering up. `Converter_State` is the output of the FSM and is fed to the PWM generator of this converter as the `ENABLE` bit. Lastly, the FSM will also output a `FAULT` signal, which will indicate when there is an issue with the converters. The `FAULT` signal will be high when the `SENSE_HP` signal is on for more than 1 ms. This is an indication that there is an issue with the additional converters turning on as they generally take 10s of μ s. This can also be an indication

that the current draw of the auxiliary systems has exceeded that maximum that the converter stack can safely provide. The clock for our FSM will be provided by the LTC6900 oscillator chip, which was chosen for its low rise and fall times and its minimal variation in operating frequency with temperature changes. This will allow for a robust FSM that is not affected by temperature. The oscillator will be run at max speed providing a clock signal with a 20 MHz frequency. The circuit schematic of this FSM in [11, fig.5].

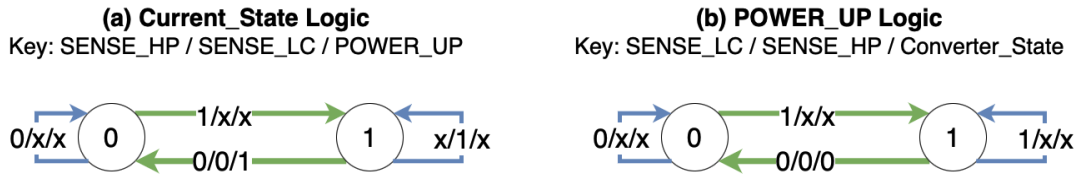


Figure 5: FSM State Diagram of Control Subsystem

2.3.2 PWM Generator

The PWM Generator consists of 2 chips, PWM controller and a PWM driver. The PWM controller creates a low power PWM signal and PWM driver amplifies that signal so that it can drive the GaN power switches. The PWM Generator will take in the output of the FSM as the ENABLE bit. When this ENABLE bit is high the PWM drivers will output the amplified PWM signal to turn on the converter. When the ENABLE bit is low the PWM Driver will output 0 V, which will turn off the converter. The LTC6992 PWM controller was chosen for its high accuracy frequency control with a <1.7% error in the output frequency. As efficiency is dependent on switching frequency this will allow us to accurately set the switching frequency for maximum efficiency. Additionally, the LTC6992 allows for the duty cycle of the PWM signal to be easily set using a single analog signal, making it easy to set the conversion ratio of the converters. The TI LMG3410R050 GaN power switches were chosen as they have integrated PWM Drivers in the same chip, which allows for a smaller design and reduces the complexity of our design. The PWM driver will be outputting a PWM waveform with a frequency of 100kHz, and a duty cycle of 43%. Due to the PWM driver being integrated into the GaN power switches, these parameters cannot be individually verified as the PWM waveform is an internal signal inside the chip.

2.3.2 Control Logic Requirements

Requirements	Verification
1. FSM holds the correct Converter_State based on SENSE_HP and SENSE_LP. This is critical to ensure that the correct ENABLE bit is input to the PWM generator to avoid abrupt on and off of the GaN power switches.	1A. Use a power supply set at 5V and mechanical switches to emulate the inputs coming from the control sensors. Additionally, power the FSM with the power supply. 1B. Using an oscilloscope probe the Converter_State output of the FSM with reference to ground to view correct switching
2. FSM holds correct Power_Up based on SENSE_HP, SENSE_LP, and Converter_State. This is to ensure that the additional converter can power up such that the correct inputs are available for the control logic before and when it decides to turn the converter off. This is critical to avoid erroneous operations.	2A. Use a power supply set at 5V and mechanical switches to emulate the inputs coming from the control sensors. Additionally, power the FSM with the power supply. 2B. Using an oscilloscope probe the Power_Up output of the FSM with reference to ground to view correct switching
3. The PWM controller outputs a 100kHz waveform with a 43% duty cycle when ENABLE is high.	3A. Use a power supply set at 5V and mechanical switches to emulate the inputs coming from the control sensors. Power the FSM with the power supply. 3B. Set the input values of the FSM such that outputs a logic high output for Converter_state output which is the ENABLE signal for the PWM controller. 3C. Using an oscilloscope probe the output of the PWM controller with reference to ground to view the waveform of the output

2.4 Power Converter

The power converter topology for each module will be a *GaN two-switch single-ended forward converter*. This converter will be able to take a 400V input and convert it to 13.8V. This converter will also feature ports that can allow us to create a modular design. This converter topology is selected because of its power conversion ratio of 29.98 (400V/13.8V), transformer galvanic isolation to prevent conduction from the high voltage source to the load, and low component count. When current builds up in the transformer, the core may become saturated and

cause an increase in current destroying components of the circuit. The two switch topology allows for leakage inductance and transformer current to be reset through the path of the diodes during the transistor's off-state, preventing saturation of current in the magnetic core. The component value selections are based on the voltage levels we would like to see at the output and the voltage ripple that is acceptable to us in order for the converter to work safely without compromising any components.

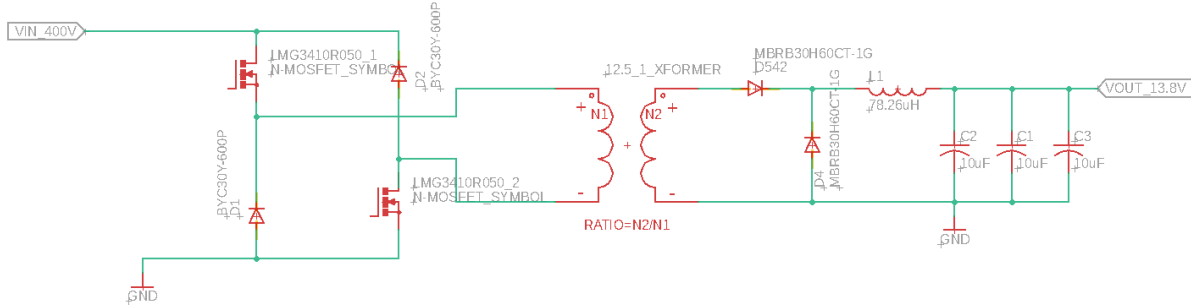


Figure 6: Power Converter Schematic

2.4.1 GaN Power FETs

The GaN power switches are used as our transistors in the converter topology. The GaN FET that we have selected is the TI LMG3410R050. This transistor was selected due to its high voltage tolerance, its built in gate driver, protection circuitry, and its ability to handle the switching frequency we require. We have selected our transistor switching frequency to be 100kHz, this value was selected to minimize component size. The sizing of passive components such as inductors and capacitors are inversely related to the switching frequency, and these equations will be detailed in Section 2.4.3. Many designs that use two switch power converter topologies, that deal with voltage conversion ratios on a scale similar to our conversion of 400V to 13.8V, use switching frequencies in the hundreds of kHz range [21][22]. These factors ensure that we can potentially have an input of 400V and reduces the overall complexity of our circuit due to the built-in gate drivers.

2.4.2 Transformer

The transformer will be used in our converter to provide galvanic isolation for safety purposes and bring the voltage down from 400 V. Galvanic isolation allows for no direct conduction path to exist between the high voltage source and output. This prevents high voltages from being

present at the load. The conversion ratio of our power converter will be determined by both the transformer turns ratio (N) and duty cycle (D), which is how long the switch is on per period, as indicated in [14, eq. (3, 4)]. The turns ratio of the transformer- the ratio of wire coils on the primary end of the transformer to the secondary end- will be large enough so that our duty cycle for the converters would not need to be very small. A lower duty cycle is avoided because more energy is dissipated during the transistor's off state causing inefficiencies. This transformer will include windings made of litz wire, which is a type of multi strand wire, to reduce DC and AC resistance [6].

$$\frac{V_{in} \cdot D}{f_{sw} \cdot N_1 \cdot A_c} \leq B_{sat} \quad (\text{Eq. 3})$$

$$V_{out} = D \cdot \frac{N_2}{N_1} \cdot V_{in} \quad (\text{Eq. 4})$$

[14, eq. (3)] is based off of Prof. Arijit Banerjee's ECE 464 course notes, [28 (appendix), fig.7].

[14, eq. (4)] is derived by manual analysis and is shown in detail in [29 (appendix), fig. 8]. V_{in} is the input voltage, D is the duty cycle of the gate driver, f_{sw} is the switching frequency of the transistor, N_1 and N_2 are the number of turns on the primary and secondary side of the transformer respectively, and A_c is the cross-sectional area of the transformer core. The duty cycle needs to be below 50% in order for the leakage inductance in the transformer core to be reset and prevent core saturation [15]. Using [14, eq. (4)], we decided to choose a turn ratio of 12.5:1, which satisfies our input voltage (400V) to output voltage (13.8V) requirement. Although a variety of turns ratios could be used, this value was chosen because it would allow us to have a duty cycle that wouldn't be too low but also stay below 50 %. Knowing the turn ratio, we can choose our duty cycle to be exactly 43 %. If the duty cycle were to be too low, that would mean a longer time where the transistors are in their off state, leading to power loss through the secondary passive components such as the diode and capacitors. With laboratory experimentation, the duty cycle and the turns ratio as our components on the power converter can be adjusted as they will be through hole and can be easily changed or modified.

We have selected N_1 to be 75, meaning that N_2 would be 6 in order to fulfill the turns ratio of 12.5:1. This is selected because it would lead to lower copper loss (energy lost as heat from the wire) than a transformer with more windings, which would be bulky on the circuit board, and also avoid core saturation for our selected transformer core. Because we have a custom turns

ratio of 12.5:1, there are not many transformers available for immediate purchase with this specification and those available will not arrive in time. Hence, we are using the cores available in the power electronics laboratory. Given that the area of most transformer ferrite cores available will be around 10mm² and have a maximum B_{sat} value of 350mT, N_I must be larger than 49 turns in order to avoid magnetic flux saturation of the core. This estimation is derived from [14, eq.(3)]. Thus, all of our conditions are satisfied with $N_I = 75$.

2.4.3 Secondary Passive Components:

Secondary passive components include the output capacitors, power diodes, and inductor. [15, eq. (5)] is used to determine the values of our output capacitor for our selected two switch forward converter topology[15].

$$C_{out} > \frac{\Delta I_{out}}{2 \cdot \pi \cdot f_{sw} \cdot \Delta V_{out}} \quad (\text{Eq. 5})$$

ΔI_{out} describes the maximum load current at the output, f_{sw} is the switching frequency, and ΔV_{out} is the ripple voltage across the output load. When putting our values of 10A max current, 100kHz switching frequency, and a ripple voltage that is 5 percent of the desired 13.8V output (0.69V), we can see that the output capacitance needs to be larger than 23μH. We have selected to place three 10uF capacitors in parallel in order to satisfy this requirement, and also to decrease the equivalent series resistance of those components. For our inductor, [15, eq.6] was derived through our own calculations and referenced from the ECE 464 course notes, detailed in [32 (appendix), fig. 11]. More regarding the choice of ripple current value is detailed in the following tolerance analysis section.

$$\Delta i_L = \frac{\left(\frac{N_2}{N_I} \cdot V_{in} - V_{out}\right) \cdot D}{L \cdot f_{sw}} \quad (\text{Eq. 6})$$

The peak reverse voltage requirement for the diodes on the secondary side of the converter can be found using [15, eq. (7)] [15]. PIV is the peak inverse voltage for the diode, $N = \frac{N_I}{N_2}$, and $V_{bulk\ max}$ is the maximum input voltage of the power converter, and k_d is the derating factor, which is estimated to be 40 %.

$$PIV = \frac{NV_{bulk\ max}}{1-k_D} \quad (\text{Eq. 7})$$

Plugging in our values of 0.08 for N ($1/12.5$), 400V for input voltage, we see that the reverse voltage requirement of the diode needs to be at least 53V. The ON MBRB30H60CT power diode is selected for the output diodes D3 and D4. It has a 60V reverse breakdown rating and supports up to 30A of average forward current, more than the 20A needed. Furthermore, this diode also has a low forward voltage drop of 0.71V. This means that the average power used will be approximately $20A \times 0.71V$, or 14.2W. The diodes on the primary side of the converter, D1 and D2 on the schematic, will need to support over 400V of reverse voltage. The WeEn BYC30Y-600P supports up to 600V of reverse voltage and is selected for our purposes. This diode has a higher forward voltage of 1.38V but it is lower than most 600V diodes needed for a 400V input.

2.4.4 Power Converter Requirements

Requirements	Verification
1. Voltage measured across the secondary side of the transformer should be the testing input voltage (80V), divided by the turns ratio (12.5) during the transistor on state as illustrated in [31 (appendix), fig. 10]. This value must be accurate within 1 percent for power draws up to 20A in 5A intervals.	1A. Attach digital load across the output of the converter, and vary load starting at 5A. 1B. Attach an oscilloscope across the secondary side of the transformer, and also across the gate of the FET to see if the average transformer voltage is at 6.4V ($80V/12V$) whenever the transistor is switched high. This is to be recorded at each load power interval. 1C. Note any voltage spikes and voltage levels that are not within 1 percent of desired 6.4V ($80V/12V$). Rewind transformer and adjust primary winding to secondary winding ratio if necessary and re-measure voltage.
2. The current ripple across the inductor should be a maximum of 1A, for power draws up to 20A in 5A intervals.	2A. Attach power ammeter probes to the oscilloscope, and probe at the output of the inductor. 2B. Attach digital load to the output of the converter, and vary load starting at 5A. 2C. Record ripple current as value to the peak current from the average inductor current using an oscilloscope. Record for each load power interval. 2D. Adjust inductor size if necessary and re-attach to the same PCB.
3. The output voltage of the	3A. Attach digital load across output of the converter, and turn

power converter should remain within 5 percent of the desired output (2.76V) for power draws up to 20A in 5A intervals. This is to simulate the single converter maximum power scenario.	up the power draw starting at 5A. 3B. Use an oscilloscope to probe the output of the loaded converter. Measure and take note of the voltage ripple levels and average voltage levels for each power draw interval. 3C. Adjust output capacitance values after and re-attach components to the same PCB if necessary. Increase capacitance values if lower voltage variation is required.
4. The power efficiency of a single converter needs to be above 95 percent for power draws up to 20A in 5A intervals.	4A. Attach oscilloscope voltage and current probes across the output of the converter. 4B. Attach digital load across the output of the converter and increase starting at 5A. 4C. Attach current probe from oscilloscope at the input of the converter, taking note of the exact power level at the input of the converter by taking the product of the voltage from the source with the current measured. 4D. Measure power efficiency by dividing output power over the input power at each load interval.
5. The power efficiency of two converters attached needs to be above 95 percent for power draws up to 20A in 5A intervals.	5A. Attach oscilloscope voltage and current probes across the output of each converter. 5B. Attach digital load across the output of each converter and increase starting at 5A. 5C. Attach current probe from oscilloscope at the input of each converter, taking note of the exact power level at the input of the converters by taking the product of the voltage from the source with the current measured. 5D. Measure power efficiency by dividing output power over the input power at each load interval.

2.5 Miscellaneous

2.5.1 *Low Voltage Power Supply*: The low voltage power supply will supply the 5-7V needed for control circuitry and will be taken from bench equipment.

2.5.2 *High Voltage Power Supply*: The high voltage power supply will be set to 80V to simulate an EV's main propulsion battery. This supply will be used to test our design and show increases in conversion efficiency due to lack of access to a 400V power supply and safety considerations.

2.5.3 *Auxiliary Load*: The auxiliary load will be taken from bench equipment and will simulate the auxiliary systems. This load will be taken from the digital load machine in the power electronics laboratory that will simulate 10A of current draw at 13.8V and higher values.

2.6 Tolerance Analysis

The area that poses the highest challenge for proper operation of our project is the power converter. Though every element of the converter requires mathematical analysis to design, the transformer and inductor are selected for further analysis due to the many degrees of freedom that need to be considered when designing essential components for power electronics.

The transformer must be designed so that magnetic flux saturation of the core does not occur. This core saturation may render the transformer unable to perform the task of converting high voltage into low voltage. Core saturation occurs when the magnetic core of the transformer is fully magnetized and cannot produce more magnetic flux. This would result in the transformer ceasing to function and uncontrolled high current levels that may damage other components of the circuit. Additionally, copper loss from the windings in the transformer and core losses of the transformer may be a large cause for inefficiencies of the circuit, which would also render the purpose of the circuit to be not as useful. The elements that are essential in designing a transformer that mitigates these issues are turns ratio, magnetizing inductance, core area, and the magnetic flux saturation limit.

[14, eq. (3, 4)] describe the tradeoffs needed to be made when designing the transformer. Based on these equations, to avoid core saturation it needs to be ensured that the combination of operating frequency, input voltage, duty cycle, and core area are considered. Although we could increase the cross sectional area of the transformer to avoid core saturation, it would also take up more area in our product. A larger core would also cause more core loss, as core loss is proportional to cross-sectional area. An increase in frequency would cause stronger EM interference between the windings which could affect noise levels at our other ICs and reduce efficiency.

These considerations are going to be measured in the lab, but with the cores that we are provided, the best solution is to increase the number of wire windings on the transformer. Though this could result in wire losses, laboratory experimentation is needed to find the exact number of windings that results in the least number of losses. $N_1 = 75$ results in a whole number for the secondary winding so that we can also have a precise transformer turns ratio.

The converter inductor needs to be sized so that we achieve the desired current ripple value. Periodic steady state analysis of the on and off states of the FETs as well as research in the converter topology brings about several equations that relate to the design of these components- derived in detail in the appendix. [19, eq. 8] referenced from ON semiconductor describes the current variation across the inductor [15].

$$\Delta I_L \geq \frac{V_{out}}{L} (1 - DC_{min}) T_{sw} \quad (\text{Eq. 8})$$

[15, eq. (6)] and [19, eq. (8)] give the same result, showing that our manual analysis is accurate. The output current ripple, Δi_L , is selected to be 1A for minimal risk of damaging our components as well as being 5 percent off from our maximum 20A of output current. We are designing to have minimal output current variation, since the exact value of the inductor ripple is generally chosen to be around 20 percent of the maximum output current [25]. However, too much ripple would result in heating of components in DC electronic systems and generate energy losses. A 5 % variation from our output current is a good starting point for testing as it is a small ripple and would not result in a significantly larger inductor. This is a moderately sized inductor that would not take up too much area while functioning with the rest of the design choices. Real output waveforms might differ from what is expected so adjustment of values could be necessary during the testing phase.

$$D = 43\%; N_1:N_2 = 12.5:1; f_{sw} = 43\% \Rightarrow [15, eq. (6)] \& [19, eq. (8)]; L = 78\mu H \quad (\text{Eq. 9})$$

3 COST AND SCHEDULE

3.1 Cost Analysis

Our fixed development costs are estimated to be \$53/hour, 8 hours/week for three people. We consider 70% of our final design completion this semester (15 weeks), neglecting the operations using an actual vehicle.

$$3 \cdot \$53/\text{hour} \cdot 8 \text{ hours/week} \cdot 15 \text{ weeks} / 0.7 = \$27,257 \quad (\text{Eq. 10})$$

Component	Cost (prototype)	Cost (bulk)
GaN FETs (Texas Instruments, LMG3410R050)	\$22.32 (x2)	\$14.23
1m Ω resistor (Vishay/Dale, WSBS85181)	\$14.59 (x1)	\$5.68
Current Sense Amplifier (Texas Instruments, LMP8640)	\$2.36 (x2)	\$1.04
Window Detector (Texas Instruments, TPS3700)	\$1.79 (x3)	\$0.79
Transformer (self-winded with litz wire on ferrite core provided by power electronics lab)	\$9.00	\$6.00
Logic ICs, inductors, and capacitors (digikey, mouser, etc.)	\$12.00 (total)	\$0.30
High Voltage Side Power Diode (WeEn BYC30Y-600P)	\$0.96 (x2)	\$0.75
Low Voltage Side Power Diode (ON MBRB30H60CT)	\$1.71 (x2)	\$0.85
PCB (PCBway, FR4, 3oz, 8 mil min spacing)	\$39.60 (x1)	\$7.75
TOTAL	\$135.26	\$37.40

3.2 Schedule

Week	Tony Xu	Sanat Pandey	Marwan Eladl
02/08	Research converter topologies	Research modular design possibilities	Sense amplifier circuit options
02/15	Converter design v1	Component search and footprint layout on Eagle for known components	FSM, Sense Amp design v1
02/22	Converter design v2	Eagle schematic for controls	FSM, Sense Amp design

03/01	Finalize theoretical converter design and Eagle schematic for converter v2	Project Eagle schematic and PCB layout	Finalize theoretical Controls design
03/08	Power electronics lab visit and transformer winding design, also change design accordingly after design review	Power electronics lab visit; Complete Project Eagle schematic and PCB layout	Power electronics lab visit and transformer winding work
03/15	Simulation of power converter; finalize PCB design v1 for converter	Simulation of HTCS and LTCS; finalize PCB design v1 for HTCS and LTCS; finalize overall PCB v1	Finalize PCB design v1 for control logic
03/22	Work on final simulations of power converter, place second round order if there are modifications based off simulations	Work on final simulations of HTCS and LTCS; finish order placements for all components based off simulations and calculations	Test control logic on a breadboard, place second round order if there are modifications based off simulations
03/29	Solder power converter components and begin testing the subsystem	Solder HTCS and LTCS components and begin testing the subsystem	Solder control logic components and begin testing the subsystem
04/05	Test of power converter circuit modules, make sure all passive component values give proper output result	Test HTCS and LTCS on the PCB, record output result; make changes if required	Test control logic on the PCB, record output result; make changes if required
04/12	Test of power converter combined with control logic and current sensor	Test of power converter combined with control logic and current sensor	Test of power converter combined with control logic and current sensor
04/19	Fine tuning of passive components on power converter, mock demo	Fine tuning of HTCS and LTCS, mock dem	Fine tuning of control logic components, mock demo
04/26	Work on Final Paper	Work on Final Paper	Work on Final Paper
05/03	Presentation	Presentation	Presentation

4 ETHICS AND SAFETY

There are various potential safety hazards and concerns relating to our project. Power electronics deals with power levels much higher than those in most electronic devices [12]. The power electronic converters and transformers can lead to high potential damage which require us to prevent any injury and/or damage to people and property due to electric shock, energy hazards, fire, heat hazards, and chemical hazards [13].

Testing on our project will be done at a maximum voltage of 80V to avoid any possible hazards and ensure feasible results as explained in Section 1.3. We will always have more than one group member present while working on the project in the power electronics lab, in case of emergency. It is critical to ensure that we are aware of what connections are made to ground which will avoid equipment damage due to unintended shorts to ground. We will examine voltage, current, power, and temperature ratings of all the equipment and components used in the project before testing. Furthermore, we will extensively check the temperature of components during operation, using an IR sensor, and ensure that we do not violate any ratings leading to a potential safety risk. We will avoid tools and other metallic objects around live circuits, and we will not make changes with power applied during operation. All these are the precautions and rules which are required to be followed while working in the Power Electronics lab as required [12].

Our project deals with essential components in converting power for automobiles, so safety is paramount for the companies and consumers using our product in their vehicles. The first rule in the IEEE Code of Ethics #1 is: to hold paramount the safety, health, and welfare of the public [11]. That being said, there are a couple of safety hazards for our project while in use. For example, if any passive component in the power converter were to fail from overheating or shorting, there would not be power supplied to the auxiliary systems that are requiring 13.8V. If the converter stops operating, essential auxiliary systems like the headlights and power steering could fail which can lead to the loss of vehicle control. Our circuits try to ensure safety measures are in place by using components that are designed for automobile and high power applications, as verified by the datasheet. Furthermore, we have certain protective measures, such as galvanic isolation that prevents a direct path of current from the high voltage power source to the 13.8V

that the user will be using in the auxiliary unit. Additional safety precautions were put in place through the use of the FSM. The FAULT signal output of the FSM will be used to indicate to the driver that there is an error with the converter module so they should stop the car and call automotive service for help. Furthermore, our PCB will be designed to withstand 80 V and 20 A in areas where high power signals will travel, to ensure that the PCB is not damaged during operation and no arcing occurs, which could potentially cause fires. For standard FR-4 PCB materials the breakdown electric field is $\sim 20\text{kV/mm}$ [26]. This means at 400V the minimum distance between adjacent tracers must be 0.02 mm (0.78 mil). The standard minimum allowed distance between traces on PCBway is 6 mil as such our PCB should be able to easily withstand 400 V. An additional safety concern when running at high voltage is current arcing through the air between lines and causing a fire. To mitigate this, we will be using rounded corners on all high voltage traces, which minimizes the chance of arcing [27]. Lastly, the current routings and traces will be short and wide. Our traces will be 3 ounces, which is $\sim 105\text{ }\mu\text{m}$ deep, and 1cm wide traces, which should withstand 30 A [28]. This gives us a good safety margin as the maximum current output of each converter module is 20 A. The signal traces will be placed in such a way that noise contamination due to power traces is minimized; this ensures signal integrity of the control logic and current sensors, which in turns leads to proper functioning of the modules and reduces the possibility of a malfunction while in a running vehicle [19].

Despite our design choices we cannot ensure a finished product that will be ready to be used in cars on the street. Companies spend thousands of hours testing a single chip used for automobile applications, because that component may be in a car for 20 years and cannot fail even once [17]. Entire reliability teams composed of test, validation, and quality engineers are expected to make sure the proper procedure and software such as analog simulation and RF analysis are used to test these components [18]. We do not have the number of hours to make sure that our product is ready to be used in a car, nor do we have the resources and funding to make sure every test is performed. That is why our product is a proof of concept that our customers, which are likely to be large companies, can purchase and develop further.

Our mitigation strategy aligns with the IEEE Code of Ethics #1-15[11]. There are various issues that come with the access to and applications of a power converter; however, we believe that a

high efficiency modular power converter would really benefit the EV industry which can then lead to more EVs on the streets. This would, over a long period of time, reduce the number of gas-fueled vehicles and hence reduce emissions leading to benefits for the environment.

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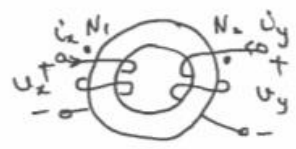
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6 APPENDICES

(5)

ungapped core



Limitation ② Design constraint on the transformer.

- Do not saturate the core.

$$B_{opt} < B_{sat}$$

peak flux in the transformer core $\leftarrow \frac{\phi_{c,peak}}{A_c} < B_{sat}$

Area of the core $\rightarrow$

$$\therefore V_1 = N_1 \frac{d\phi_c}{dt}$$

$$\therefore \frac{1}{N_1 A_c} \int_0^{DT} V_1 dt < B_{sat}$$

or $\frac{V_1 DT}{N_1 A_c} < B_{sat}$

So for given V_1 , D , f_{sw} .

N_1 and A_c should be high to satisfy B_{sat} constraint.

N_1 : more turns $\Rightarrow C_u \uparrow \uparrow$

A_c : more core area $\Rightarrow$ Ferrite/Iron $\uparrow \uparrow$

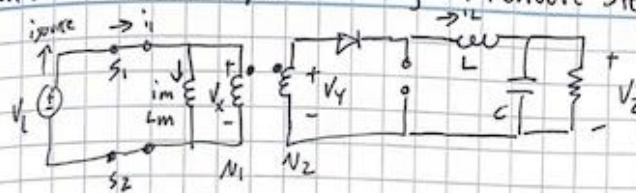
Bigger transformer.

Also, $\phi_c = \frac{N_1 i_m}{R_c} \therefore B_c = \frac{N_1 i_m \mu_0 \mu_r}{l_c}$

Figure 7: Derivation for Equation 1

Derivation of conversion equation using Periodic steady state

Model:



$$V_x = V_1, \quad V_y = \frac{N_2}{N_1} V_1, \quad \frac{N_2}{N_1} V_1 = V_L + V_2$$

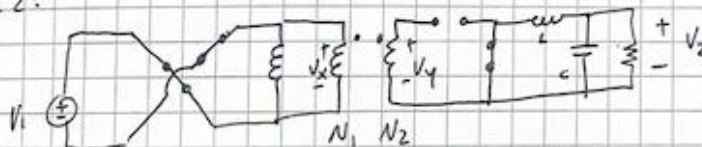
take average $\frac{1}{T} \int_0^T \frac{N_2}{N_1} V_1 dt = \langle V_L \rangle + \frac{1}{T} \int_0^T V_2 dt$

Since $\langle V_L \rangle = 0$ over p.s.s. (periodic steady state)

$$\frac{1}{T} \cdot DT \cdot \frac{N_2}{N_1} V_1 = 0 + V_2 \cdot DT \cdot \frac{1}{T},$$

in model $D \left(\frac{N_2}{N_1} V_1 - V_2 \right) = 0$

Mode 2:



$$V_L = -V_2, \quad \langle V_L \rangle = -\frac{1}{T} \int_0^{(1-D) \cdot T} V_2 dt,$$

$$0 = -V_2 \cdot (1-D) \cdot T \cdot \frac{1}{T}, \quad -V_2 (1-D) = 0 \quad \text{in mode 2}$$

So then

$$D \left(\frac{N_2}{N_1} V_1 - V_2 \right) - V_2 (1-D) = 0$$

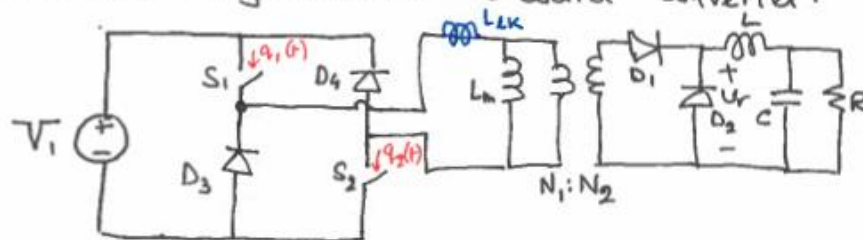
$$D \frac{N_2}{N_1} V_1 - DV_2 = V_2 - DV_2, \quad \boxed{V_2 = D \frac{N_2}{N_1} V_1}$$

Figure 8: Derivation for Equation 2

Lecture 18

Last time : Isolated DC-DC converter .

Two-switch single-ended Forward Converter .

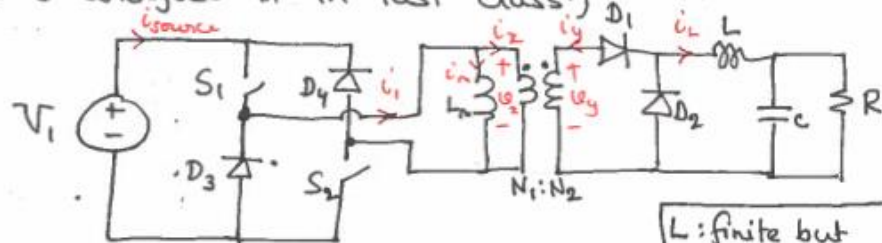


- * Energy recovery even from L_{lk} .
- * More components compared to single-switch forward converter .
- * Leakage leads to commutation of diodes .

Today : ① Challenges of single-ended Forward converter .

② Double-ended Forward Converter .

① Let us ignore leakage for the time being .
(we analysed it in last class.)

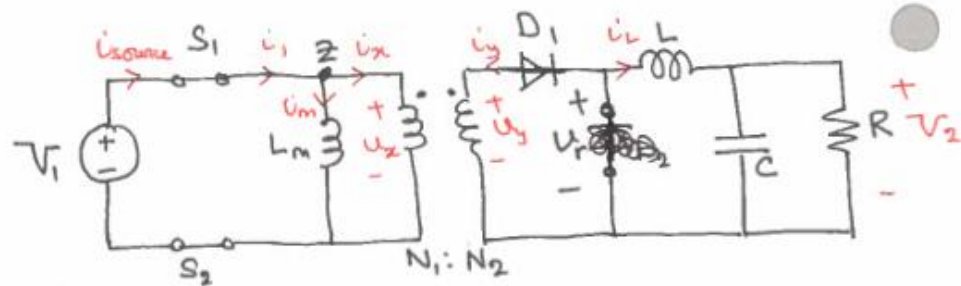


L : finite but in CCM.
 C : Large

Mode I : When S_1 and S_2 is ON

Figure 9: Derivation for Equation 4 (part 1)

$$i_L = I_L + \tilde{i}_L; L \text{ is in CCM.}$$



D_1 : ON
 D_2 : OFF

$$u_x = \sqrt{1} ;$$

For
inductor }
Lm
Magnetizing
inductance }

$$L_m \frac{di_m}{dt} = V_1$$

$$\therefore \Delta i_m = \frac{V_1 DT}{L_m}$$

$$v_y = \frac{N_2}{N_1} \cdot v_1$$

For inductor L {

$$\left\{ L \frac{di_L}{dt} = V_1 - V_2 \right.$$

$$\therefore i_y = -i_L$$

$$\dot{v}_x = \frac{N_2 \dot{v}_L}{N_1}$$

KCL @ Node Z

$$i_1 = i_m + i_x$$

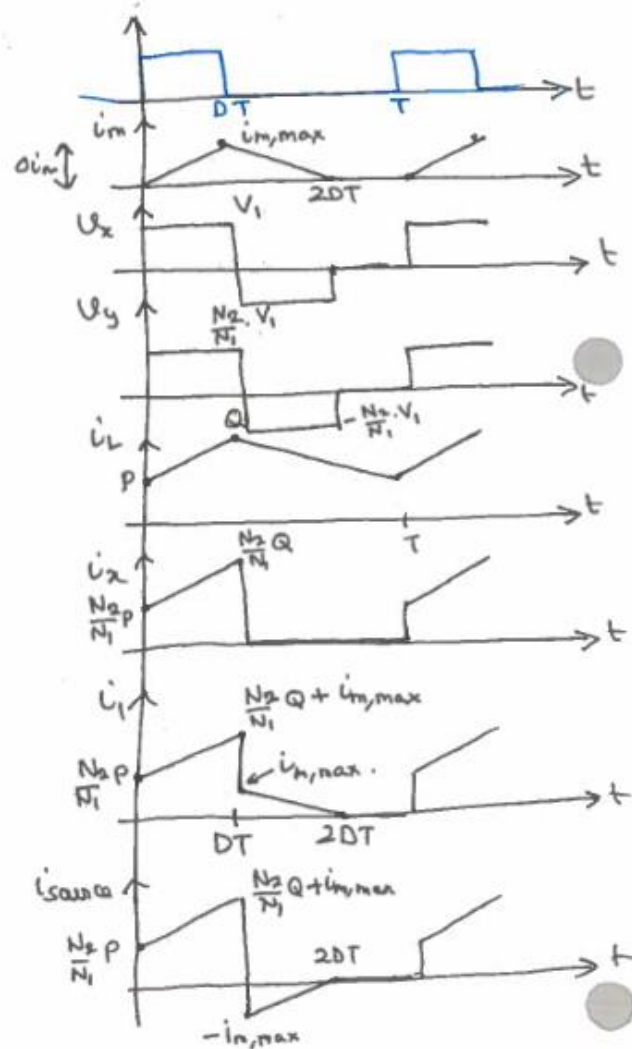


Figure 10: Derivation for Equation 4 (part 2)

$$L \frac{di_L}{dt} = V_y - V_z$$

$$V_y = \frac{N_2}{N_1} V_1$$

Inductor

$$L \cdot \frac{\Delta i_L}{D \cdot T} = \frac{N_2}{N_1} V_1 - V_2$$

$$\Delta i_L = \frac{\left(\frac{N_2}{N_1} V_1 - V_2 \right) \cdot D \cdot T}{L}$$

Figure 11: Derivation for Equation 4 (part 3)

Low Threshold Current Sensor Appendix Entry

- The threshold is set such that if the n^{th} converter is turned off the remain converters each provide 10 A.

$$I_{\text{total}} = (n-1) \cdot 10 \text{ A.}$$

Alt

While the n^{th} converter is still on, each converter provides I_{total}/n as they are in parallel

$$\therefore I_{\text{low, threshold}} = \frac{(n-1)}{n} \cdot 10 \text{ A.}$$

Figure 12: Derivation for the Threshold of Low Threshold Current Sensor