High-Speed NRZ SerDes Receiver in 65-nm CMOS

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***Abstract*—High-speed serial links have become fundamental to modern computing and communication systems, enabling efficient and fast data transfer across printed circuit boards, cables, and backplanes while minimizing pin count and power consumption. The widely adopted serializer/deserializer (SerDes) architecture addresses many of the fundamental limitations of wide parallel interfaces, including excessive I/O pin requirements, clock skew between parallel lanes, increased EMI, and higher power consumption. In this project, we propose the design of a 5 Gb/s NRZ SerDes receiver. At this data rate, channel loss, ISI, and timing uncertainty can significantly degrade signal integrity. Therefore, emphasis will be placed on demonstrating the impact of channel loss and the effectiveness of equalization techniques through eye diagram analysis and BER estimation. As an advanced feature, we aim to implement adaptive equalization techniques that enable self-tuning of our chip's equalization blocks; this is extremely useful at high data rates as the channel properties will vary depending on the interface used.**

I. Introduction

Using parallel data buses becomes impractical at higher speeds due to several fundamental limitations. Wide parallel interfaces require a large number of I/O pins, increasing chip area and package complexity, and suffer from higher power consumption and EMI. Additionally, maintaining precise timing alignment across multiple parallel lanes becomes increasingly difficult due to clock skew, process variations, etc. These challenges motivated the transition to SerDes architectures, where parallel data is converted into a high-speed serial stream at the transmitter (TX) and reconstructed at the receiver (RX).

However, serial transmission introduces new challenges associated with high-speed signaling over bandwidth-limited channels. PCB traces and cables exhibit frequency-dependent loss, reflections, and dispersion, which distort the transmitted waveform and introduce intersymbol interference (ISI). Additionally, at our target data rate of 5 Gb/s, the bit period is only 200 ps, leaving a narrow timing margin for accurate signal detection. Furthermore, SerDes links do not transmit a dedicated clock signal, which requires the RX to recover timing information from the incoming data stream.

To address these challenges, our proposed receiver will incorporate key blocks used in modern SerDes designs, including a half-rate Clock and Data Recovery (CDR) loop integrated with an analog front-end comprising a Continuous-Time Linear Equalizer (CTLE) and a Decision Feedback Equalizer (DFE). A deserializer block will convert the serialized data to the desired parallel output.

A 5 Gb/s NRZ SerDes receiver strikes a good balance between complexity and feasibility for a semester-long effort. Given the complexity inherent in the receiver itself, we will only be designing the RX. The TX will be emulated using a Bit Error Rate Tester (BERT), discussed later in Section IV.

II. Target Specifications

The list below is a good starting point for our project. As our work progresses, it is possible additional specs may be added to the list, while some of the given specs may need to be modified. The BER spec is quite important to our design, as the RX must reliably maintain good signal integrity.

- Data Rate: > 5Gb/s
- Signaling scheme: Non-return-to-zero (NRZ), implemented using differential signaling
- Bit Error Rate (BER): $< 10^{-12}$
- Power Consumption: < 5mW, 5pJ/bit
- Supply Voltage Range: 1-1.2V
- Area: $< 1\text{mm}^2$
- Serialization Factor: 1 serial lane to 4 parallel lines

III. System Architecture

The top-level block diagram of our proposed chip is illustrated in Figure 1. The individual blocks are discussed in the remainder of this section along with any necessary sub-block diagrams.

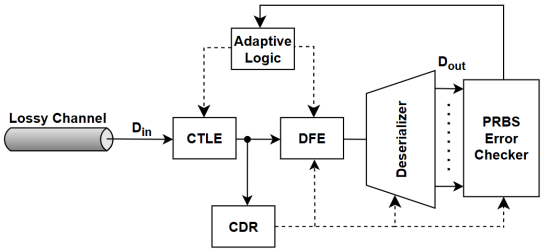

Fig. 1: SerDes top-level block diagram.

A. Continuous-Time Linear Equalizer (CTLE)

As Figure 2 suggests, all real channels have some frequency-dependent loss profile. At the low GHz-range frequencies we want to operate our chip at, a loss of, at minimum, a few dB is essentially guaranteed. The CTLE, as the name suggests, is an analog circuit designed to perform the first stage of equalization of the signal. It accomplishes this by providing sufficient gain at the high frequency components of the signal that are typically attenuated by the channel, thus equalizing the signal over all frequencies within bandwidth.

If we have a fixed channel, then we can measure the loss profile (S-parameters) as a function of frequency and design our CTLE with the exact profile in mind. However, if the characteristics of the channel are unknown to us (which is often the case practically), then it would be necessary to make the characteristics of the CTLE programmable. This includes being able to adjust the input impedance for

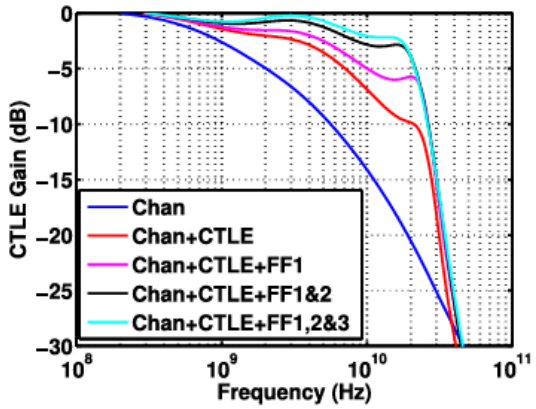

Fig. 2: Some possible frequency response plots [3] for the channel-CTLE cascade. The CTLE helps reduce the roll-off due to the lossy channel.

impedance matching with the channel, the bandwidth to ensure the equalization is at least above the Nyquist rate, and the peaking gain to ensure good signal integrity for the subsequent components.

1) Advanced Feature: Provided the fundamental features of the SerDes have been completed first, a potential advanced feature that may be implemented would be a form of adaptive equalization. As illustrated in Figure 1, one way to accomplish this is through the use of an on-chip error checker. As we discuss in more detail in Section IV, the input to the channel is generated using a Bit Error Rate Tester (BERT). This equipment can generate a pseudorandom binary sequence (PRBS), a quasi-random sequence of bits, and send it to our chip via a PCB trace. Since PRBS is deterministic in nature, the on-chip checker can compare the input bits and output bits and send an error (feedback) signal to our adaptive logic circuitry. Thus, if the initial BER is too high, the CTLE and DFE blocks will be automatically tuned until an optimal BER is achieved.

B. Decision Feedback Equalizer (DFE)

The DFE is a non-linear equalizer designed to mitigate post-cursor inter-symbol interference (ISI). Unlike the linear equalization which often suffers from high frequency noise amplification and channle notch effect, the DFE improve signal integrity through subtracting the weighted influence of the previously detected bits. For a 5 Gbps application, the primary design constraint is closing this critical feedback path within a single 200ps Unit Interval (UI). To achieve this while simultaneously easing high-speed clock distribution, we chose a direct-feedback, half-rate architecture that operates on the half-rate clock recovered in the CDR.

1) Summation Node: The analog summer acts as the primary junction for subtracting the post-cursor ISI of the previous bit from the current bit. It takes the continuous incoming signal from the CTLE and combines it with the equalization feedback from the h_1 tap. By performing this operation in the current domain, the block is able to achieve high speed analog subtraction prior to digitization.

2) Slicer: The slicers act as high-speed clocked comparators and latches that digitize the analog output of the summation node into a clean digital signal and hold that decision at the output node. The slicer output feeds directly into both the deserializer and feedback tap (h_1).

3) Feedback Tap: The feedback tap is responsible for generating the h_1 equalization weight, corresponding to the ISI tail that needs to be subtracted from the incoming signal. It functions as a 1-bit DAC that takes the previous bit (output of SR latch) and converts it into a weighted analog current. This current is fed directly to the summation node, where it is subtracted from the current bit, forming a feedback loop.

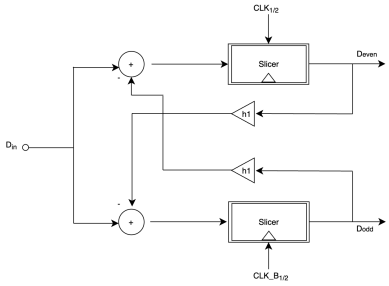

Fig. 3: DFE Block Diagram

C. Clock and Data Recovery (CDR)

The CDR circuit is designed to extract the timing information from the incoming data stream and generate a synchronized clock for data sampling. Since the system is a half-rate architecture, the desired output frequency of this circuit is 2.5 GHz, half of the input data rate. The design constraints of this module include the output stability, as the DFE and deserializer circuits' performance relies on the output of this module. The architecture consist of a Phase Detector, Charge Pump, Loop Filter, and Voltage Controlled Oscillator(VCO).

1) Bang-Bang Phase Detector (BBPD): The phase detector is implemented using a Bang-Bang (binary) architecture consisting of 4 flip-flops and two XOR gates. It compares the phase of the incoming data (D_{in}) with the recovered clock and provides a binary output indicating a 'Lead' or 'Lag'condition.

2) Charge Pump (CP) and Loop Filter (LF): The Charge Pump converts the digital phase error from the BBPD into discrete current pulses. These pulses are integrated by a passive, second-order loop filter to generate the control voltage for the VCO. The filter includes a series resistor and capacitor for stability in a second order system and another capacitor in parallel for ripple suppression caused by the charge pump.

3) Ring VCO: The VCO is implemented as a multi-stage ring of delay cells. The control voltage from the loop filter modulates the delay of each stage to adjust the frequency and phase of the output clock. This ring-based design provides a wide tuning range and compact area, making it ideal for integration.

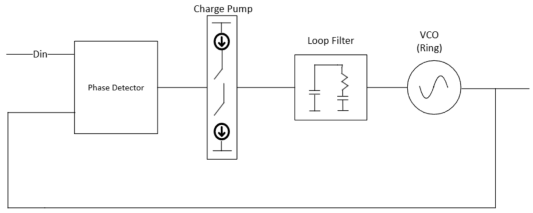

Fig. 4: Architectural Block Diagram of the CDR.

D. Deserializer

The deserializer is the final stage of the RX architecture. This converts the 5 Gb/s serial stream into low-frequency parallel buses for digital processing. Due to the system's implementation as a half-rate architecture, the deserializer is reliant upon a cascaded tree of latches to meet the 1:4 demux ratio . This reduces each lane to 1.25 Gbps per lane.

1) Tree Architecture: The deserializer utilizes the 1:2 split of data performed by the initial samplers of the half-rate system, which capture data on rising and falling edges of the 2.5 GHz clock from the CDR. This acts as a 1:2 demux individually. To reach the required 1:4 ratio, these two streams are demuxed further through a series of latches using a 1.25 GHz clock divided from the 2.5 GHz recovered clock. For more parallel lanes this tree architecture can be further extended from the 1:4 to support 1:8 by cascading latches with a further divided clock.

2) Clock synchronization: The divide-by-2 toggle flip-flop will be implemented by either current mode logic (CML) or standard logic gates. The clocks running the deserializer must maintain a 50% duty cycle to ensure stability for the 1.25 GHz reliant stage of the demux tree, further addressing the cruciality of the CDR performance. Skew minimization and phase alignment ensure the system runs reliably.

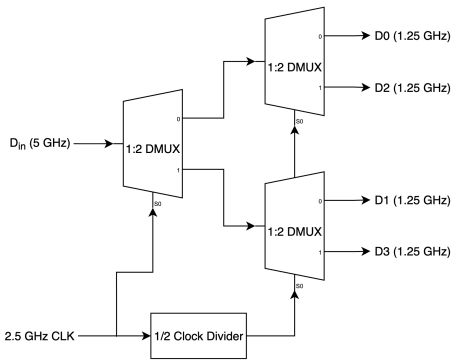

Fig. 5: Architectural Block Diagram of the Deserializer

IV. Testing Plan

The primary method of testing involves using a Bit Error Rate Tester (BERT) to measure the BER of our SerDes receiver. The proposed block diagram for the testing setup is illustrated in Figure 6. The first component of the test setup would be the BERT itself, which can be programmed to generate a pattern of bits (pseudorandom binary sequence (PRBS)) and send it to our chip via a channel (PCB). The BERT can then compare the output bits of our chip with the original bit sequence (error analysis).

Once the data has been deserialized by our chip, a spectrum analyzer and scope can be used to analyze performance characteristics like the clock quality, BER, data rate, power consumption, and eye diagram.

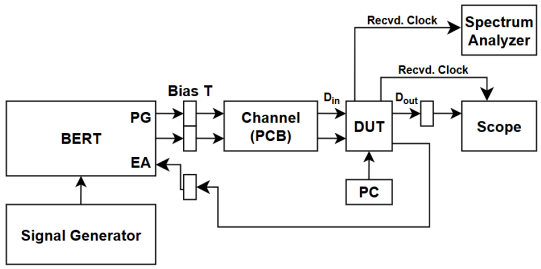

Fig. 6: SerDes test setup

V. Roles

This may change depending on the needs of each block as our project progresses.

- **Continuous-Time Linear Equalizer (CTLE)**: Siddharth Vadyalam, Sourojit Mazumder
- **Decision Feedback Equalizer (DFE)**: Guy Robbins, Pete Sanguanchua
- **Clock and Data Recovery (CDR)**: Qiuyang Lu, Jack Chang
- **Deserializer (DEMUX)**: All

VI. Tentative Timeline

Phase 1: Behavioral Modeling (May to Mid-Summer)
Completion of system-level modeling using SystemVerilog. This phase establishes the architectural parameters for loop bandwidth, equalization levels, etc. before moving to transistor-level design.

Phase 2: Schematic Design & Unit Testing (Mid-Summer to late August)
Design and simulation of individual blocks (CTLE, DFE, CDR, and DEMUX). Focus will be on achieving target performance across PVT corners and ensuring target specs are met.

Phase 3: System-Level Integration (Late August to Sept.)
Integration of individual blocks into a complete receiver top-level schematic. This phase focuses on timing closure between the CDR clock and the DFE feedback loop, as well as verifying global biasing and power distribution.

Phase 4: Physical Implementation / Layout (Oct.)
Transistor-level layout. Key focus areas include symmetric routing for the differential pairs in the VCO and CTLE, and careful placement of the loop filter capacitor to minimize parasitic coupling.

Phase 5: Post-Layout Extraction & Verification (Nov.)
Parasitic extraction and back-annotated simulations. This period accounts for the significant simulation time required

to verify that the integrated system meets the desired BER and data rate targets after accounting for layout parasitics.

Phase 6: Post-Silicon Validation (Spring 2027)

This phase focuses on the PCB and hardware bring-up of the testing setup described in Section IV.

VII. Group Experience

Sourojit Mazumder - B.S. ECE

- Relevant Coursework: ECE 483, 546, 425, 482, 453, 385
- Experience: Incoming Analog IC Design Intern at Infineon Technologies, Device Modeling Intern at Infineon
- Technical Strength: Virtuoso, ADS, Analog Design

Guy Robbins - B.S. ECE

- Relevant Coursework: ECE 483, ECE 482, ECE 453, ECE 425
- Experience: Incoming Hardware Design Intern at Marvell Semiconductor
- Technical Strength: Cadence Virtuoso, Analog Circuit Design

Jack Chang - B.S. ECE

- Relevant Coursework: ECE 483, ECE 425, ECE 444, ECE 486
- Experience: FPGA Design Intern, Altera
- Technical Strength: Virtuoso, Circuit design, System Modeling

Siddharth Vadyalam - B.S. ECE

- Relevant Coursework: ECE 483, ECE 425, ECE 444, ECE 486
- Experience: Incoming Silicon Solutions Engineering Intern at NVIDIA
- Technical Strength: Cadence Virtuoso, Analog Circuit Design

Qiuyang Lu - M.S. ECE

- Relevant Coursework: ECE 483, ECE 482, ECE 459
- Experience: MEMS Oscillator Transimpedence Amplifier Design(TIA), Incoming Analog IC Design intern at Omni Design
- Technical Strength: Analog Circuit Design, Cadence Virtuoso

Pete Sanguanchua - B.S. ECE

- Relevant Coursework: ECE 482, ECE 385, ECE 453
- Experience: Incoming Analog IC Design Intern at Analog Devices, Highspeed Electrical Validation Intern at Astera Labs
- Technical Strength: Cadence Virtuoso, Circuit Modelling, Highspeed IO Testing

References

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