ECE 425 Fall 2019 Course Information

Class Meetings: Tuesdays and Thursdays 15:30-16:50, 3081 ECEB

Instructor
Anu Aggarwal (agganu@*illinois.edu*)
Office hours: T,R – 5-6pm, W-4-5pm , ECEB3044

Course Director
Volodymyr Kindratenko (*kindrtnk@illinois.edu*)

Teaching Assistant
Xinheng Liu (*xliu79@illinois.edu*)
Office hours: Wednesday, 9am-noon, 2022 ECEB
Additional in MP due weeks: Friday 9am-noon, L440 DCL

Text Book

Neil Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th edition.

Recommended Book

De Micheli, *Synthesis and Optimization of Digital Circuits*

Other Reference Books

Sherwani, *Algorithms for VLSI Physical Design Automation*
Rabaey, Chandrakasan, Nikolic, *Digital Integrated Circuits: a Design Perspective (2nd edition)*

Grading

- Homework assignments (three in total): 10%
- Exams (mid-term and final, both in class): 20%+20%
- Machine Problems (four in total): 50%
    - MP0: 2.5%; MP1: 10%; MP2: 25% (checkpoint: 5%, final: 20%); MP3: 12.5%

- Homework will be due on the due dates in class (no late acceptance).
- Machine problems will be due on Compass by 11:59pm on the due dates. You will submit PDF version of the MP report on Compass. All MPs, except MP3, are accepted up to three days late with penalties:
    - 1 day: 90%;
    - 2 days: 70%;
    - 3 days: 50%;
    - >3 days: 0%.

Web page: https://courses.engr.illinois.edu/ece425

Syllabus, class notes, announcements, MP & HW materials, etc. will be posted here.

Piazza: https://piazza.com/illinois/fall2019/ece425

This is the **primary** means of staff-student communication outside of lecture hours and office hours.

Grades and **MPs submission:** https://compass2g.illinois.edu

Grades will be posted in Compass2g. MPs will be submitted electronically via Compass2g as well.

Class Schedule

Week	Date	Lecture	Topic	Due Dates
1	08/27	1	Introduction	
	08/29	2	IC Fabrication	
2	09/03	3	Circuits and Layout	
	09/05	4	MIPS Case Study	
3	09/10	5	CMOS Transistor Theory (1)	
	09/12	6	CMOS Transistor Theory (2)	
	09/13		*Deadline for MP0 report*	MP0
4	09/17	7	MP1 overview; SPICE	
	09/19	8	Combinational Circuit Design	HW1
5	09/24	9	Sequential Circuit Design	
	09/26	10	Wires	
6	10/01	11	Adders	
	10/03	12	Multipliers and Other FUs	
	10/04		*Deadline for MP1 report*	MP1
7	10/08	13	MP2 overview; SRAMs,	
	10/10	14	PLAs, FSMs, ROMs	
8	10/15	15	Modeling Digital Systems, Verilog	HW2
	10/17		*Review for midterm*	
9	**10/22**		**Midterm**	
	10/24	16	Circuit Pitfalls and Design for Testability	
10	10/29	17	Design for Low Power	
	10/31	18	Special topics: Packaging, power and clock	
	11/01		*Deadline for MP2 checkpoint report*	MP2cp*
11	11/05	19	VLSI Design Styles	
	11/07	20	VLSI CAD Tools	
12	11/12	21	High-Level Synthesis	
	11/14	22	Logic Synthesis (1)	
13	11/19	23	Logic Synthesis (2)	
	11/21	24	Partitioning and Floorplan	
	11/22		*Deadline for MP2 report*	MP2
	11/26&28		*Fall break*	
14	12/03	25	MP3 overview, Placement and Routing	HW3
	12/05		*Review for final exam*	
15	**12/10**		**Final exam**	
	12/13		*Hard Deadline for MP3 report*	MP3**

*: MP2cp is a check point, where students need to submit intermediate results on the MP. The purpose of this is to make sure students are making good progress. Delay for submitting MP2cp is counted as delay of the overall MP as well.

**: MP3 has a hard deadline. No late submission is accepted.