Problem Set #4 Solutions

NMOS: $\mu_n C_{OX} = 100\mu A/V^2$; $V_{TN} = 1V$ **PMOS:** $\mu_p C_{OX} = 50\mu A/V^2$; $|V_{TP}| = 1V$

1. Given V_{DD}=5V, $R_1 = 40k\Omega$, $R_2 = 60k\Omega$, $R_D = 2.7k\Omega$, $R_S = 2k\Omega$, $\frac{W}{L} = \frac{450}{1}$, $R_{SRC} = 500\Omega$, and $R_L = 3k\Omega$. Ignore channel length modulation, $r_{ds} = \infty$.

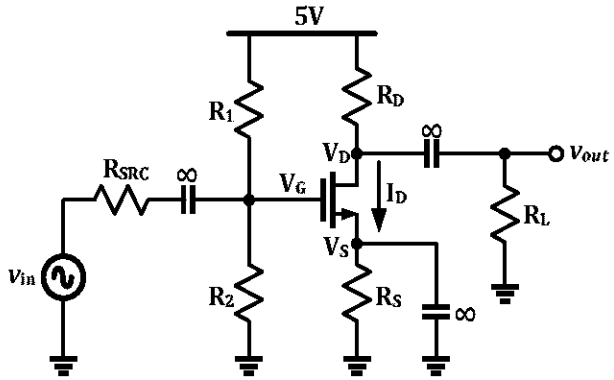
a. Find DC operating point i.e. find I_D, V_G, V_D.

b. Compute transistor g_m

c. Sketch incremental model.

d. Compute DC incremental gain $A_V = \frac{v_{out}}{v_{in}}$.

e. Compute the range of V_D voltages for which transistor stays in saturation.



Assume transistor is biased in saturation:

(a) $V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD} \Rightarrow \boxed{V_G = 3V}$

(b) $I_D = \frac{100\mu}{2} \times \frac{450}{1} \times [3 - V_S - 1]^2$

$V_S = I_D \cdot R_S = 2I_D [V]$

$\Rightarrow I_D = \frac{100\mu}{2} \times \frac{450}{1} \times [2 - 2I_D]^2 \Rightarrow I_D = 1.11mA$ or $I_D = 0.9mA$

case #1: $I_D = 1.11mA \Rightarrow V_S = 2.22V$

$V_D = V_{DD} - I_D R_S = 2V$; $V_G = 3V \Rightarrow$ CUT OFF

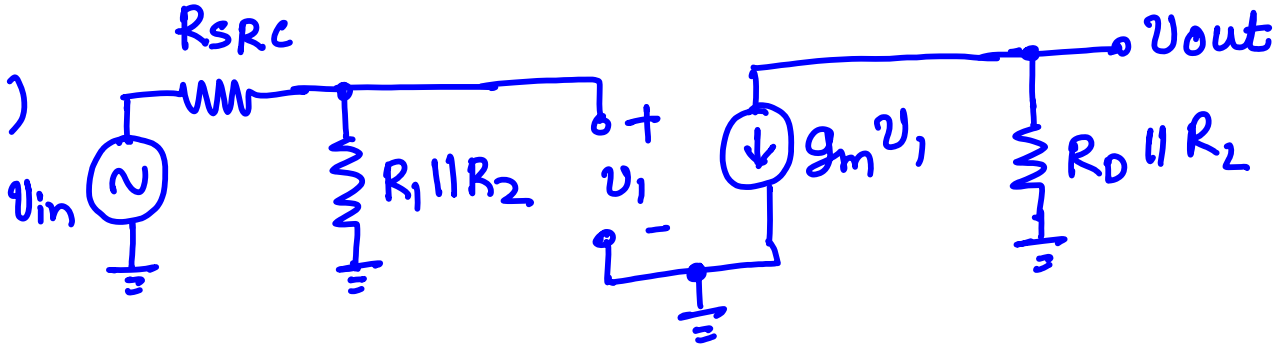
case #2: $I_D = 0.9mA \Rightarrow \boxed{V_S = 1.8V}$ & $\boxed{V_D = 2.57}$

$\Rightarrow V_{GS} > V_T$ & $V_{DS} > V_{OV} \Rightarrow$ SATURATION

$\therefore \boxed{I_D = 0.9mA}$

(b) $g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 0.9m}{0.2} \Rightarrow \boxed{g_m = 9 mA/V}$

(c)



(d) $v_{out} = -g_m \cdot v_1 \cdot (R_D \| R_L)$

$$v_1 = \frac{R_1 \| R_2}{R_{SRC} + (R_1 \| R_2)} \cdot v_{in}$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -\frac{g_m \cdot (R_1 \| R_2)}{R_{SRC} + (R_1 \| R_2)} \cdot (R_D \| R_L)$$

$$\Rightarrow \boxed{A_v = -12.53 V/V}$$

(e) Assuming DC operating point is not altered:

$$V_{DS} \geq V_{OV} \Rightarrow V_D \geq V_S + V_{OV} = 2V$$

$$\Rightarrow \boxed{2V \leq V_D \leq 5}$$

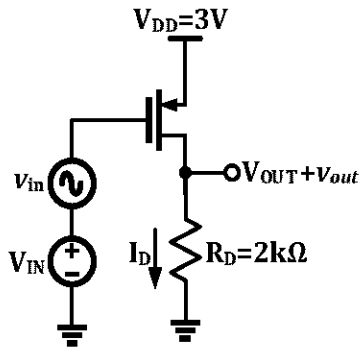
2. Consider PMOS common source amplifier shown below. Given V_{DD}=3V, V_{IN}=1.8V, $\frac{W}{L} = \frac{250}{1}$. Ignore channel length modulation, $r_{ds} = \infty$.

a. Compute I_D and V_{OUT}.

b. Sketch incremental model.

c. Find incremental gain $A_V = \frac{v_{out}}{v_{in}}$.

d. Compute range of output voltage range for which transistor stays in saturation.

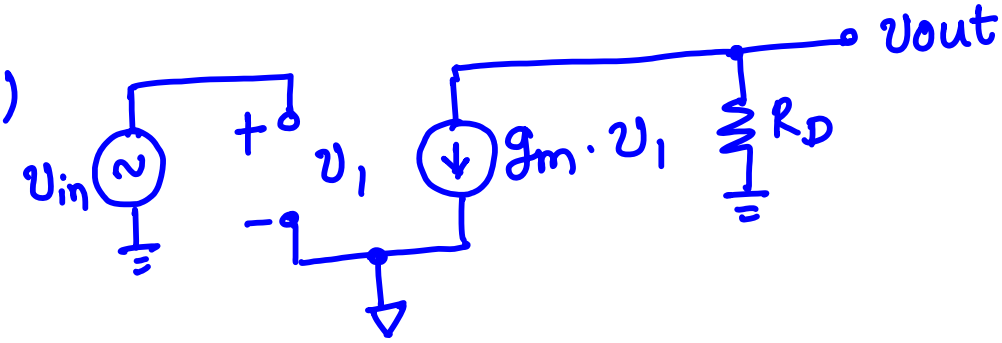


Assuming transistor is biased in saturation:

(a) $I_D = \frac{50\mu}{2} \times \frac{250}{1} \times (3 - 1.8 - 1)^2$

$\Rightarrow$ $I_D = 250\,\mu A$ $\Rightarrow$ SATURATION

(b)



(c) $A_v = -g_m \cdot R_D$; $g_m = \frac{2 \times 0.25mA}{0.2V}$

$\Leftarrow$ $g_m = 2.5\,mA/V$

$A_V = -5\,V/V$

(d) For staying in saturation:

$$V_{SD} \geq V_{OV} \Rightarrow 3 - V_D \geq 0.2V$$

$$\Rightarrow V_D \leq 2.8V$$

$$\Rightarrow \boxed{0 \leq V_D \leq 2.8V}$$