ECE 340
Solid State Electronic Devices

M,W,F 12:00-12:50 (X), 2015 ECEB

Professor John Dallesasse
Department of Electrical and Computer Engineering
2114 Micro and Nanotechnology Laboratory
Tel: (217) 333-8416
E-mail: jdallesa@illinois.edu

Office Hours: Wednesday 13:00 – 14:00

ECE Illinois
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Announcements

- Quiz 2 Regrade Requests Due Today (Monday)
  - Write reason for regrade request on 8.5”x11” paper stapled to quiz
  - Do not write on the quiz
  - Review e-mail sent on part b

Streetman Errata

- Equation 6-35 in Streetman's "Solid State Electronic Devices" 6th edition has a typo:

Equation in Streetman:

$$C_i = \frac{\varepsilon_s}{W}$$

Corrected Version:

$$C_d = \frac{\varepsilon_s}{W}$$

Today's Discussion

- Finish Threshold and Flatband Voltages
- Comments on C-V Analysis
- MOSFET I-V
- Assignments
- Topics for Next Lecture

Tentative Schedule [3]

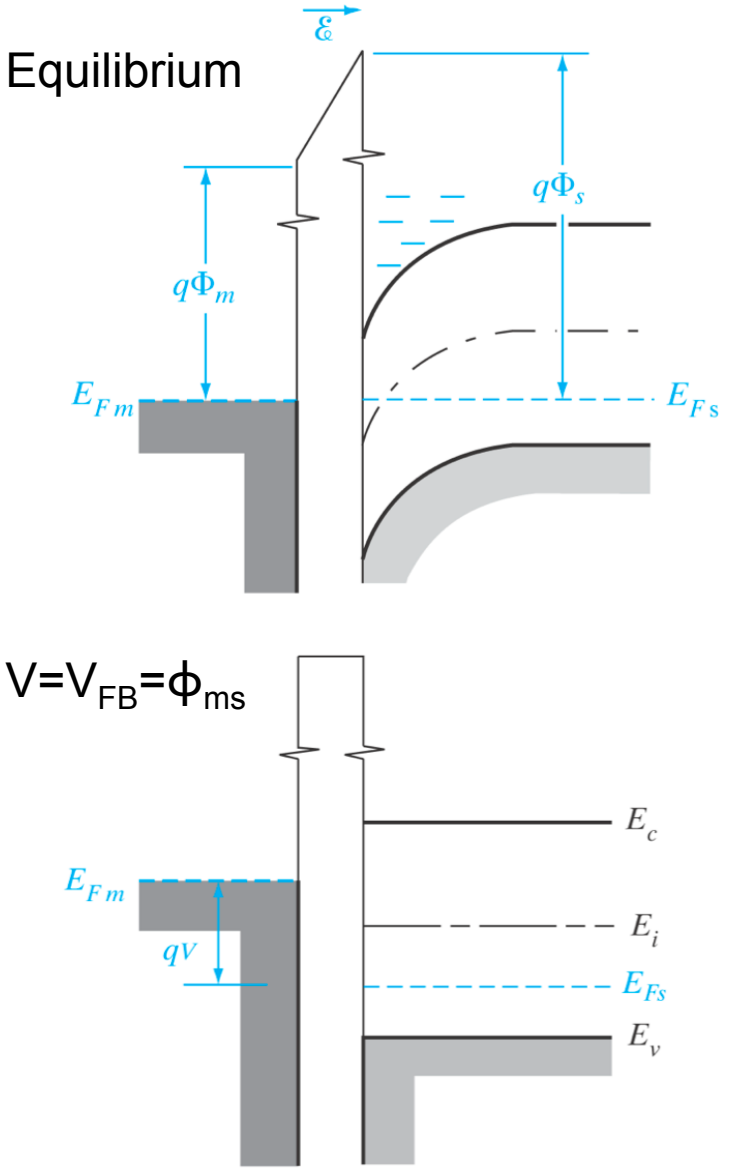
APR 2 LEDs and Diode Lasers	APR 4 Metal-semiconductor junctions	APR 6 MIS-FETs: Basic operation, ideal MOS capacitor
APR 9 MOS capacitors: flatband & threshold voltage	APR 11 Review, discussion, problems (4/12 exam)	APR 13 MOS capacitors: C-V analysis
APR 16 MOSFETs: Output & transfer characteristics	APR 18 MOSFETs: small signal analysis, amps, inverters	APR 20 Narrow-base diode
APR 23 BJT fundamentals	APR 25 BJT specifics	APR 27 BJT normal mode operation
APR 30 BJT common emitter amplifier and current gain	MAY 2 (LAST LECTURE) Review, discussion, problem solving	FINAL EXAM **Date & time to be announced**

Subject to Change

Effects of Real Surfaces

Band Alignment: Differing Work Functions

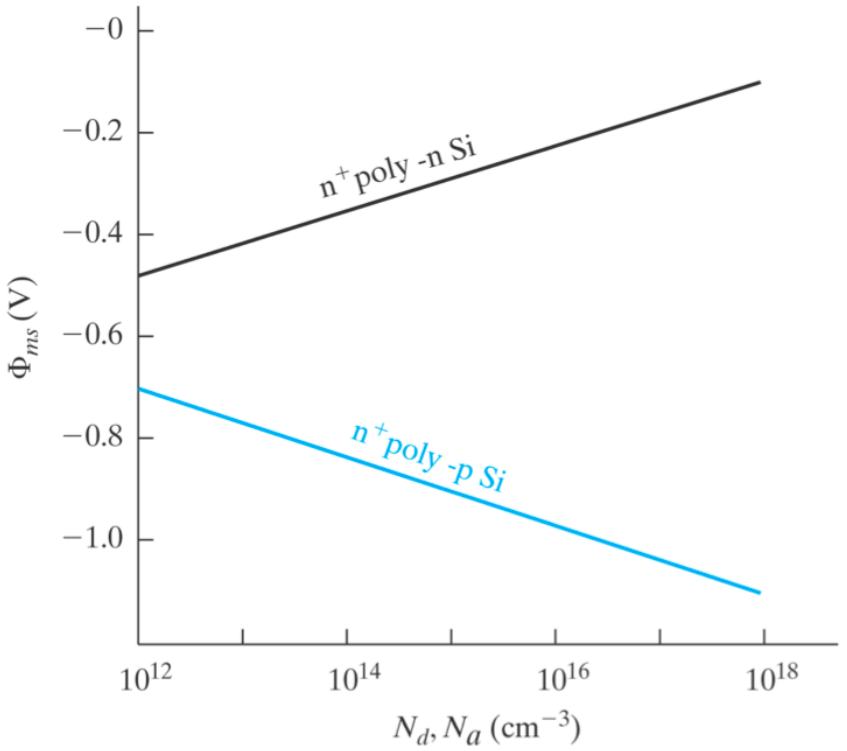
- Alignment of the metal and semiconductor work functions results in a potential difference between the metal and semiconductor
- The potential difference creates an electric field across the insulator, and the metal is positively charged relative to the semiconductor
- If ϕ_{ms} is sufficiently negative, an inversion layer forms with no applied voltage
- To obtain a flat band condition, a negative voltage must be applied to the metal



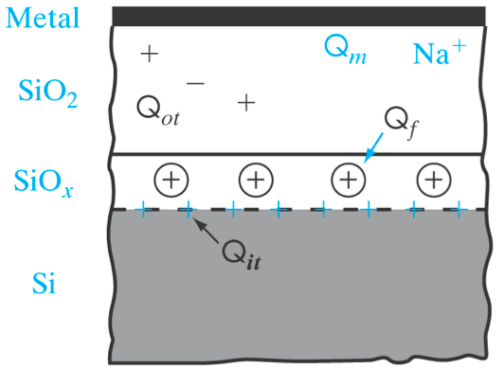
Work Function Difference

- Ideal case assumed that the metal and semiconductor work functions were the same
- Typical materials depart from the ideal case
- The semiconductor modified work function varies with semiconductor doping density (Fermi level changes with doping)
- Note that Φ_{ms} is always negative, and most negative for heavily p-doped material (think of this as the difference between n^+ crystalline silicon and n or p-type material)
- Fermi level alignment can produce an inversion layer with no voltage applied

Metal-Semiconductor Work Function Difference

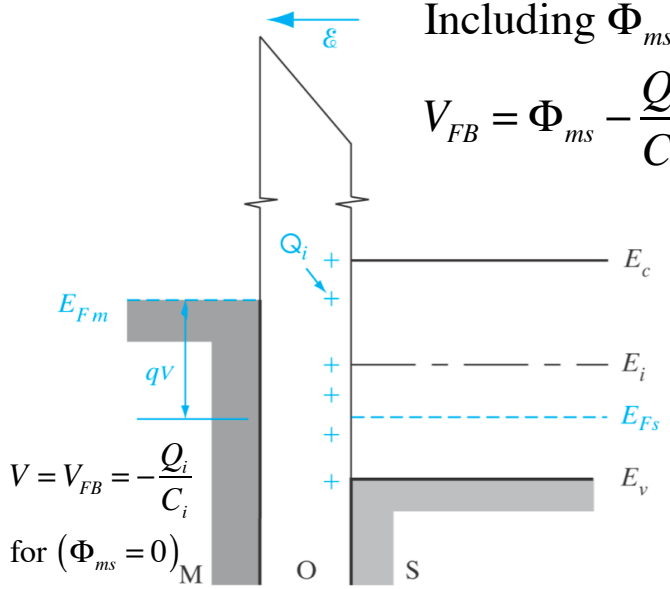


Interface Charge & Flat Band Voltage



Q_m Mobile ionic charge
Q_{ot} Oxide trapped charge
Q_f Oxide fixed charge
Q_{it} Interface trap charge

~10^{10} charges/cm^2 on {100} Si



Including Φ_{ms} :

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i}$$

$$V = V_{FB} = -\frac{Q_i}{C_i}$$

for $(\Phi_{ms} = 0)$

- Charge in the oxide and at the interface comes from a variety of sources
- Mobile ionic charge is typically from contaminants such as sodium
- Oxide trapped charge arises from imperfections in the SiO_2
- Interface states occur abrupt transition between the oxide and semiconductor
- Oxide fixed charge occurs in the transition region between fully oxidized silicon and unoxidized crystalline silicon
- The net positive charge in the oxide requires a negative voltage in the metal to achieve flat bands

Key Definition

- ***Flat Band Voltage:*** Voltage that must be applied to the gate to achieve unbent (flat) bands. This compensates for the work function difference and any interface charge.

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i}$$

Threshold Voltage

Key Definition

- ***Threshold Voltage:*** The gate voltage required to obtain strong inversion.

Threshold Voltage: Ideal Case, n-channel

Charge per unit area
to create depletion region
at strong inversion:

$$Q_d = -qN_aW_m = -2\left(\varepsilon_s qN_a\phi_F\right)$$

$$V_T = -\frac{Q_d}{C_i} + \underbrace{2\phi_F}_{\phi_s}$$

The applied voltage to achieve strong inversion must be large enough to create Q_d plus the surface potential $\phi_s(inv.) = 2\phi_F$.

Threshold Voltage: Ideal Case, p-channel

Charge per unit area
to create depletion region
at strong inversion:

$$Q_d = +qN_dW_m = +2\left(\varepsilon_s qN_d\phi_F\right)$$

$$V_T = -\frac{Q_d}{C_i} + \underbrace{2\phi_F}_{\phi_s}$$

The applied voltage to achieve strong inversion must be large enough to create Q_d plus the surface potential $\phi_s(inv.) = 2\phi_F$.

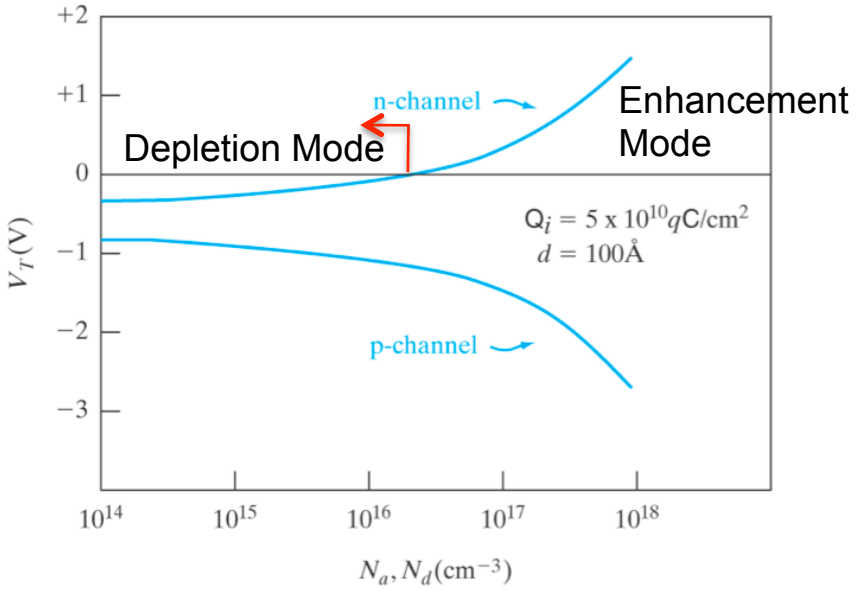
Threshold Voltage

Non-Ideal Case

Threshold Voltage: Non-Ideal Case

- The ideal expression for threshold voltage is modified by the work function difference and interface charge
- p-channel: the negative voltage applied to introduce a channel must be larger than V_T
- n-channel: if V_T is positive, a voltage larger than this must be applied to induce a channel (normally "OFF")
- n-channel: if V_T is negative, a channel exists at V=0 and a negative voltage must be applied to turn the device off (depletion mode, or normally "ON")

$V_T =$	Φ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+ 2\phi_F$
	(−)	(−)	(+) n channel (−) p channel	(+) n channel (−) p channel



$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

Add V_{FB} to $V_{T,ideal}$

Example

Assuming a n^+ polysilicon gate with an n-channel MOS device (p-substrate):

Given $N_a = 5\times10^{15}\,cm^{-3}$, an oxide thickness of 100A, and an interface charge density $Q_i = 4\times10^{10}\,qC/cm^2$, determine C_i, C_{min}, W_m, V_{FB}, and V_T.

$$\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i} = 0.0259\ln\frac{5\times10^{15}}{1.5\times10^{10}} = 0.329eV$$

$$W_m = 2\left[\frac{\varepsilon_s\phi_F}{qN_a}\right]^{1/2} = 2\left[\frac{11.8\times8.85\times10^{-14}\times0.329}{1.6\times10^{-19}\times5\times10^{15}}\right]^{1/2} = 4.15\times10^{-5}\,cm = 0.415\,\mu m$$

From the figure, $\Phi_{ms} \approx -0.95V$

$$Q_i = 4\times10^{10}\times1.6\times10^{-19} = 6.4\times10^{-9}\,C/cm^2$$

$$C_i = \frac{\varepsilon_i}{d} = \frac{3.9\times8.85\times10^{-14}}{0.1\times10^{-5}} = 3.45\times10^{-7}\,F/cm^2$$

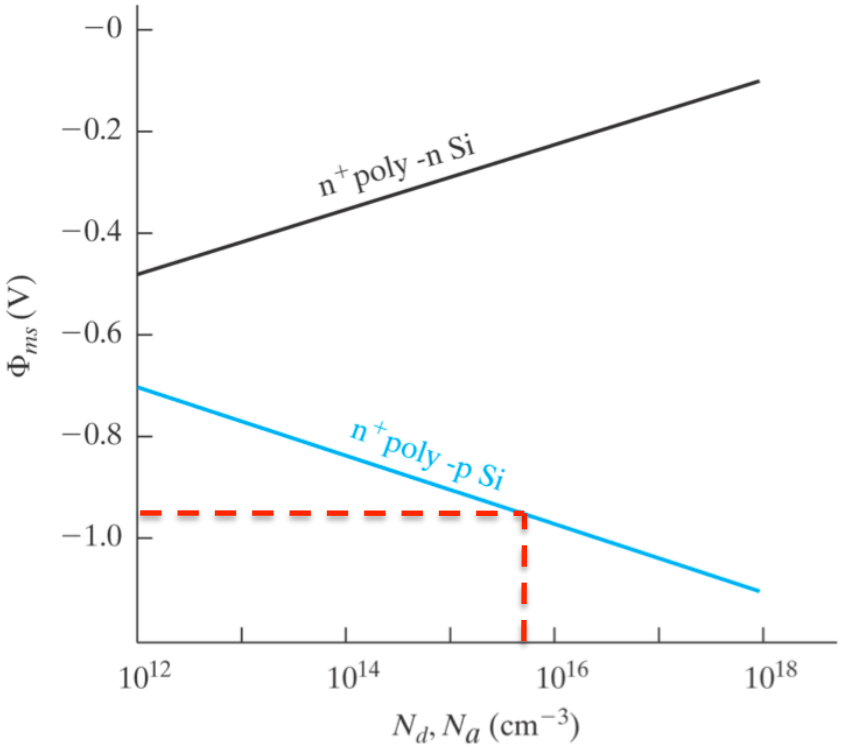
$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i} = -0.95 - \frac{6.4\times10^{-9}}{3.45\times10^{-7}} = -0.969V$$

$$Q_d = -qN_aW_m = -1.6\times10^{-19}\times5\times10^{15}\times4.15\times10^{-5} = -3.32\times10^{-8}\,C/cm^2$$

$$V_T = V_{FB} - \frac{Q_d}{C_i} + 2\phi_F = -0.969 + \frac{3.32\times10^{-8}}{3.45\times10^{-7}} + 0.658 = -0.215V$$

$$C_d = \frac{\varepsilon_s}{W_m} = \frac{11.8\times8.85\times10^{-14}}{4.15\times10^{-5}} = 2.5\times10^{-8}\,F/cm^2$$

$$C_{min} = \frac{C_iC_d}{C_i + C_d} = \frac{3.45\times10^{-7}\times2.5\times10^{-8}}{3.45\times10^{-7} + 2.5\times10^{-8}} = 2.33\times10^{-8}\,F/cm^2$$



MOS C-V Analysis

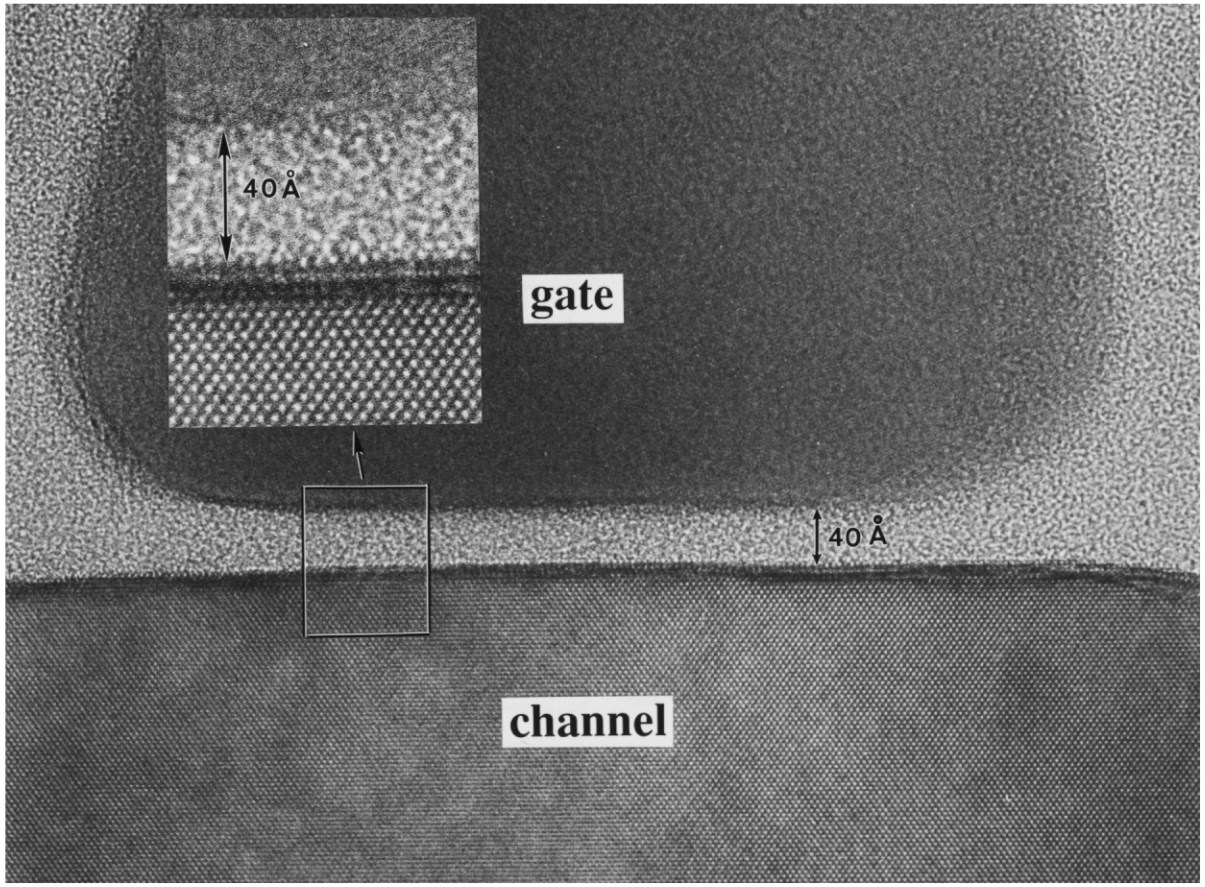
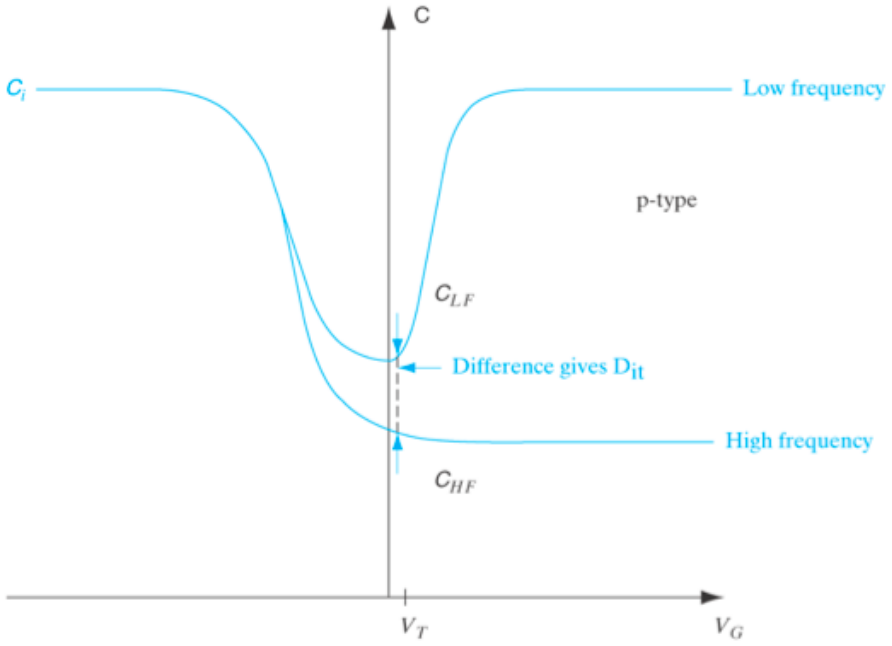


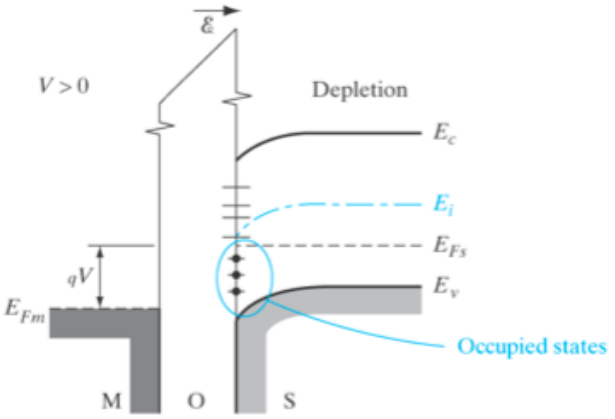
Figure 6.33

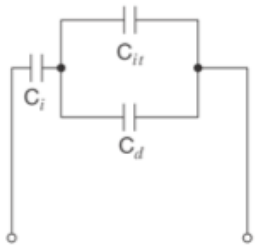
Cross section of a MOSFET. This high resolution transmission electron micrograph of a silicon Metal–Oxide Semiconductor Field Effect Transistor shows the silicon channel and metal gate separated by a thin (40 Å, 4 nm) silicon–dioxide insulator. The inset shows a magnified view of the three regions, in which individual rows of atoms in the crystalline silicon can be distinguished. (Photograph courtesy of AT&T Bell Laboratories.)

MOS Device Parameter Extraction

- Insulator thickness, substrate doping, and threshold voltage can be determined by examining the C-V curve

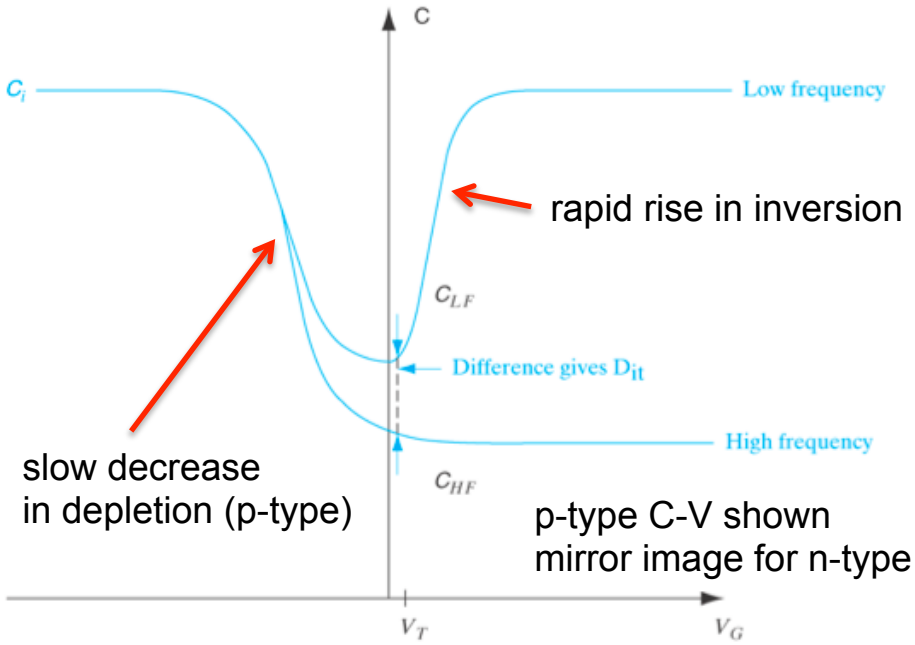


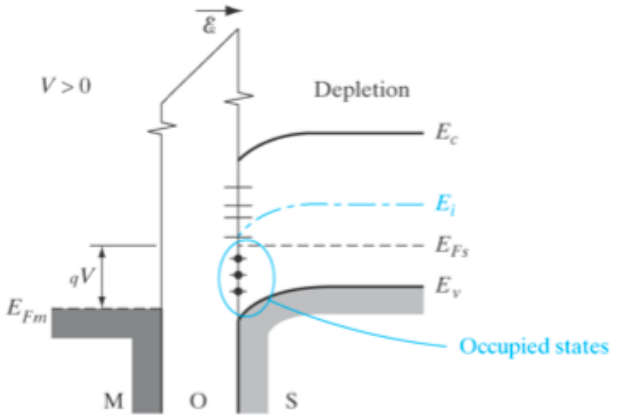


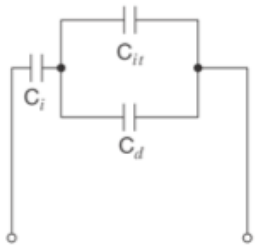


Substrate Doping Type

- p-type substrate: high frequency capacitance large for negative gate biases and small for positive biases
- n-type substrate: high frequency capacitance small for negative gate biases and high for positive biases

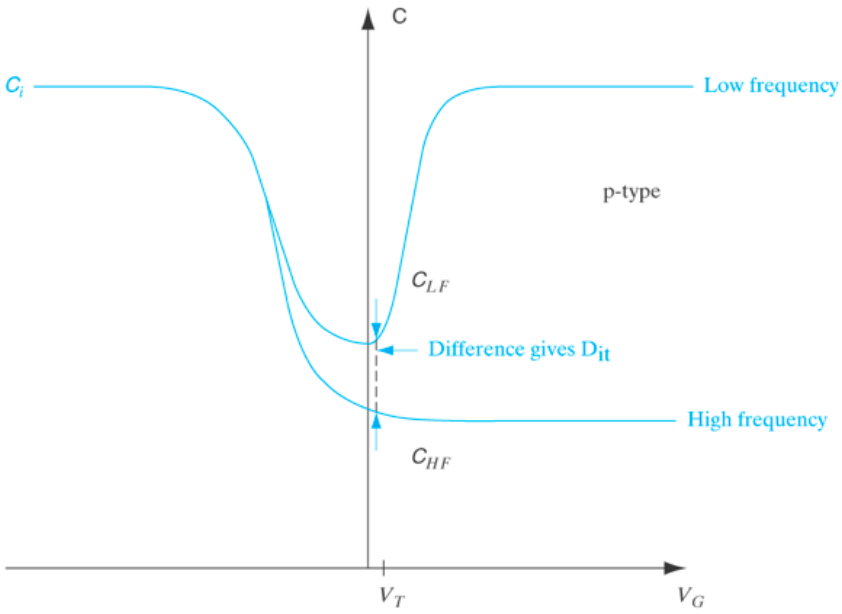






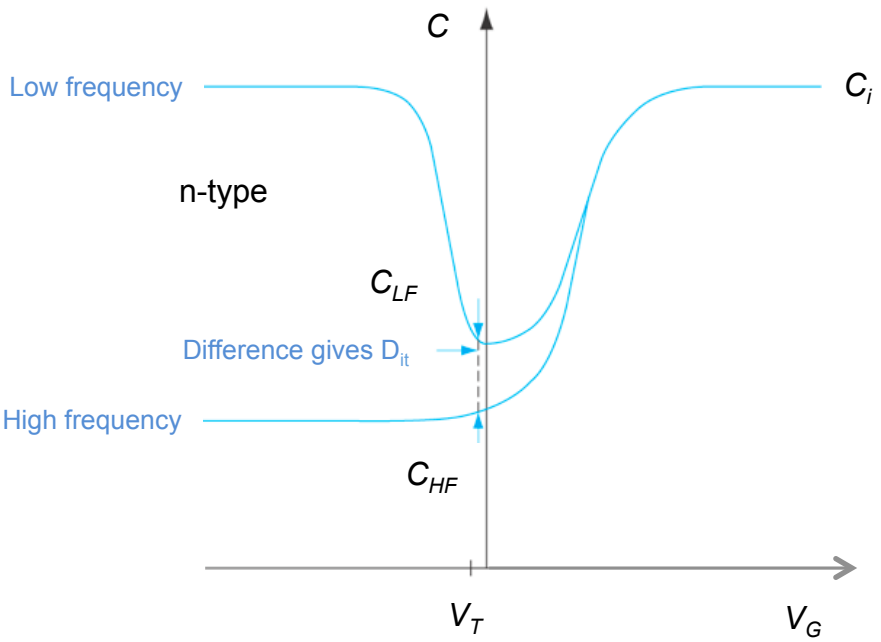
Substrate/Well Doping Type

p-Type Substrate (Well)



n-Channel Device

n-Type Substrate (Well)



p-Channel Device

Insulator Thickness and Substrate Doping Density

- The minimum capacitance C_{min} is the series combination of the insulator capacitance C_i and the minimum depletion capacitance C_{dmin} corresponding to the maximum depletion width W_m ($C_{dmin}=\varepsilon_s/W_m$)
- The expression for W_m can be solved numerically to give substrate doping density

$$C_i = \frac{\varepsilon_i}{d}$$

$d \equiv$ oxide thickness

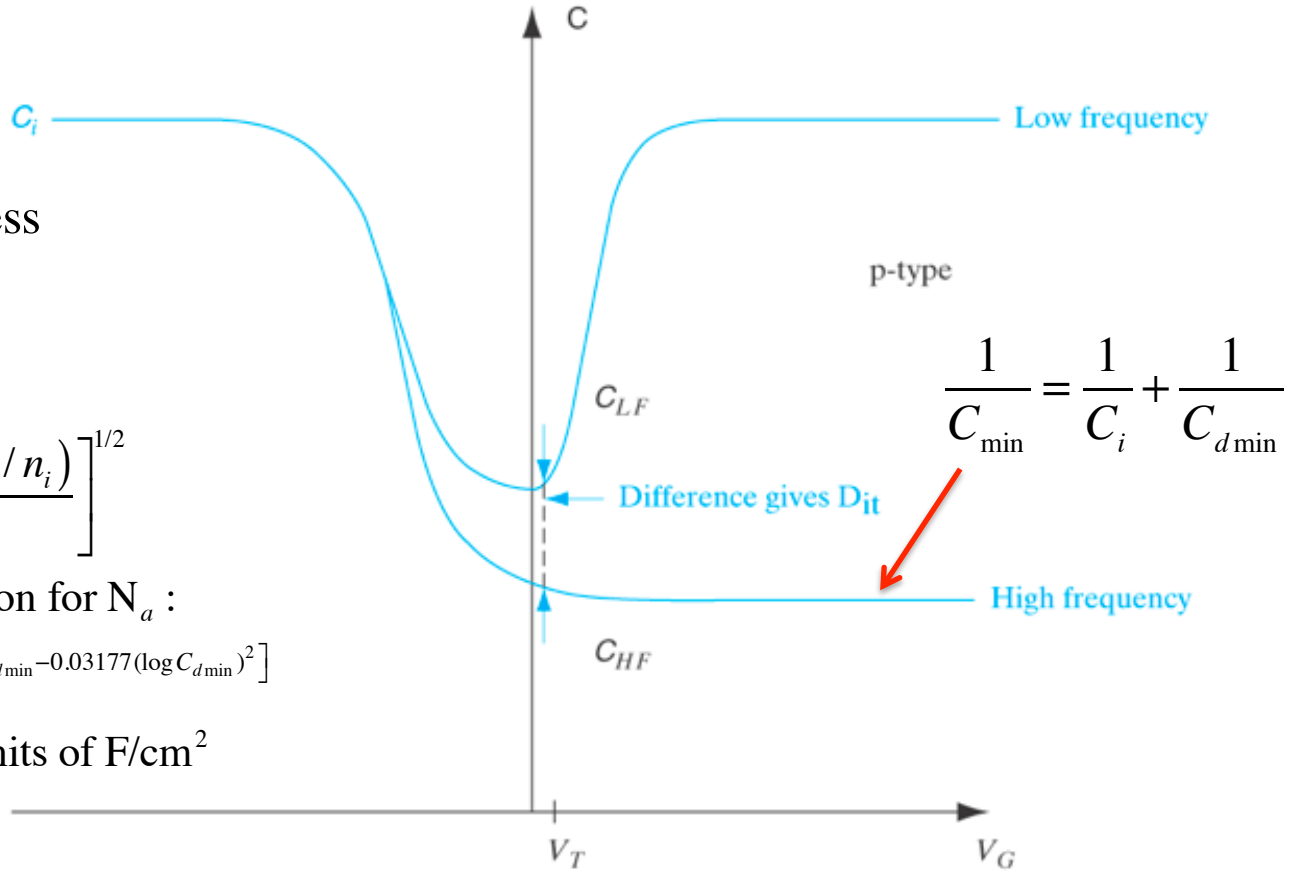
$$C_{d\min} = \frac{\varepsilon_s}{W_m}$$

$$W_m = 2\left[\frac{\varepsilon_s kT \ln\left(N_a / n_i\right)}{q^2 N_a}\right]^{1/2}$$

Approximate Solution for N_a :

$$N_a \approx 10^{\left[30.388+1.638\log C_{d\min}-0.03177(\log C_{d\min})^2\right]}$$

Where $C_{d\min}$ is in units of F/cm^2



$$\frac{1}{C_{\min}} = \frac{1}{C_i} + \frac{1}{C_{d\min}}$$

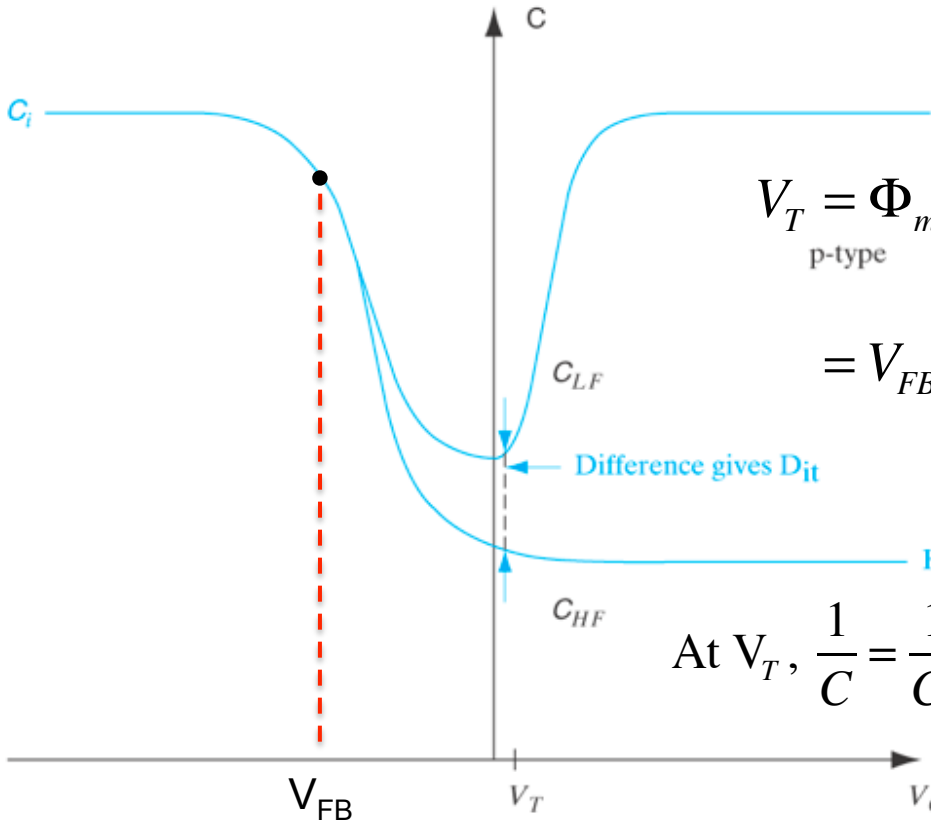
Flat Band Capacitance and Threshold Voltage

- The flat-band capacitance C_{FB} is the series combination of the Debye length capacitance and the insulator capacitance
- The measurement voltage that gives a value of C_{FB} is the flat-band voltage V_{FB}
- With this, all of the parameters have been determined that are needed to calculate V_T
- At the onset of strong inversion, the change of charge is the sum of the change in depletion charge and inversion charge – leading to the $2C_{dmin}$ term for the capacitance at V_T

$$\frac{1}{C_{FB}} = \frac{1}{C_i} + \frac{1}{C_{debye}}$$

$$C_{debye} = \frac{\varepsilon_s}{L_D}$$

$$L_D \equiv \sqrt{\frac{\varepsilon_s kT}{q^2 p_o}}$$



$$V_T = \underset{\text{p-type}}{\Phi_{ms}} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F$$

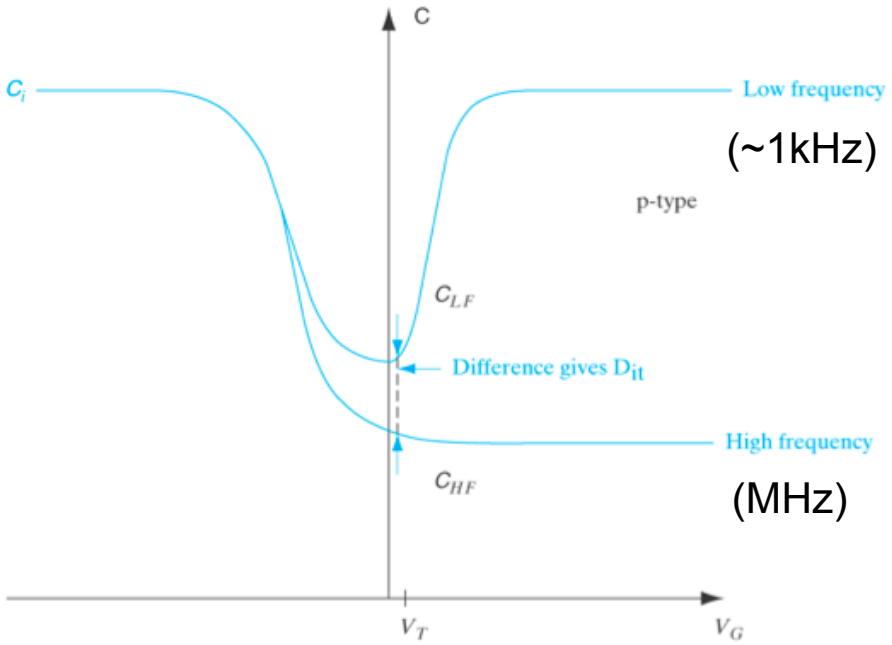
$$= V_{FB} + \frac{qN_A W_m}{C_i} + 2\frac{kT}{q}\ln\frac{N_A}{n_i}$$

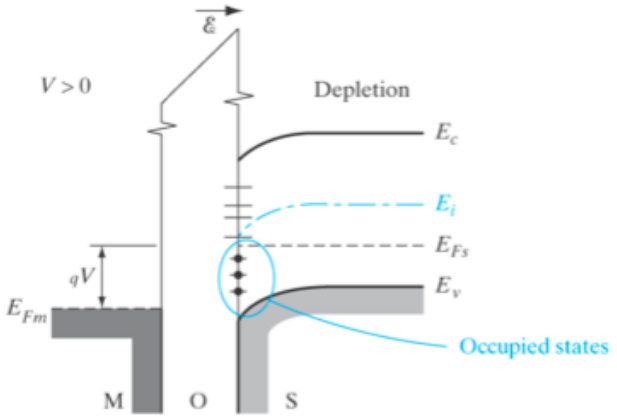
$$\text{At } V_T, \quad \frac{1}{C} = \frac{1}{C_i} + \frac{1}{2C_{d\min}}$$

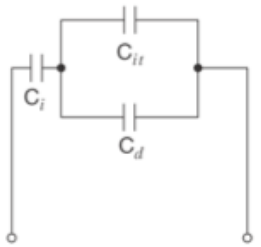
Fast Interface State Density D_{it}

- Fast interface state density D_{it} can also be determined from the C-V curve
- Variation in the surface potential moves the Fermi level, causing states to become occupied or unoccupied
- Since charge is stored or released in response to an applied potential, this is a capacitance in parallel with the channel depletion capacitance (additive relationship) and in series with the insulator capacitance
- The interface states can respond to low frequency changes but not to high frequency changes (they are fast but not "fast enough")

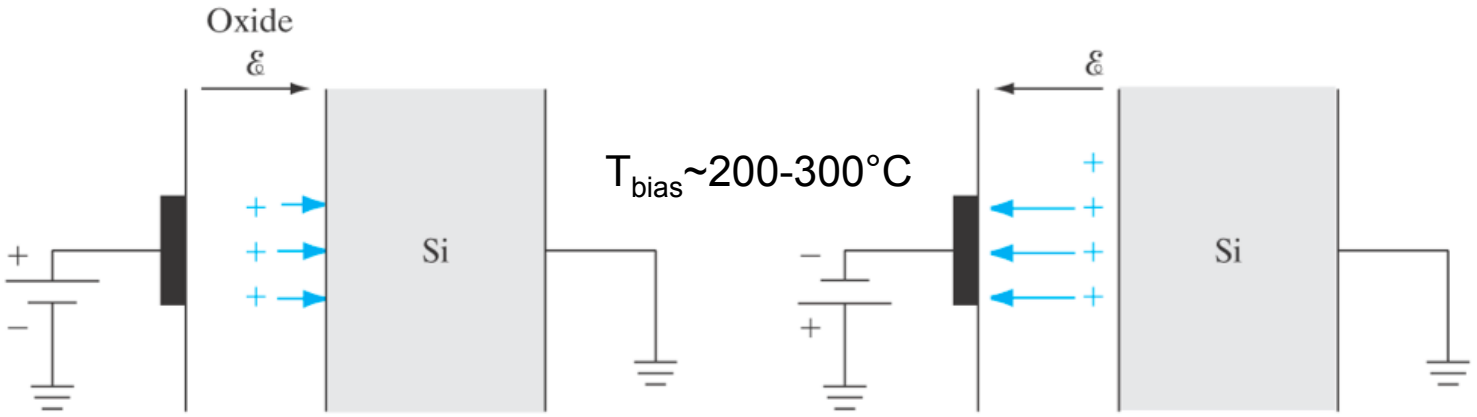
$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{LF}}{C_i - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right) cm^{-2}eV^{-1}$$



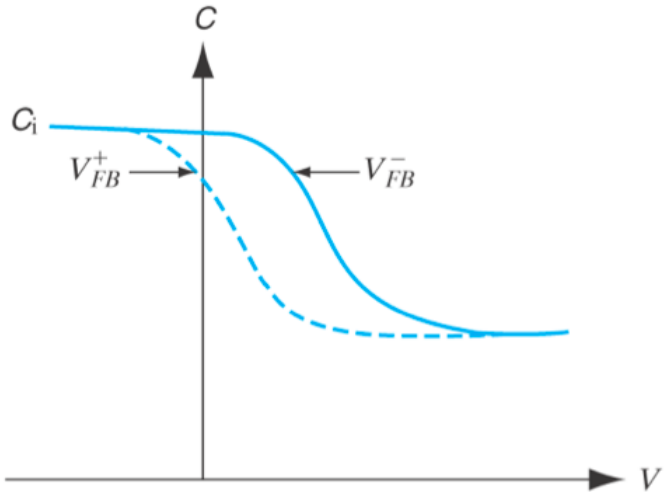




Fixed and Mobile Oxide Charge



- Fixed charge Q_f modifies the flat band and threshold voltage
- Mobile charge Q_m can be measured using an bias-temperature stress test
  - MOS capacitor heated to ~200-300° C with a bias applied to the gate (~1 MV/cm)
  - Mobile charge will move under the influence of the applied bias
- When the charge is next to the oxide-semiconductor interface, negative charge is induced in the semiconductor and a more negative gate voltage is required to achieve the flat band condition
- When the charge is next to the metal, a negative image charge is induced in the metal, and a less negative voltage needs to be applied to the gate to achieve the flat band condition



Since $V_{FB} = \Phi_{ms} - \frac{Q_i}{C_i}$, $Q_m = C_i\left(V_{FB}^- - V_{FB}^+\right)$

MOSFETs

Output Characteristics

Gate Voltage & Charge

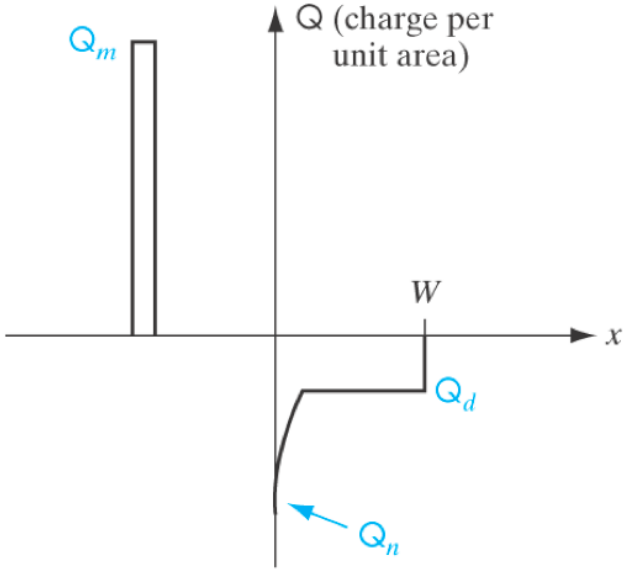
In general, the gate voltage can be broken down into the following:

$$V_G = \left(\Phi_{ms} - \frac{Q_i}{C_i} \right) - \frac{Q_s}{C_i} + \phi_s = V_{FB} - \frac{Q_s}{C_i} + \phi_s$$

Potential Across Semiconductor

Voltage to Achieve Flat Band Condition

Voltage Due to Charge Across Insulator



Q_s ← induced charge

$Q_s = Q_d + Q_n$

Q_d ← Fixed charge (depletion region)

Q_n ← Mobile charge (channel)

ϕ_s ← potential across semiconductor (band bending)

$$V_G = V_{FB} - \frac{(Q_d + Q_n)}{C_i} + \phi_s \quad \rightarrow \quad Q_n = -C_i \left[V_G - \left(V_{FB} + \phi_s - \frac{Q_d}{C_i} \right) \right]$$

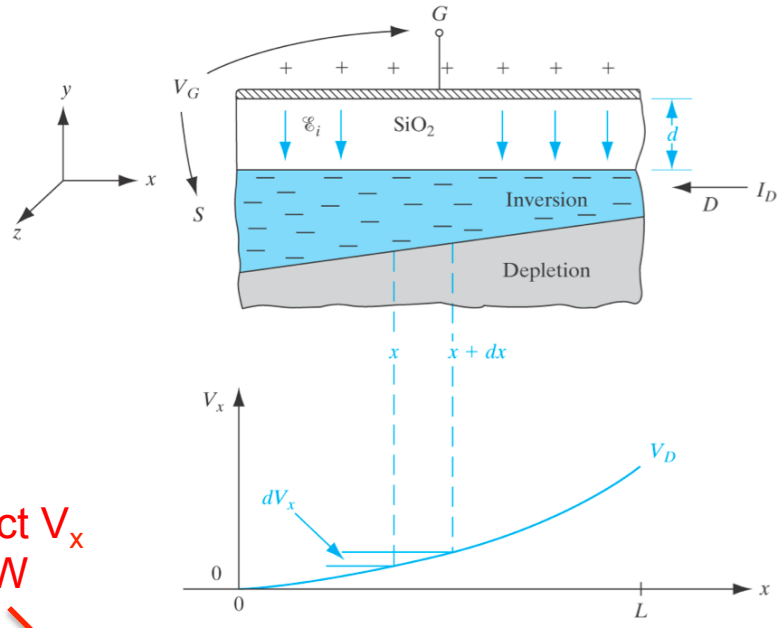
Above Threshold ($V_G > V_T$): $Q_n = -C_i \left[V_G - (V_T) \right]$ ← Does not hold at or below threshold

Charge With Applied Drain Voltage

With a voltage V_D applied to the drain and the source grounded:

1) There is a voltage rise along the channel from the source to drain with any point along the channel x having a voltage $V_x(x)$
2) The potential $\phi_s(x)$ along the channel is:

$$\phi_s(x) = 2\phi_F + V_x(x)$$



Therefore:

Neglect V_x in W

$$Q_n(x) = -C_i\left[V_G - V_{FB} - 2\phi_F - V_x(x) - \frac{1}{C_i}\sqrt{2q\varepsilon_s N_a\left(2\phi_F + V_x\right)}\right]$$

x

Since $V_T = V_{FB} - \frac{Q_d}{C_i} + 2\phi_F$ and neglecting the variation in Q_d :

$$Q_n(x) = -C_i\left(V_G - V_T - V_x(x)\right)$$

Mobile Charge in Channel at "x" (low V_D)

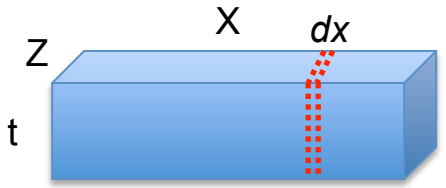
Note:

$$Q_d = -qN_a^- W(x)$$

$$W(x) = \left[\frac{2\varepsilon_s(2\varphi_F + V_x)}{qN_a}\right]^{1/2}$$

Output Characteristics: I_D for Small V_D

Recall the expression for conductance: $G = \frac{wt\sigma}{X} = \frac{wtqn\mu_n}{X}$



The conductance of the differential element dx is then:

$G(x) = \frac{\bar{\mu}_n Z Q_n(x)}{dx}$ where Z is the channel width and $\bar{\mu}_n$ is the "surface mobility"

The current at "x" is $I = G(x)V$ therefore: $I_D = \frac{\bar{\mu}_n |Q_n(x)| Z}{dx} dV_x$ and

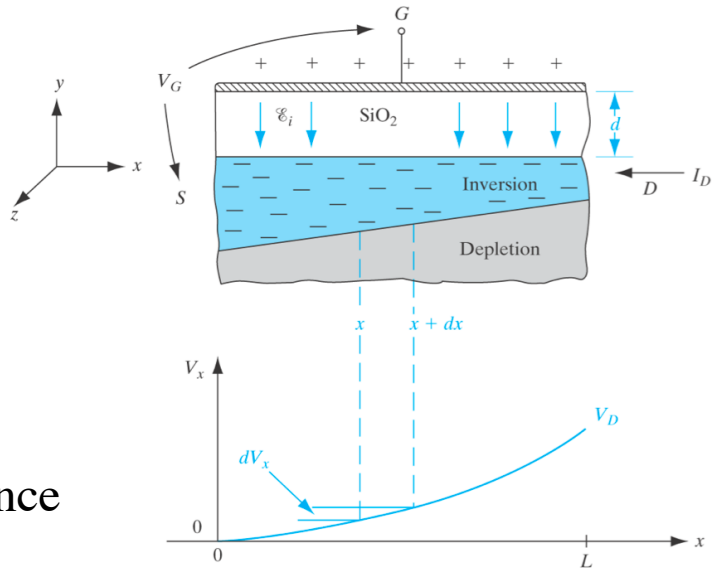
$I_D dx = \bar{\mu}_n |Q_n(x)| Z dV_x$ $\Leftarrow$ Integrating this from source to drain:

$$\int_0^L I_D\, dx = I_D \int_0^L dx = \bar{\mu}_n Z C_i \int_0^{V_D} (V_G - V_T - V_x)\, dV_x$$

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

Small V_D: Neglect Q_n Variation

$\frac{\bar{\mu}_n Z C_i}{L} = k_n$ $\Leftarrow$ Determines conductance and transconductance



Output Characteristics: General Case

For larger drain currents, the variation in $Q_n(x)$ cannot be neglected, and the full expression is integrated:

$$\int_0^L I_D\,dx = \bar{\mu}_n Z C_i \int_0^{V_D}\left[V_G - V_{FB} - 2\phi_F - V_x - \frac{1}{C_i}\sqrt{2q\varepsilon_s N_a\left(2\phi_F + V_x\right)}\right]dV_x \text{ so:}$$

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left\{\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D\right)V_D - \frac{2}{3}\frac{\sqrt{2q\varepsilon_s N_a}}{C_i}\left[\left(V_D + 2\phi_F\right)^{3/2} - \left(2\phi_F\right)^{3/2}\right]\right\}$$

Low Drain Bias:

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

General Bias Condition:

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left\{\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D\right)V_D - \frac{2}{3}\frac{\sqrt{2q\varepsilon_s N_a}}{C_i}\left[\left(V_D + 2\phi_F\right)^{3/2} - \left(2\phi_F\right)^{3/2}\right]\right\}$$

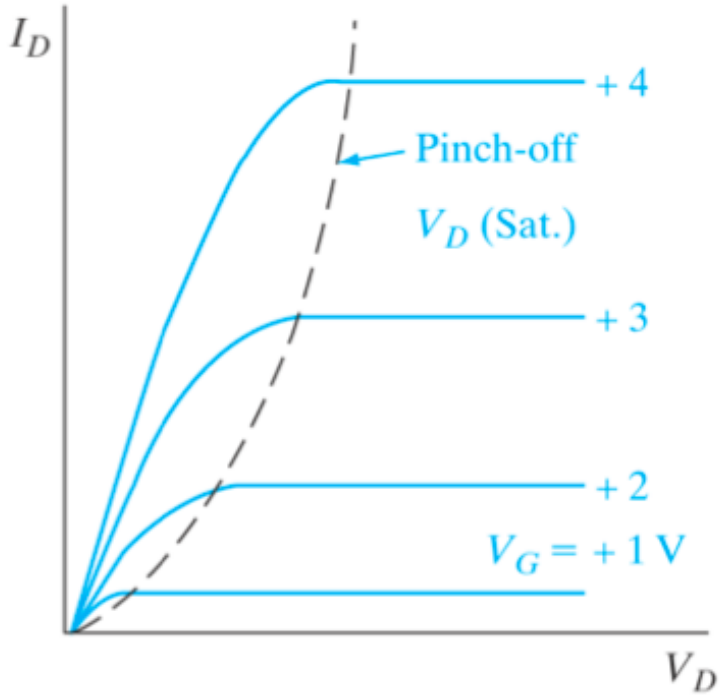
Above $V_D \simeq V_G - V_T$, use $V_D \simeq V_D(sat.) = V_G - V_T$

Output Characteristics: Conductance

Under low drain voltage and $V_G > V_T$, the channel resembles a linear resistor:

$$g = \frac{\partial I_D}{\partial V_D} = \frac{\bar{\mu}_n Z C_i}{L} \frac{\partial}{\partial V_D}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

$$= \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T) - V_D\right] \simeq \frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T) \text{ for } V_D \ll V_G - V_T$$



As V_D is increased, ΔV between the oxide and semiconductor near the drain decreases. When ΔV becomes lower than V_T, the channel becomes pinched off:

$$V_D(sat.) \simeq V_G - V_T$$

The current then becomes constant after entering saturation:

$$I_D(sat.) \simeq \frac{1}{2}\frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)^2 = \frac{1}{2}\frac{\bar{\mu}_n Z C_i}{L}V_D^2(sat.)$$

The **transconductance** at saturation is:

$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G} \simeq \frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)$$

For p-channel devices➔ V_G V_D V_T and I_D are negative

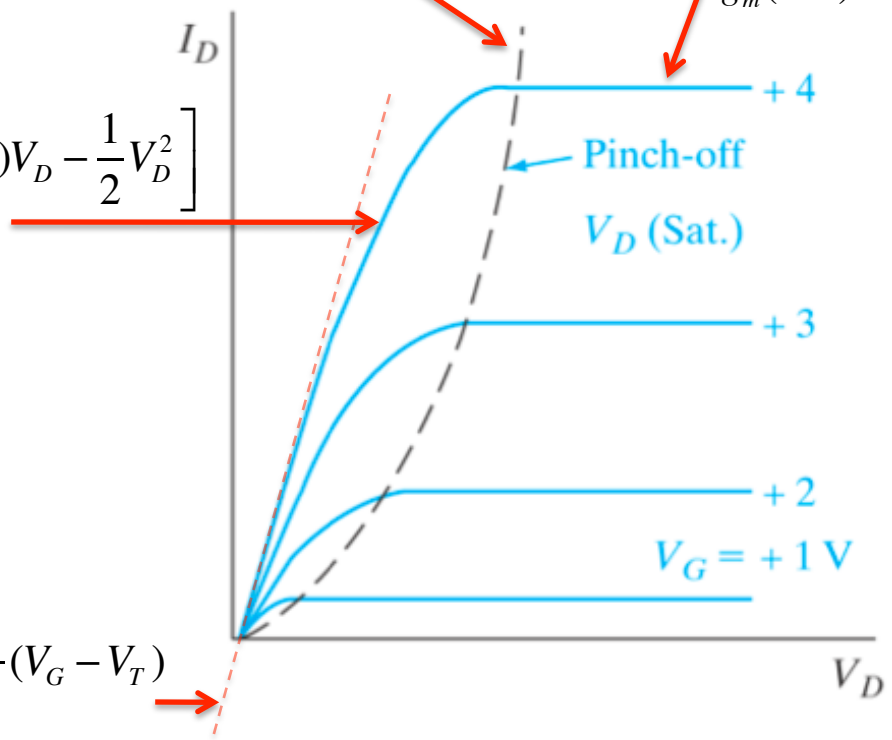
Summary: Output Characteristics

$$I_D(sat.) \simeq \frac{1}{2}\frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)^2 = \frac{1}{2}\frac{\bar{\mu}_n Z C_i}{L}V_D^2(sat.)$$

$$V_D(sat.) \simeq V_G - V_T$$

$$g_m(sat.) \simeq \frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)$$

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$



$$g = \frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)$$

General Bias Condition:

$$I_D = \frac{\bar{\mu}_n Z C_i}{L}\left\{\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D\right)V_D - \frac{2}{3}\frac{\sqrt{2q\varepsilon_s N_a}}{C_i}\left[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}\right]\right\}$$

Characteristics for n-channel and p-channel MOSFETs

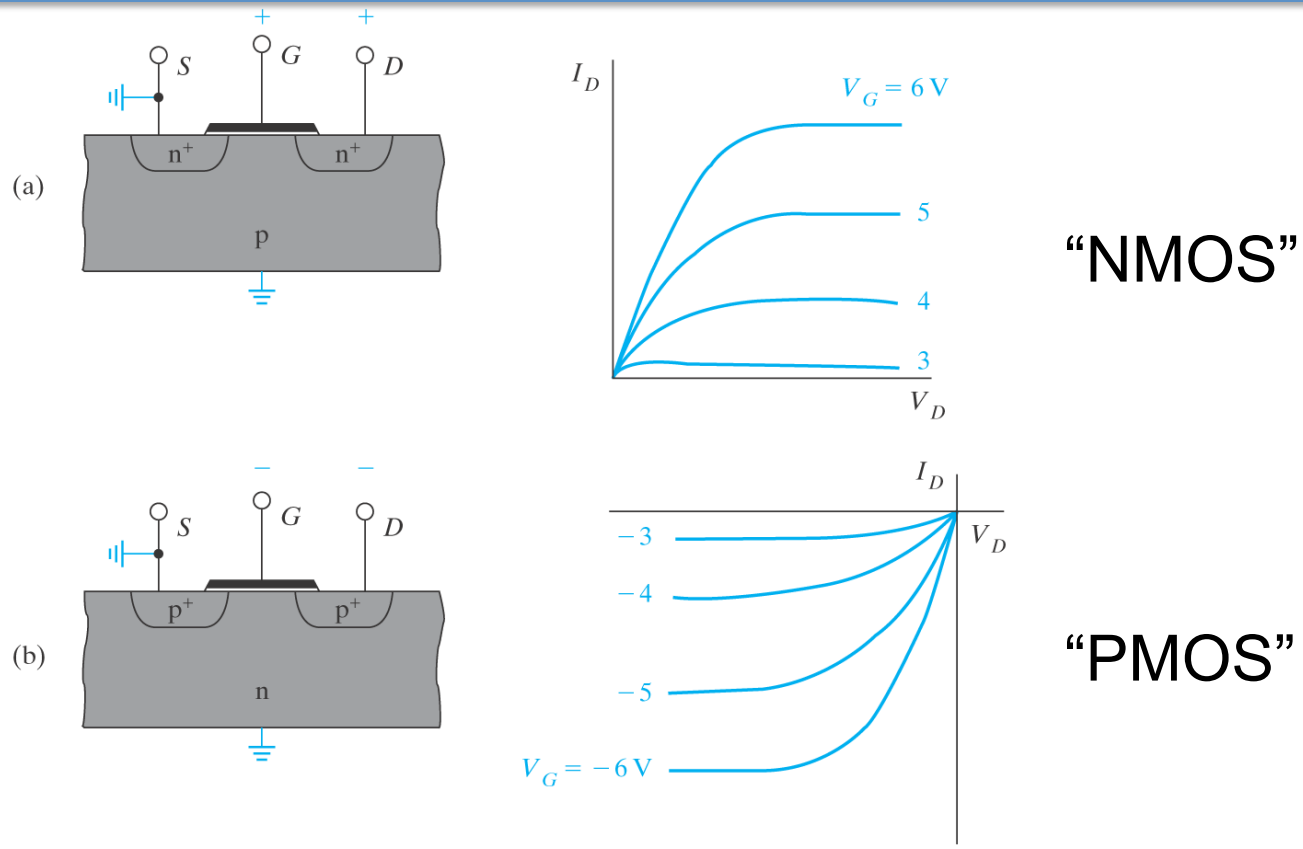
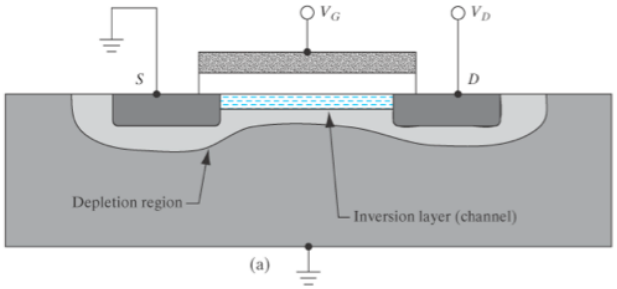


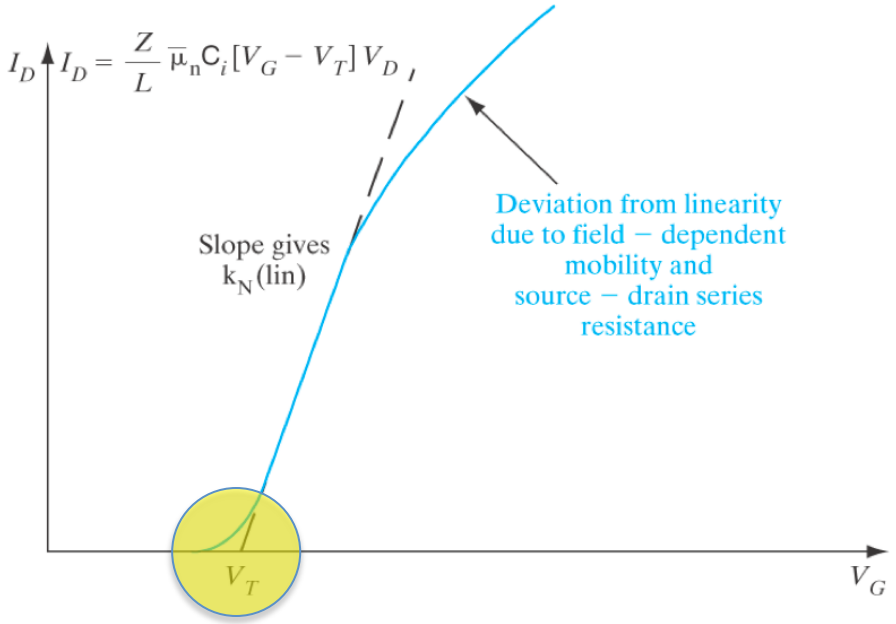
Figure 6.27

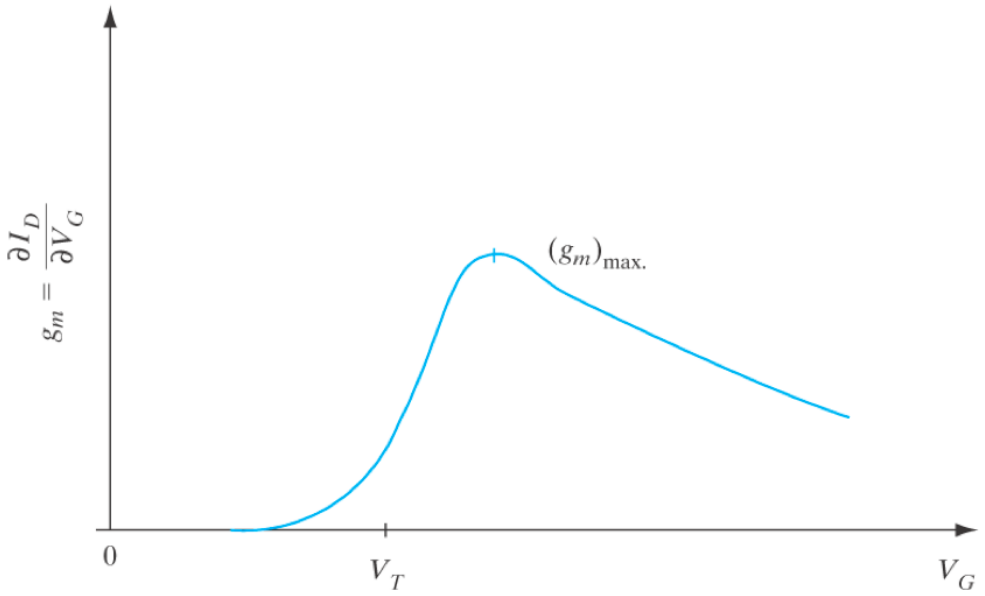
Drain current–voltage characteristics for enhancement transistors: (a) for n-channel V_D, V_G, V_T, and I_D are positive; (b) for p-channel all these quantities are negative.

Transfer Characteristics

Transfer Characteristic: Small V_D

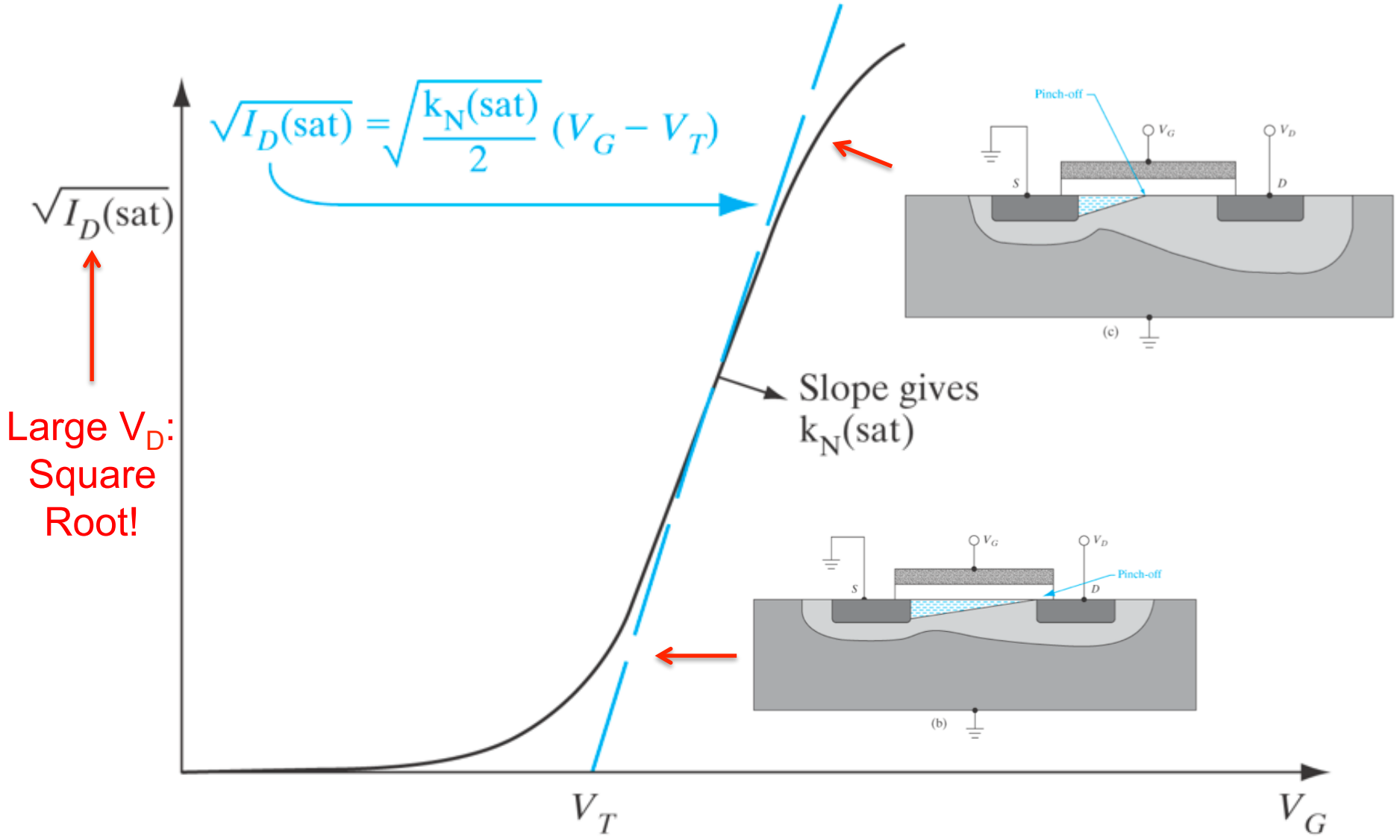






$Q_n = -C_i [V_G - V_T]$ is not valid near $V_G = V_T$

Transfer Characteristic: Large V_D



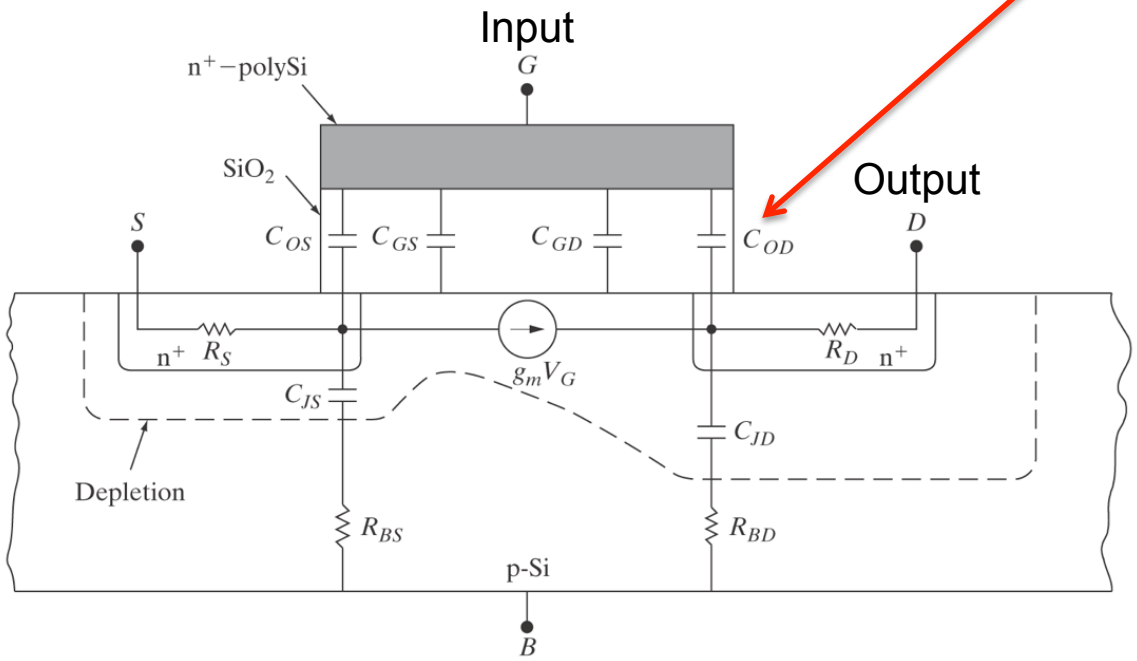
Small Signal Analysis

MOSFET Equivalent Circuit

Gate Insulator Capacitance

Contributions to C_i:

- C_{OS}: Gate to source overlap capacitance
- C_{GS}: Gate to source distributed capacitance
- C_{OD}: Gate to drain overlap capacitance ("Miller overlap capacitance") – potential source of feedback
  - Minimize with self-aligned gate, measured with V_G=0
- C_{GD}: Gate to drain distributed capacitance



Other Components

Other Components:

- C_{JS}: Source p-n junction capacitance
- C_{JD}: Drain p-n junction capacitance
- R_S: Source parasitic series resistance
- R_D: Drain parasitic series resistance
- R_{BS}, R_{BD}: Source and Drain parasitic bulk resistance
- $g_m V_G$: Voltage-controlled current source

$$\frac{V_D}{I_D} = R_{Ch} + R_{SD} = \frac{L - \Delta L}{Z - \Delta Z} \frac{1}{\bar{\mu}_n C_i (V_G - V_T)} + R_{SD}$$

Effective Channel Width:

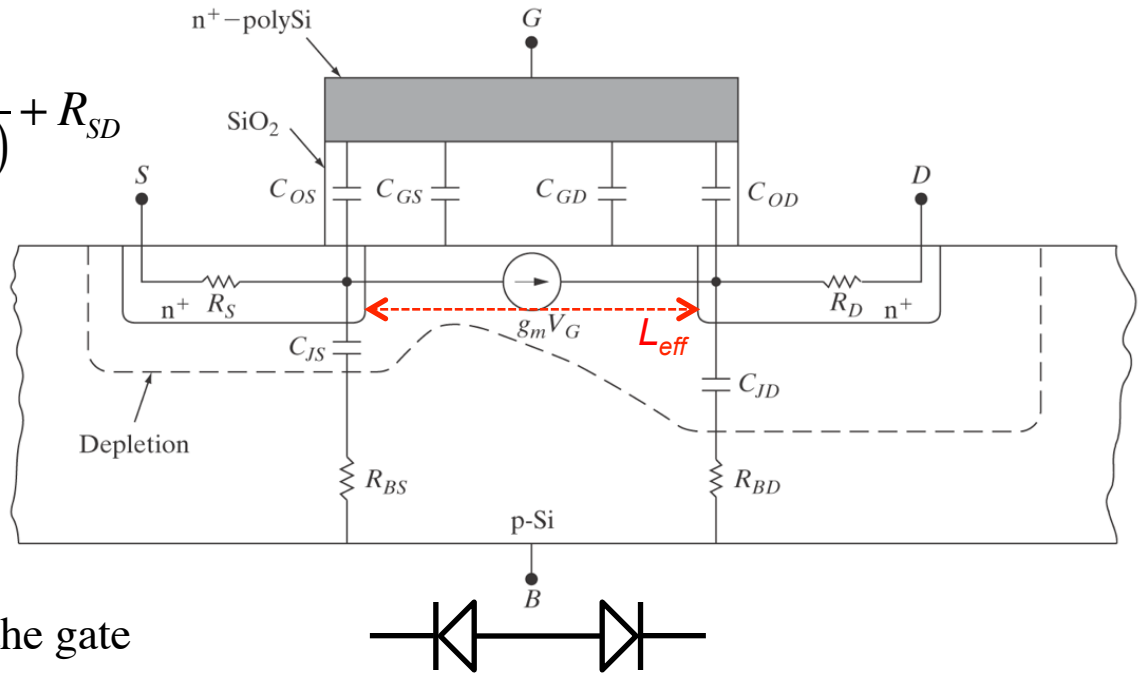
$Z_{eff} = Z - \Delta Z$

ΔZ is the side spread under the gate

Effective Channel Length:

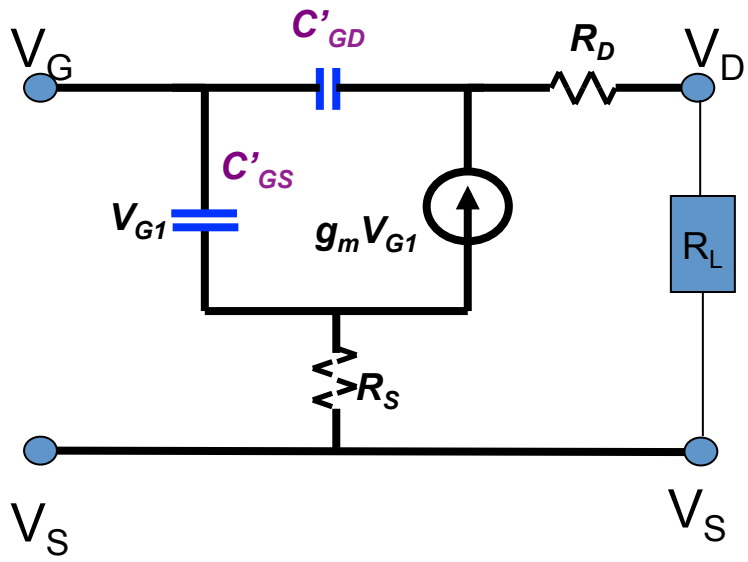
$L_{eff} = L - \Delta L_R$

ΔL_R is the spread of source/drain under the gate



Comments: Simplified Model

- The MOSFET acts like a voltage-controlled current source
- The gate-drain capacitance acts as a feedback path
- The source and drain resistances induce ohmic losses and reduce drain current for a given drain voltage
  - Since a given gate voltage will then result in a lower drain current, the transconductance is reduced



Neglecting R_S and R_D :

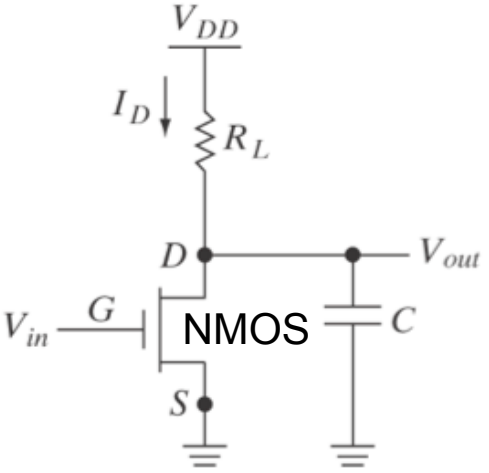
$$\frac{V_{out}}{V_{in}} = \frac{g_m V_G \bullet R_L}{V_G} = g_m R_L$$

Logic Devices

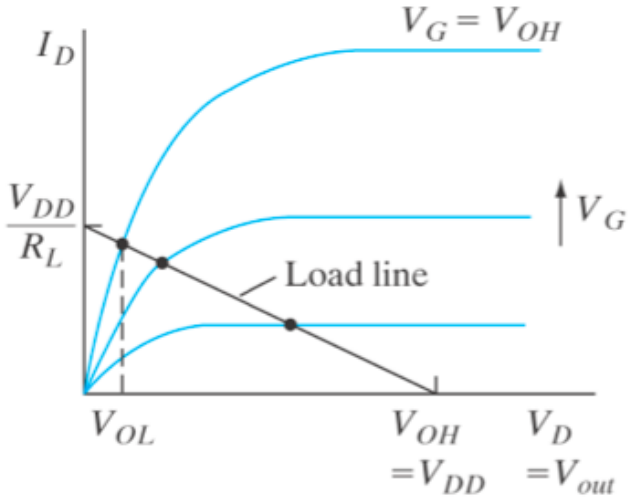
Inverter

MOSFET Inverter (n-Channel)

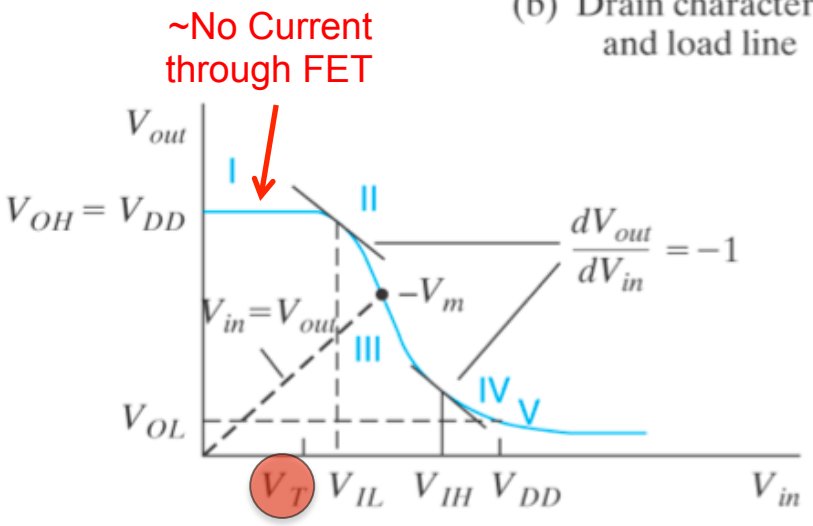
- Voltage Transfer Characteristic (VTC): output voltage as a function of input bias
- V_{OH}: logic high level
- V_{OL}: logic low level
- V_{IL} and V_{IH}: unity gain points (between V_{IL} and V_{IH} the input is amplified)
- V_m: logic threshold, point where output equals input
- Load line used to create VTC (resistor current equals FET current)



(a) Inverter



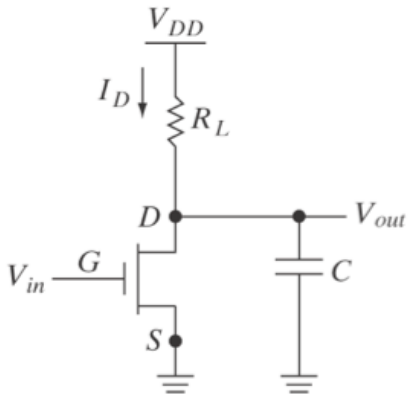
(b) Drain characteristics and load line



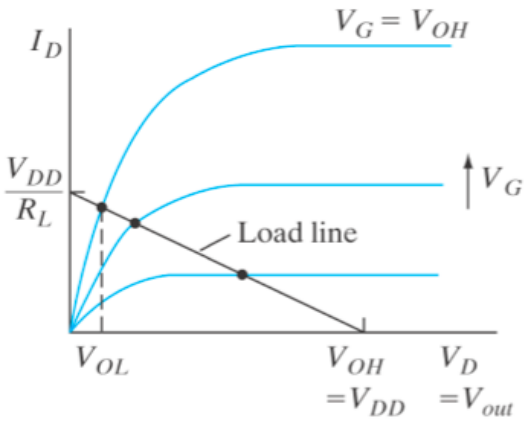
(c) Voltage transfer characteristic

NMOS: n-channel

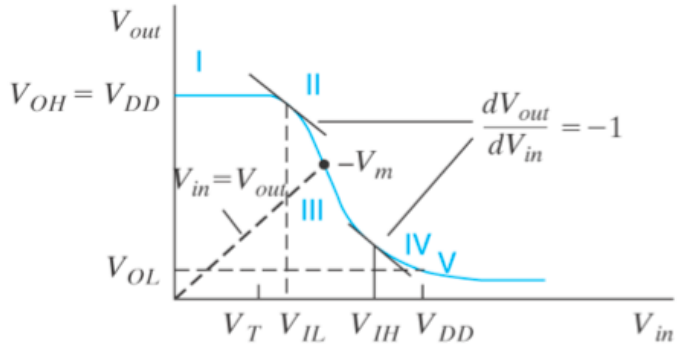
MOSFET Inverter (n-Channel)



(a) Inverter



(b) Drain characteristics and load line



(c) Voltage transfer characteristic

- Gate voltage low – no current flow, no voltage drop across R_L and V_{out} is high
- Gate voltage high – current flow, large voltage drop across R_L and V_{out} is low

MOSFET Drain Current (linear region):

$$I_D = k\left[V_G - V_T - \frac{V_D}{2}\right]V_D = k\left[V_{DD} - V_T - \frac{V_{OL}}{2}\right]V_{OL}$$

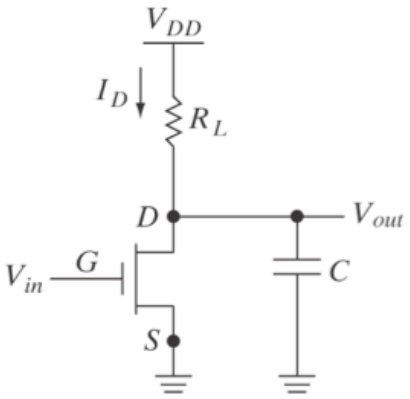
MOSFET Drain Current (saturation region):

$$I_D = \frac{1}{2}k\left[V_G - V_T\right]^2$$

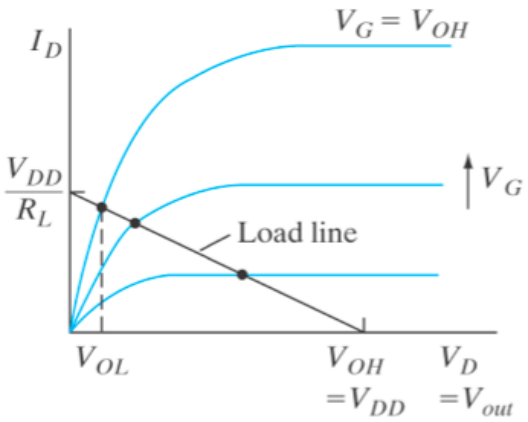
Resistor Current (equal to MOSFET current):

$$I_R = I_D = \frac{V_{DD} - V_{OL}}{R_L}$$

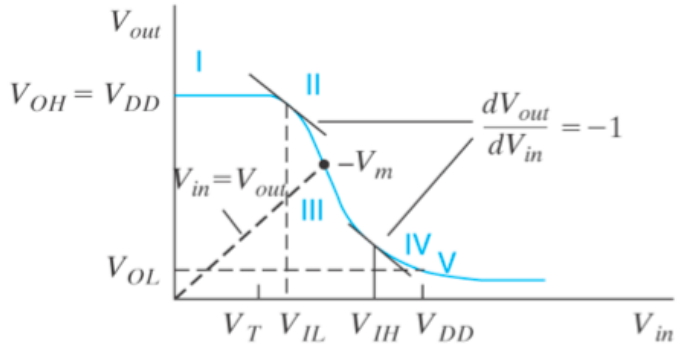
MOSFET Inverter (n-Channel)



(a) Inverter



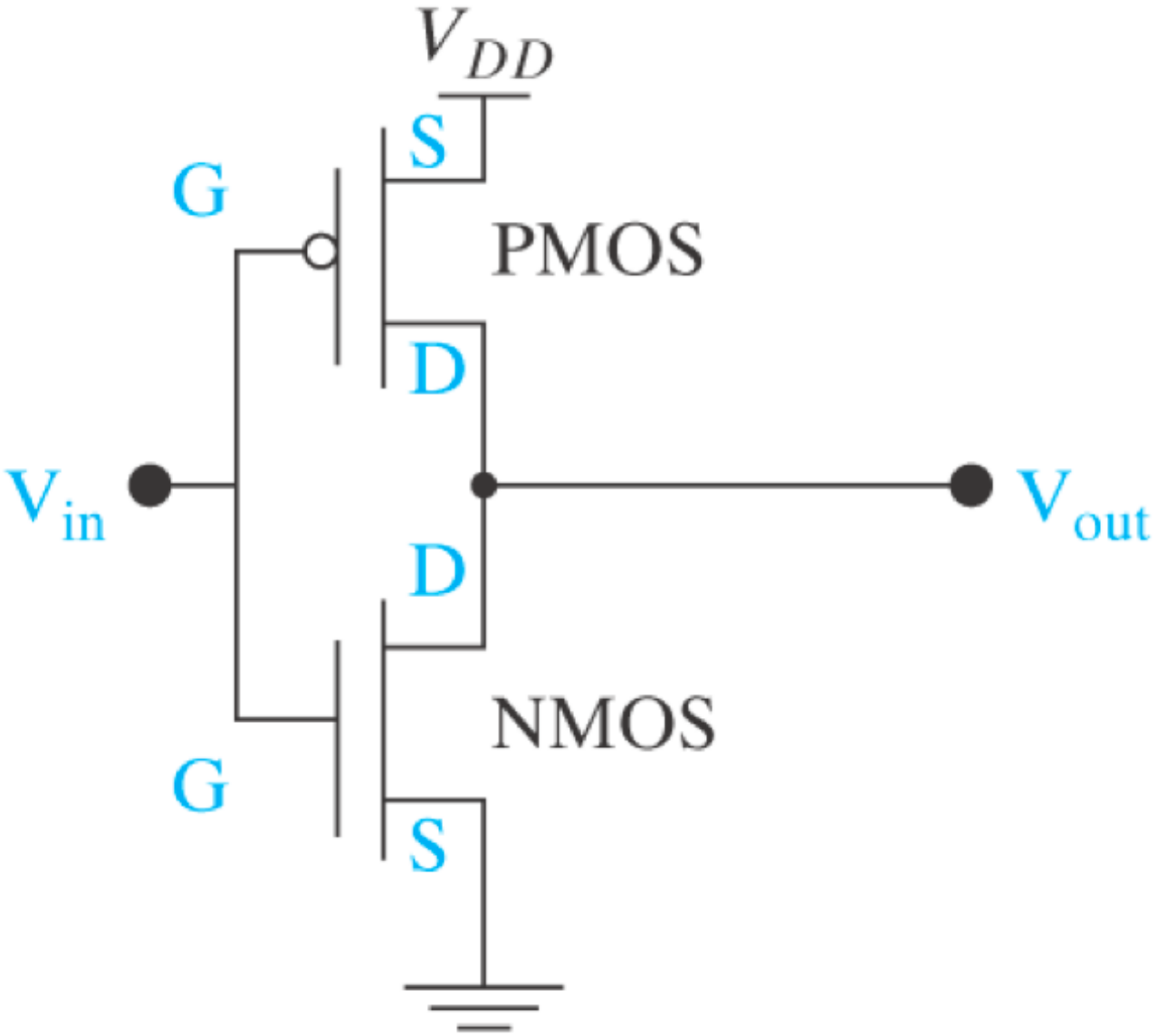
(b) Drain characteristics and load line



(c) Voltage transfer characteristic

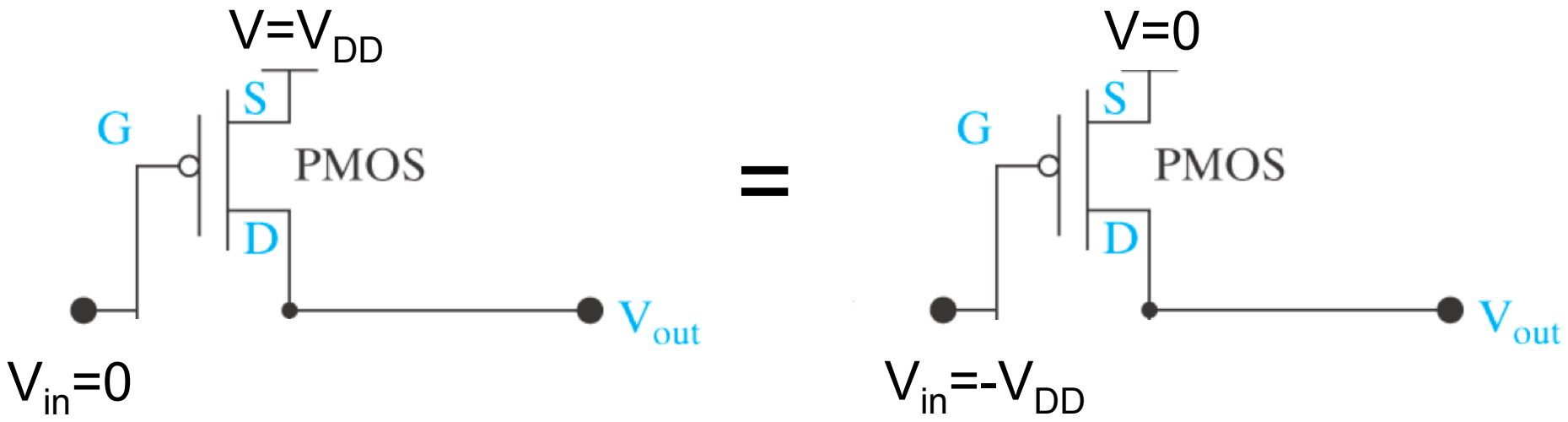
- Ideally:
  - Region III should be as steep as possible (high gain)
  - V_m should be close to $V_{DD}/2$
- Noise Immunity (Noise Margin): How much variation in input voltage can be tolerated while still having correct output logic level
- Problems with resistive inverter:
  - Power dissipation in resistor
  - V_{OL} is not zero
- Solution: CMOS

CMOS Inverter

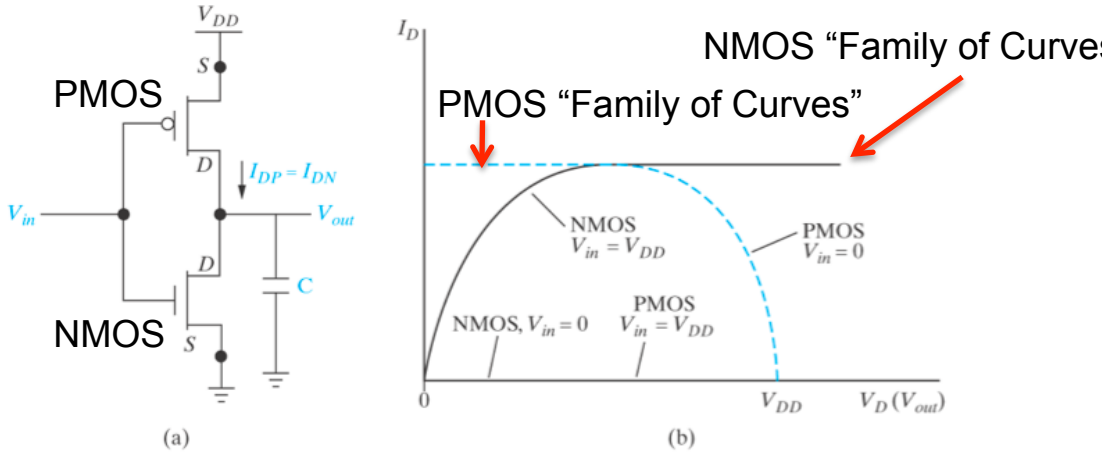


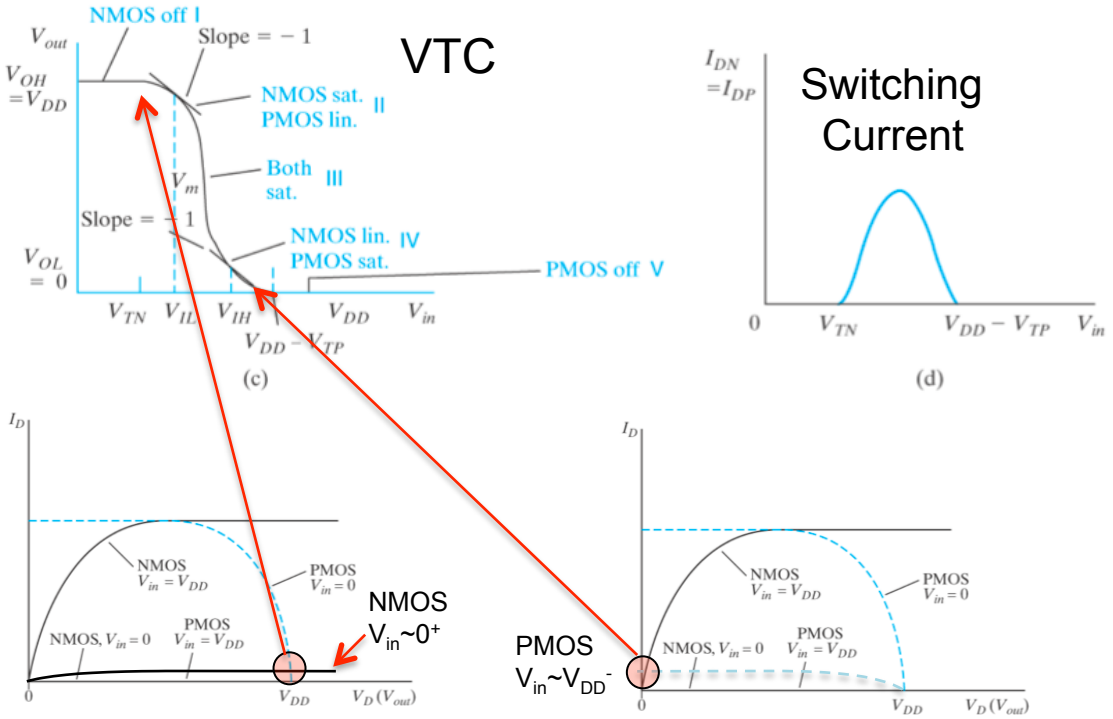
PMOS Biasing Comment

From a PMOS channel conductance perspective:



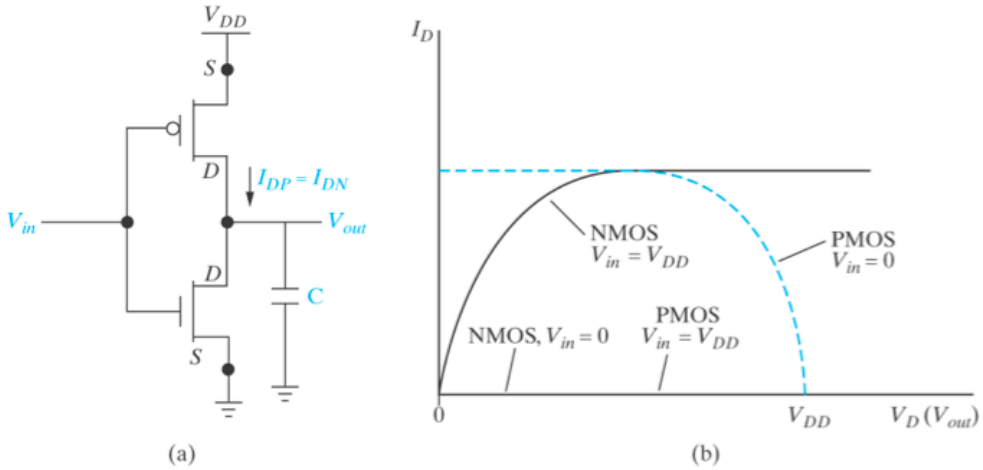
CMOS: Description

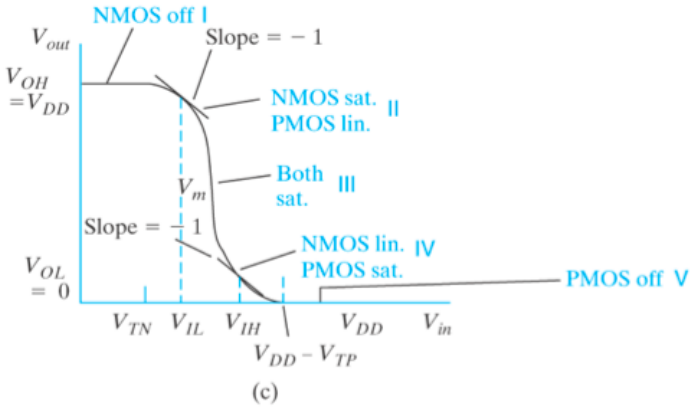


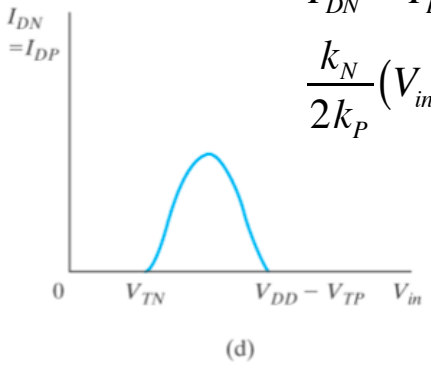


- Overall circuit voltage transfer characteristic determined by solving the set of equations where the n-channel MOSFET (NMOSFET) current equal to the p-channel MOSFET (PMOSFET) current
- The I_D relationship used to determine the operating characteristic is chosen based upon whether the FETs are in the linear or saturation operating regions

CMOS Current-Voltage Characteristic







Region II Current Calculation

NMOSFET Drain Current (Saturation):

$$I_{DN} = \frac{k_N}{2}\left(V_{in} - V_{TN}\right)^2$$

PMOSFET Drain Current (Linear):

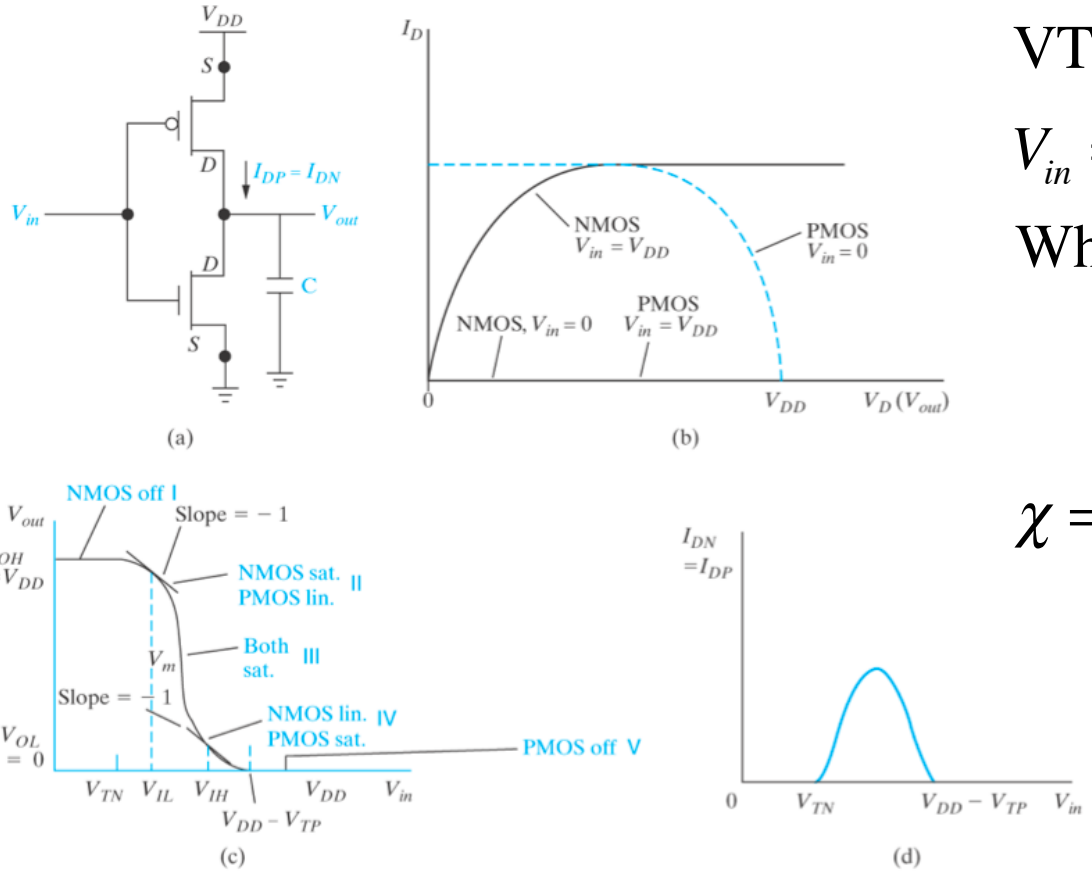
$$I_{DP} = k_P\left[\left(V_{DD} - V_{in}\right) + V_{TP} - \frac{\left(V_{DD} - V_{out}\right)}{2}\right]\left(V_{DD} - V_{out}\right)$$

To determine operation point (VTC):

$I_{DN} = I_{DP}$ So:

$$\frac{k_N}{2k_P}\left(V_{in} - V_{TN}\right)^2 = \left[\frac{V_{DD}}{2} - V_{in} + V_{TP} + \frac{V_{out}}{2}\right]\left(V_{DD} - V_{out}\right)$$

CMOS Transition Voltage



VTC Transition Region Occurs At:

$$V_{in} = \left(V_{DD} + \chi V_{TN} + V_{TP}\right) / \left(1 + \chi\right)$$

Where:

$$\chi = \left(\frac{k_N}{k_P}\right)^{\frac{1}{2}} = \frac{\left[\bar{\mu}_n C_i \left(\frac{Z}{L}\right)_N\right]^{\frac{1}{2}}}{\left[\bar{\mu}_p C_i \left(\frac{Z}{L}\right)_P\right]^{\frac{1}{2}}}$$

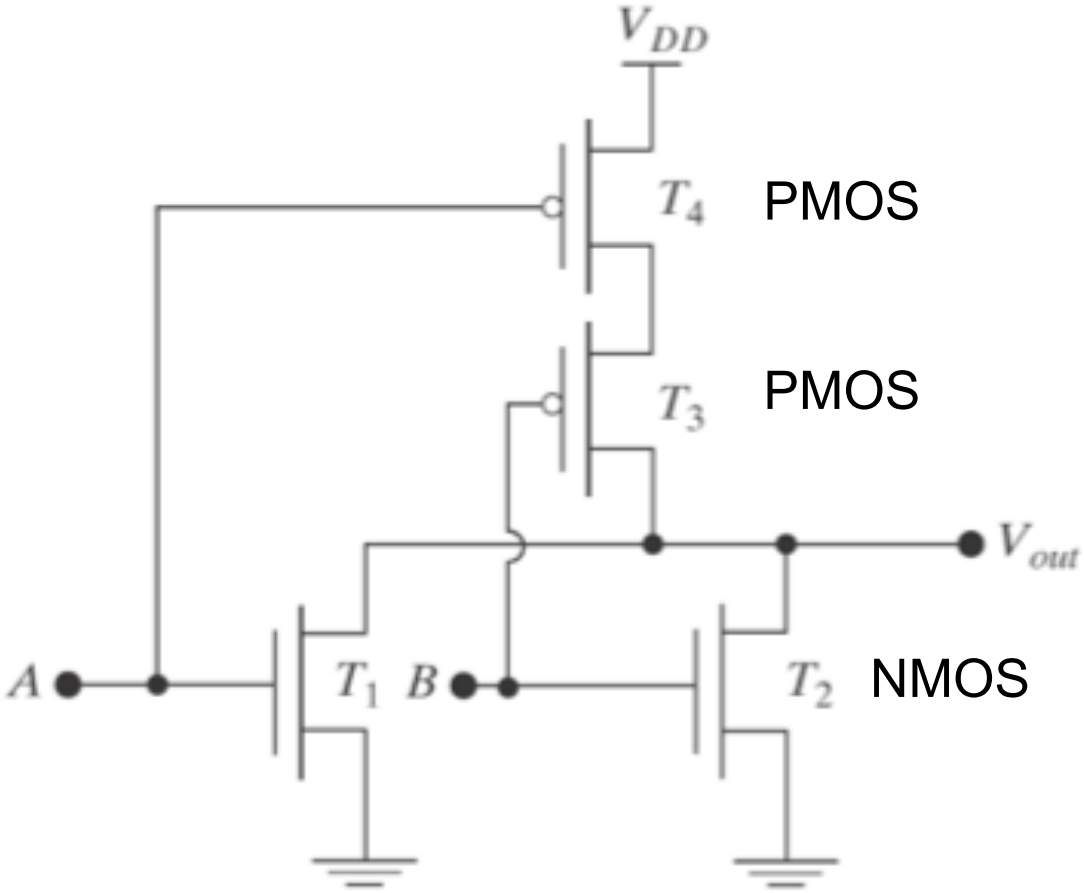
Want to have $V_{in} \sim \frac{V_{DD}}{2}$

To get $V_{in}=V_{DD}/2$ at the switching point, design device such that $V_{TN}=-V_{TP}$ and $\chi=-1$:
For Si, with an electron mobility roughly 2X hole mobility, $(Z/L)_P=2(Z/L)_N$

Logic Devices

NOR, NAND

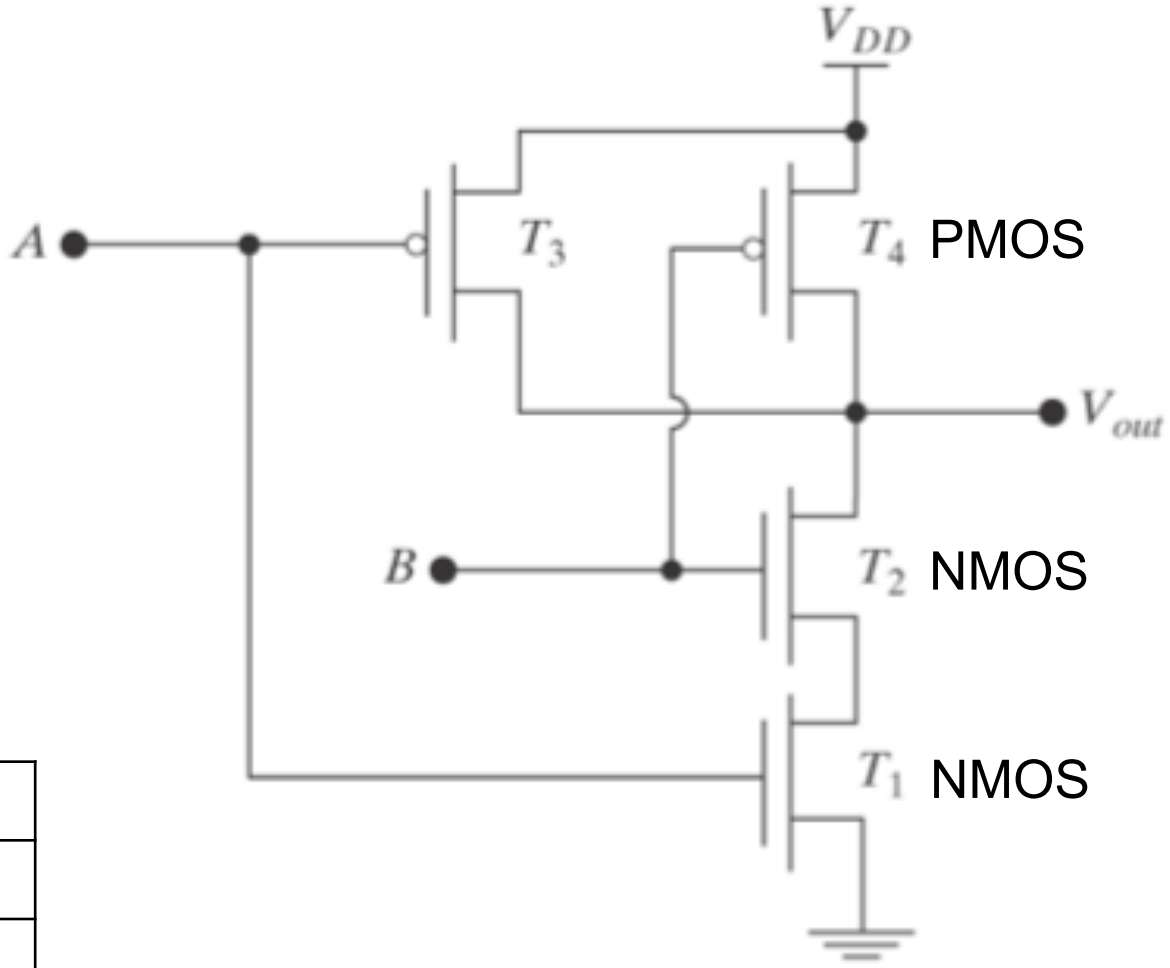
CMOS NOR



A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

PMOS in series (slower)

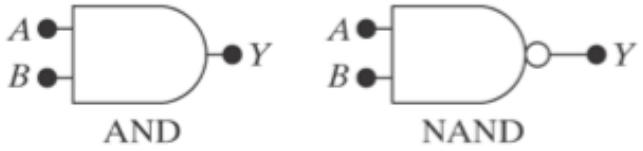
CMOS NAND



A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

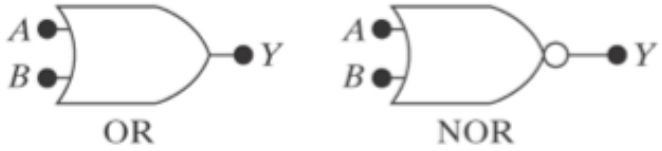
NMOS in series (faster)

Truth Tables



Input		Output Y	
A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(a)



Input		Output Y	
A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(b)

Input		Output Y
A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

Power Dissipation

The input capacitance of the inverter is the parallel combination of the NMOSFET and PMOSFET:

$$C_{inv} = C_i\left\{(ZL)_N + (ZL)_P\right\}$$

Multiplying this term by the fan-out gives a total load capacitance of "C"

The energy expended in charging "C" is given by integrating the product of the time-dependent voltage and the time-dependent current:

$$E_C = \int i_p(t)\left[V_{DD} - v(t)\right]dt = V_{DD}\int i_p(t)\,dt - \int i_p(t)v(t)\,dt$$

but $i_p(t) = C\dfrac{dv(t)}{dt}$ so:

$$E_C = V_{DD}\int C\frac{dv(t)}{dt}dt - \int Cv(t)\frac{dv(t)}{dt}dt = CV_{DD}\int_0^{V_{DD}} dv - C\int_0^{V_{DD}} v\,dv = CV_{DD}^2 - \frac{1}{2}CV_{DD}^2 = \frac{1}{2}CV_{DD}^2$$

During a discharge cycle:

$$E_d = \int i_n(t)v(t)\,dt = -\int_{V_{DD}}^{0} Cv\,dv = \frac{1}{2}CV_{DD}^2$$

For a charge/discharge frequency "*f*":

$$P = CV_{DD}^2 f$$

Switching Delays

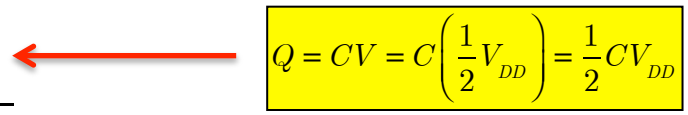
The propagation delay time t_P is a metric for the switching speed of the gate.

$t_{PHL} \equiv$ the time for the output to transition from V_{OH} to $V_{OH}/2$

$t_{PLH} \equiv$ the time for the output to transition from V_{OL} to $V_{OH}/2$

The time needed to reach $V_{OH}/2$ is found by dividing charge stored in the capacitor by the charge or discharge current. Since the transistor providing the current is in saturation, and $I(sat).= \frac{k}{2}(V_{DD}-V_T)^2$:

$$t_{PHL} = \frac{\frac{1}{2}CV_{DD}}{I_{DN}} = \frac{\frac{1}{2}CV_{DD}}{\frac{k_N}{2}(V_{DD}-V_{TN})^2}$$



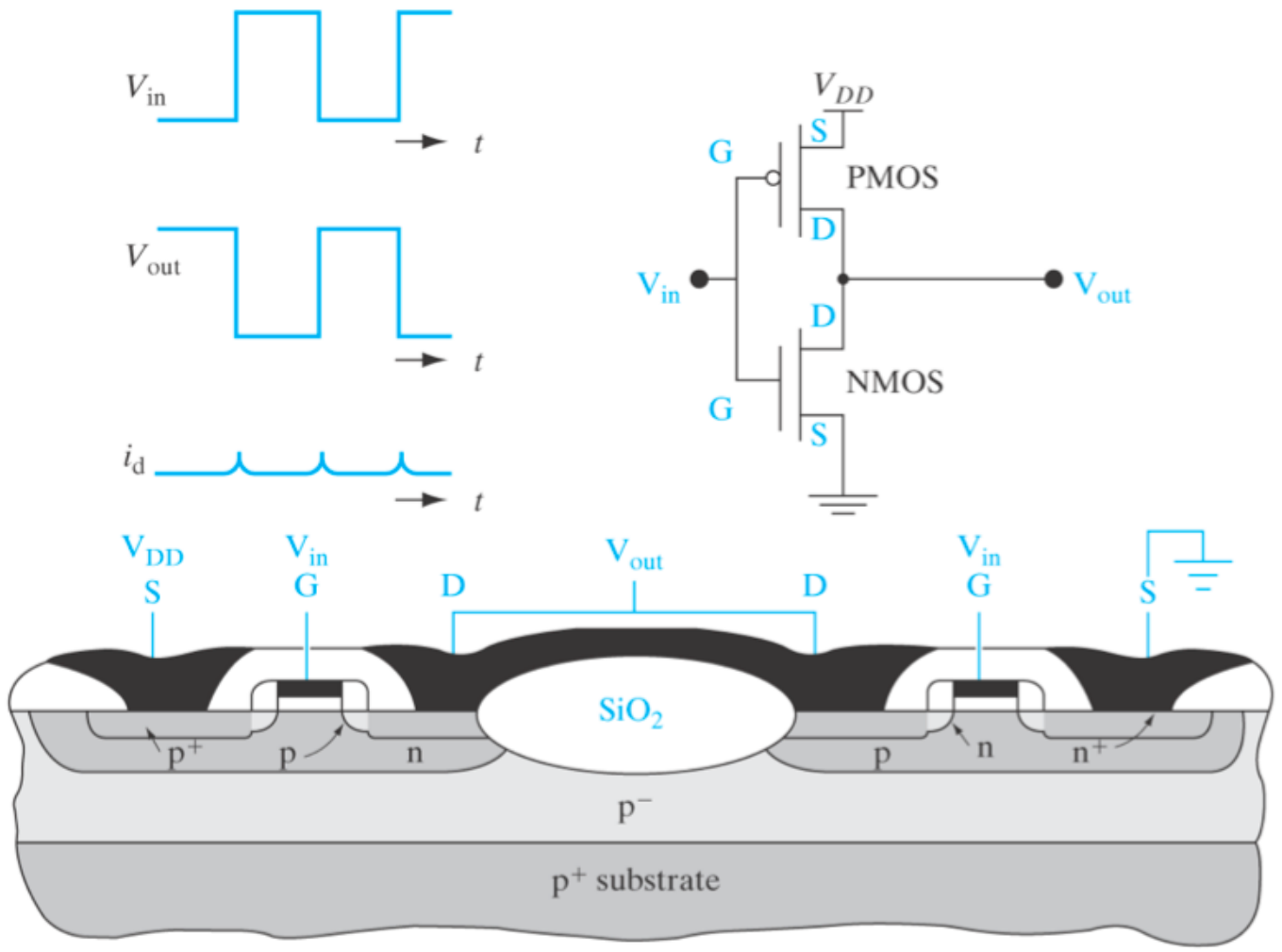
$$Q = CV = C\left(\frac{1}{2}V_{DD}\right) = \frac{1}{2}CV_{DD}$$

$$t_{PLH} = \frac{\frac{1}{2}CV_{DD}}{I_{DP}} = \frac{\frac{1}{2}CV_{DD}}{\frac{k_P}{2}(V_{DD}+V_{TP})^2}$$

CMOS Processing

Complimentary MOS

Cross Section: CMOS Inverter



Comment: Be aware of parasitic bipolar structures (pnpn switch) and latch-up

Self-Aligned Silicide (SALICIDE) Process

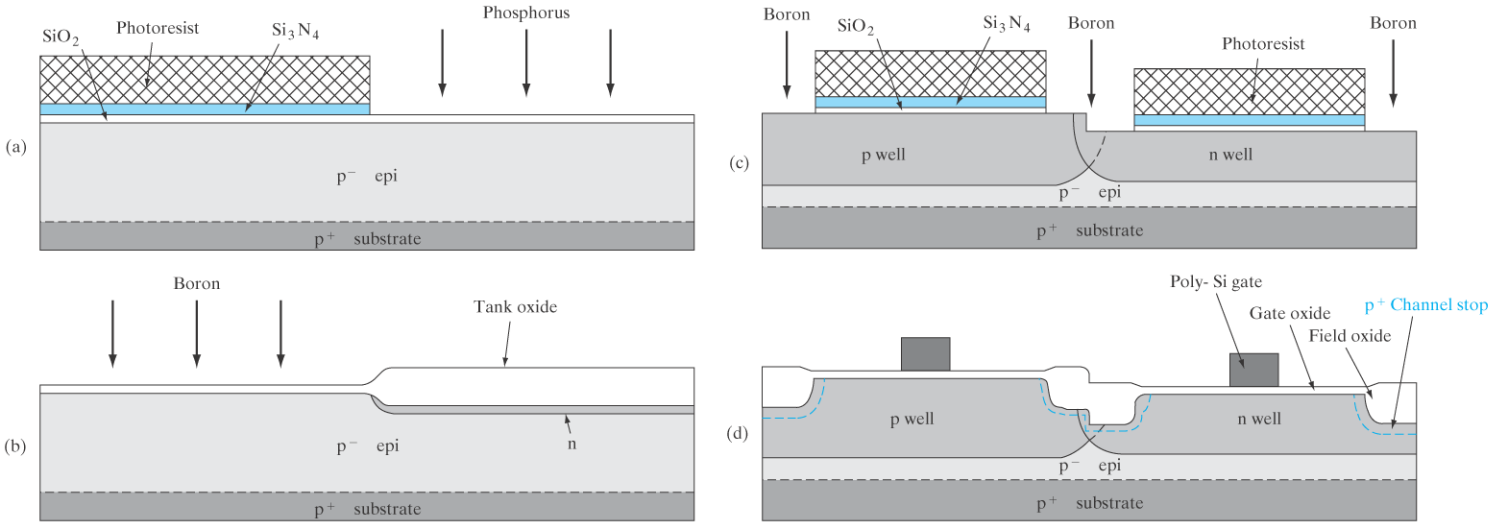
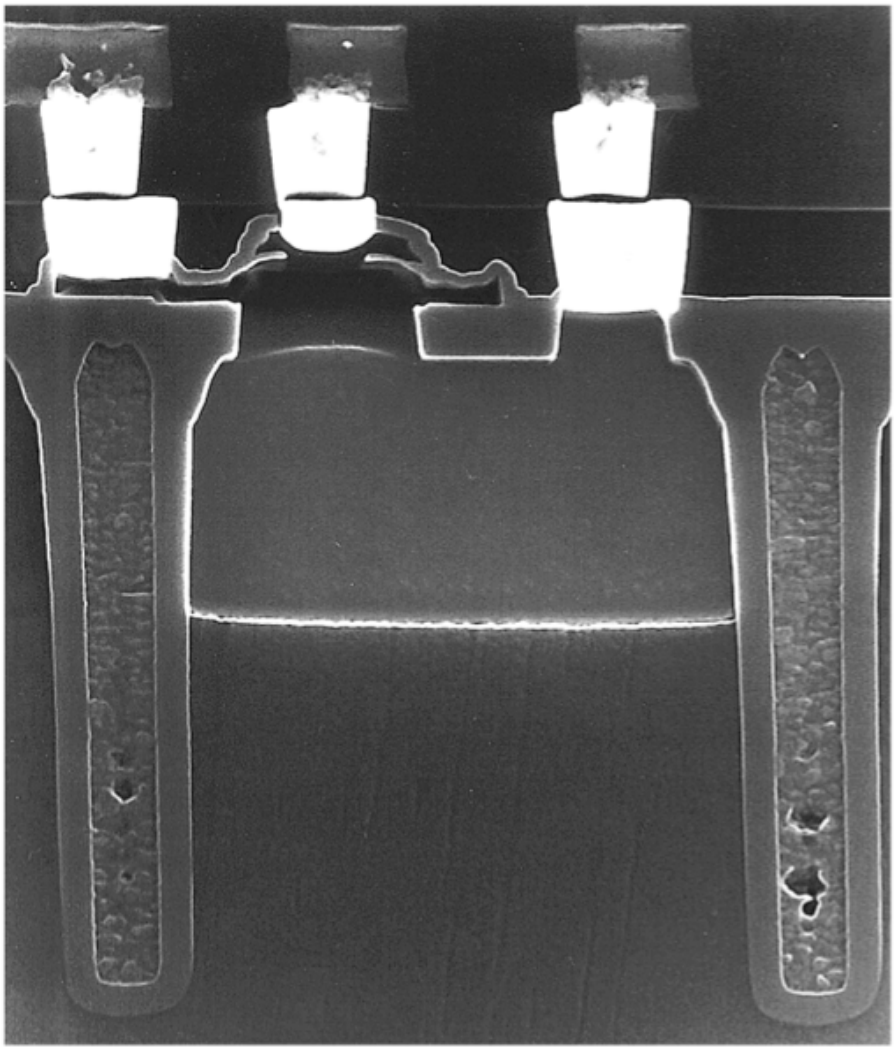


Figure 9.5

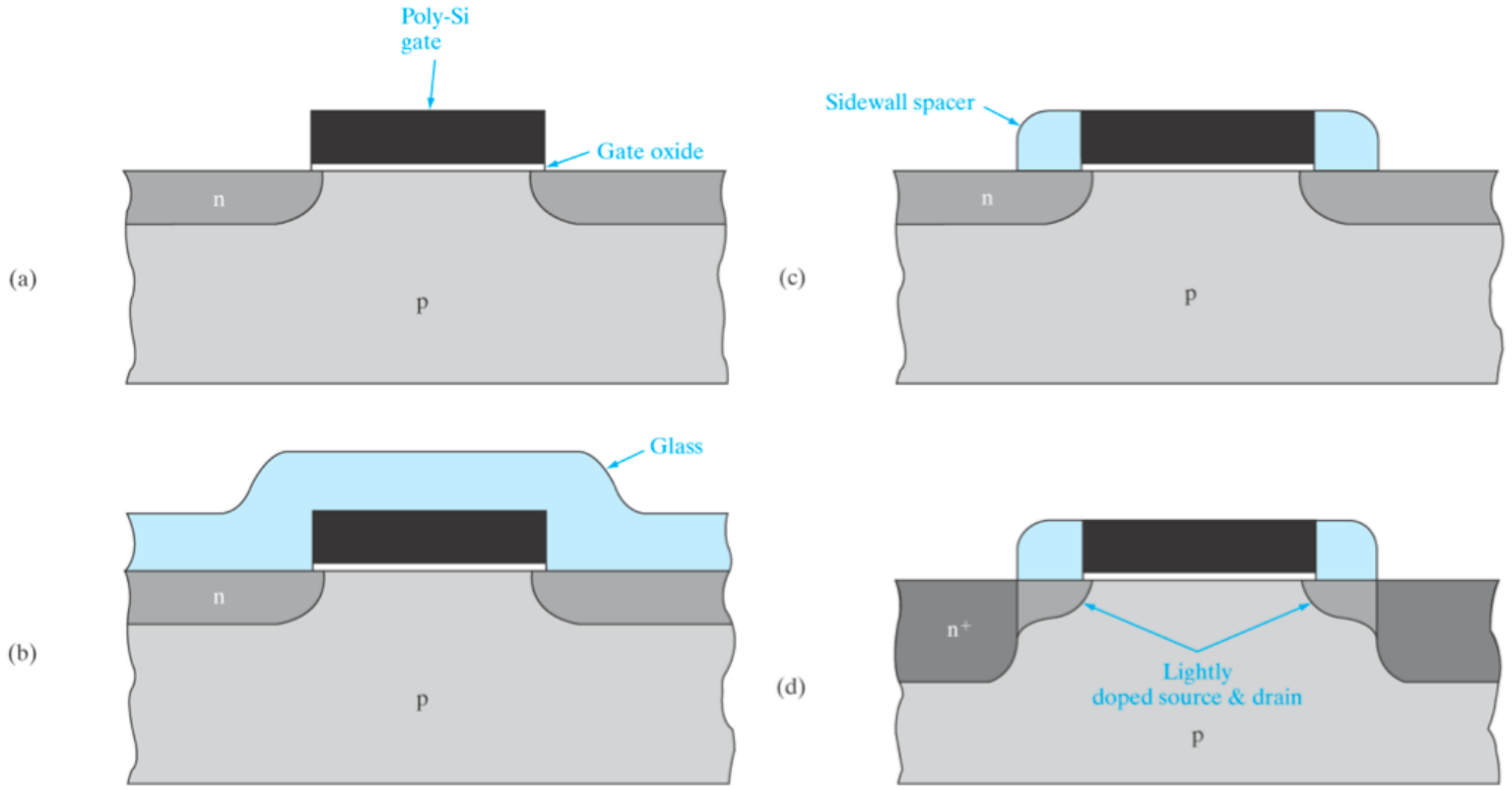
Self-aligned twin well process: (a) an n-well formation using P donor implant and a photoresist mask; (b) p-well formation using B acceptor implant. A thick (~200 nm) "tank" oxide layer is grown wherever the silicon nitride–oxide stack is etched off, and the tank oxide is used to block the B implant in the n-wells in a self-aligned manner; (c) an isolation pattern for field transistors showing a B channel stop implant using a photoresist mask; (d) local oxidation of silicon wherever the nitride mask is removed, leading to thick LOCOS field oxide.

Shallow Trench Isolation

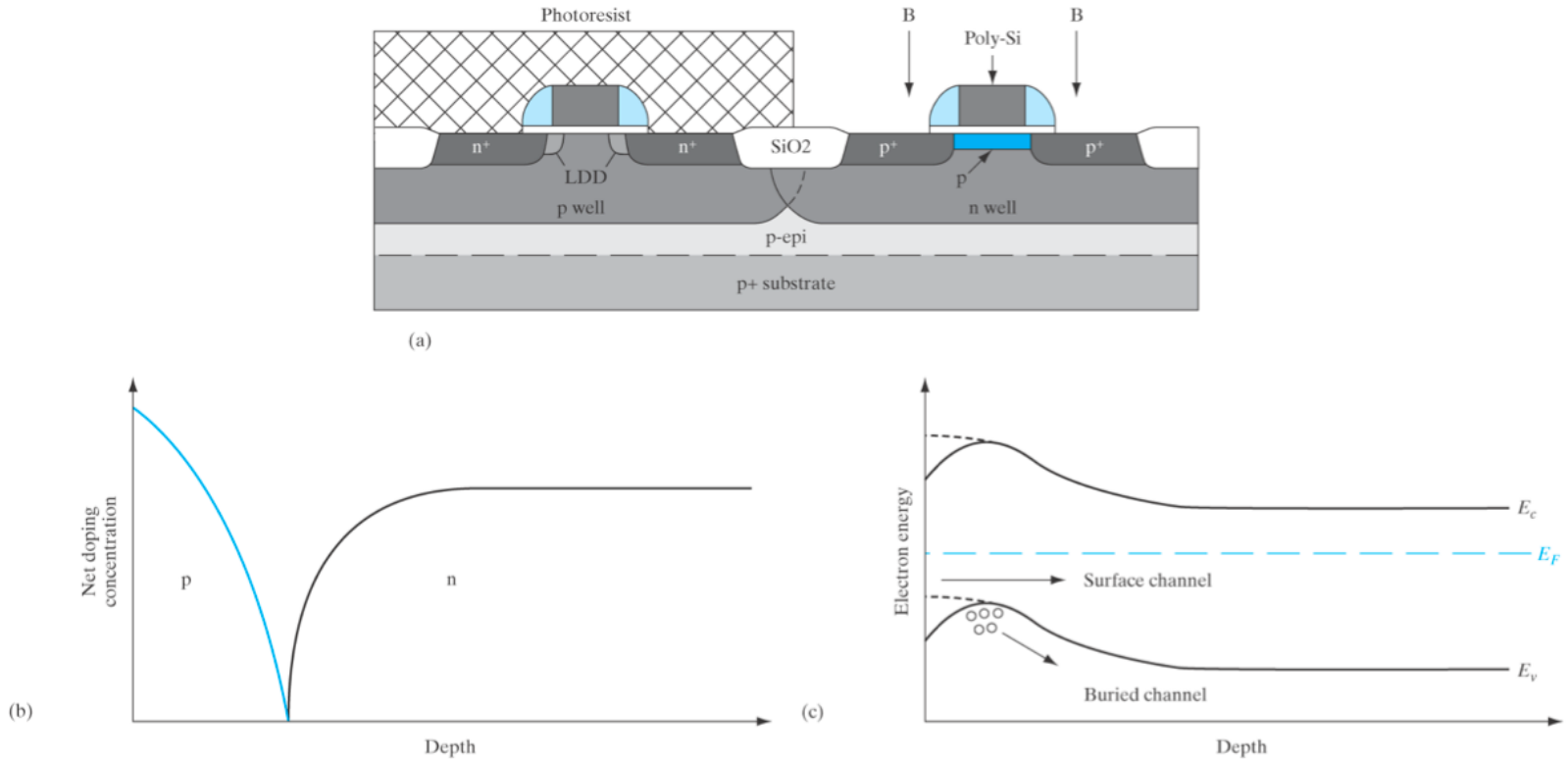
- Isolation process using SiO_2 and polysilicon
- Reduces issues with lateral oxidation using other isolation processes (“LOCOS”)



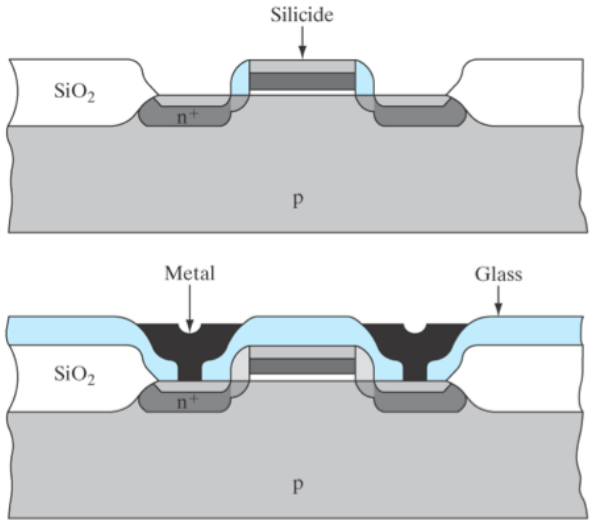
NMOS Fabrication in p-Well



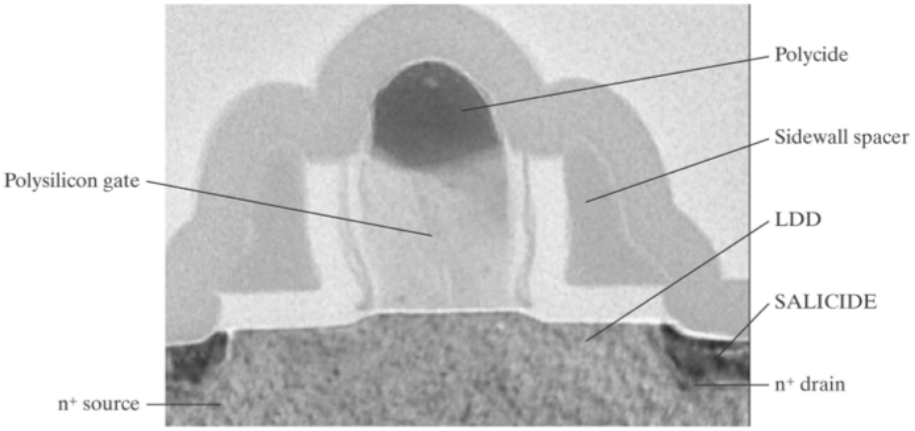
Buried Channel Operation



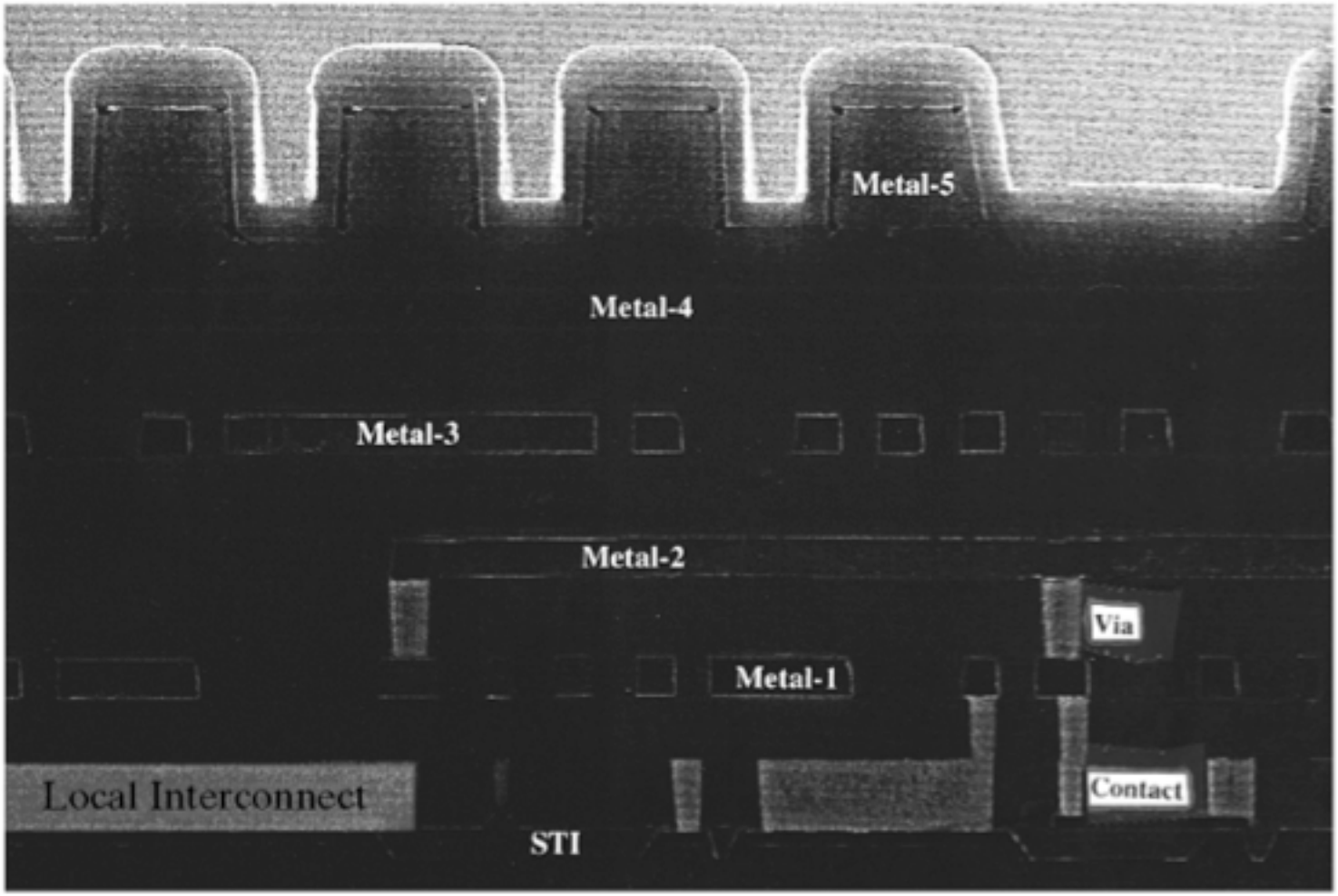
MOSFET with SALICIDE



(c)



Multilevel Interconnects



Assignments

Assignments

- Homework assigned every Friday, due following Friday
- Reading from Streetman's book:
  - Mon 4/9: §'s 6.4.3, 6.4.4
  - Fri 4/13: § 6.4.5
- Chapters 5, 6, 7, 8, and 9 in Pierret cover similar material

Assignments

- Homework assigned every Friday, due following Friday
- Reading from Streetman's book:
  - Mon 4/16: §'s 6.5.1, 6.5.2
  - Wed 4/18: §'s 6.5.8, 9.3.1, 9.5.1
  - Fri 4/20: Handout on BJT (Posted on Website)
  - Mon 4/23: §'s 6.1.1, 6.1.2, 7.1, 7.2, 7.3, and handout
  - Wed 4/25: §'s 7.3, 7.4.1, 7.4.2, 7.4.3, 7.4.4, and handout
  - Fri 4/27: §'s 7.3, 7.4.1, 7.4.2, 7.4.3, 7.4.4, and handout
  - Mon 4/30: §'s 7.4.1, 7.4.2, 7.4.3, 7.4.4, and handout
- Chapters 16, 17, 18, 10, 11, and 12 in Pierret cover similar material

Topics for Next Lecture

Outline, 4/9/18

- MOS Capacitors

Thank You for Listening!

Instructional Objectives (1)

By the time of exam No. 1 (after 17 lectures), the students should be able to do the following:

1. Outline the classification of solids as metals, semiconductors, and insulators and distinguish direct and indirect semiconductors.
2. Determine relative magnitudes of the effective mass of electrons and holes from an E(k) diagram.
3. Calculate the carrier concentration in intrinsic semiconductors.
4. Apply the Fermi-Dirac distribution function to determine the occupation of electron and hole states in a semiconductor.
5. Calculate the electron and hole concentrations if the Fermi level is given; determine the Fermi level in a semiconductor if the carrier concentration is given.
6. Determine the variation of electron and hole mobility in a semiconductor with temperature, impurity concentration, and electrical field.
7. Apply the concept of compensation and space charge neutrality to calculate the electron and hole concentrations in compensated semiconductor samples.
8. Determine the current density and resistivity from given carrier densities and mobilities.
9. Calculate the recombination characteristics and excess carrier concentrations as a function of time for both low level and high level injection conditions in a semiconductor.
10. Use quasi-Fermi levels to calculate the non-equilibrium concentrations of electrons and holes in a semiconductor under uniform photoexcitation.
11. Calculate the drift and diffusion components of electron and hole currents.
12. Calculate the diffusion coefficients from given values of carrier mobility through the Einstein's relationship and determine the built-in field in a non-uniformly doped sample.

https://my.ece.illinois.edu/courses/description.asp?ECE340

Instructional Objectives (2)

By the time of Exam No.2 (after 32 lectures), the students should be able to do all of the items listed under A, plus the following:

13. Calculate the contact potential of a p-n junction.
14. Estimate the actual carrier concentration in the depletion region of a p-n junction in equilibrium.
15. Calculate the maximum electrical field in a p-n junction in equilibrium.
16. Distinguish between the current conduction mechanisms in forward and reverse biased diodes.
17. Calculate the minority and majority carrier currents in a forward or reverse biased p-n junction diode.
18. Predict the breakdown voltage of a p+-n junction and distinguish whether it is due to avalanche breakdown or Zener tunneling.
19. Calculate the charge storage delay time in switching p-n junction diodes.
20. Calculate the capacitance of a reverse biased p-n junction diode.
21. Calculate the capacitance of a forward biased p-n junction diode.
22. Predict whether a metal-semiconductor contact will be a rectifying contact or an ohmic contact based on the metal work function and the semiconductor electron affinity and doping.
23. Calculate the electrical field and potential drop across the neutral regions of wide base, forward biased p+-n junction diode.
24. Calculate the voltage drop across the quasi-neutral base of a forward biased narrow base p+-n junction diode.
25. Calculate the excess carrier concentrations at the boundaries between the space-charge region and the neutral n- and p-type regions of a p-n junction for either forward or reverse bias.

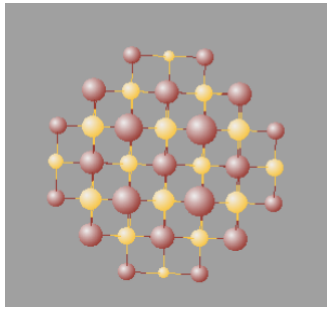
Instructional Objectives (3)

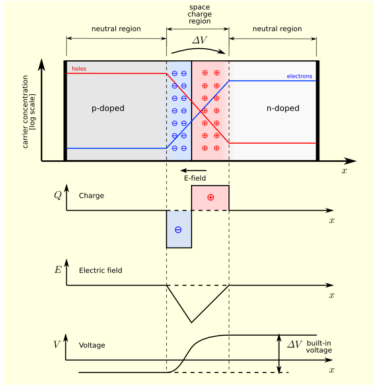
By the time of the Final Exam, after 44 class periods, the students should be able to do all of the items listed under A and B, plus the following:

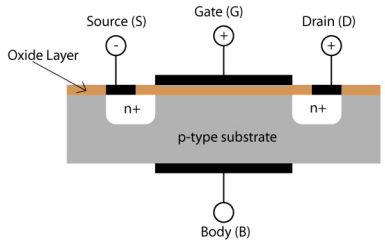
26. Calculate the terminal parameters of a BJT in terms of the material properties and device structure.
27. Estimate the base transport factor “B” of a BJT and rank-order the internal currents which limit the gain of the transistor.
28. Determine the rank order of the electrical fields in the different regions of a BJT in forward active bias.
29. Calculate the threshold voltage of an ideal MOS capacitor.
30. Predict the C-V characteristics of an MOS capacitor.
31. Calculate the inversion charge in an MOS capacitor as a function of gate and drain bias voltage.
32. Estimate the drain current of an MOS transistor above threshold for low drain voltage.
33. Estimate the drain current of an MOS transistor at pinch-off.
34. Distinguish whether a MOSFET with a particular structure will operate as an enhancement or depletion mode device.
35. Determine the short-circuit current and open-circuit voltage for an illuminated p/n junction solar cell.

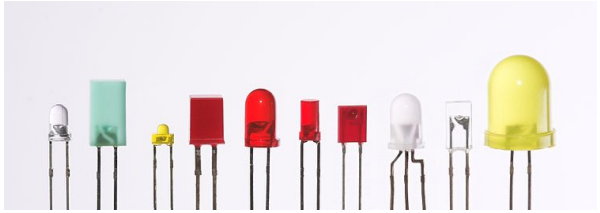
Course Purpose & Objectives

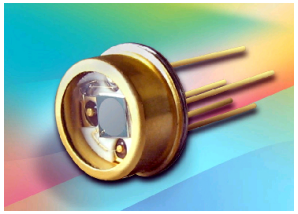
- Introduce key concepts in semiconductor materials
- Provide a basic understanding of p-n junctions
- Provide a basic understanding of light-emitting diodes and photodetectors
- Provide a basic understanding of field effect transistors
- Provide a basic understanding of bipolar junction transistors

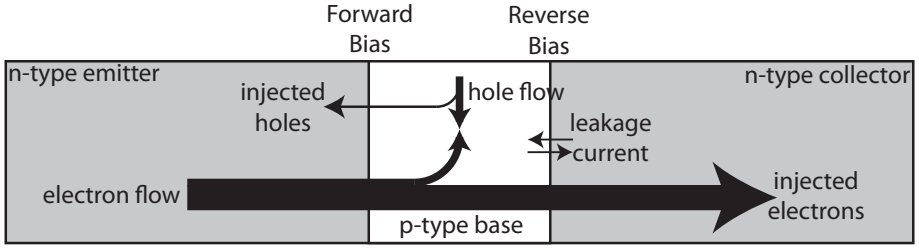












Tentative Schedule [1]

	JAN 17 Course overview	JAN 19 Intro to semiconductor electronics
JAN 22 Materials and crystal structures	JAN 24 Bonding forces and energy bands in solids	JAN 26 Metals, semiconductors, insulators, electrons, holes
JAN 29 Intrinsic and extrinsic material	JAN 31 Distribution functions and carrier concentrations	FEB 2 Distribution functions and carrier concentrations
FEB 5 Temperature dependence, compensation	FEB 7 Conductivity and mobility	FEB 9 Resistance, temperature, impurity concentration
FEB 12 Invariance of Fermi level at equilibrium	FEB 14 Optical absorption and luminescence	FEB 16 Generation and recombination

Subject to Change

Tentative Schedule [2]

FEB 19 Quasi-Fermi levels and photoconductive devices	FEB 21 Carrier diffusion	FEB 23 Built-in fields, diffusion and recombination
Feb 26 Review, discussion, problems (2/27 exam)	FEB 28 Steady state carrier injection, diffusion length	MAR 2 p-n junctions in equilibrium & contact potential
MAR 5 p-n junction Fermi levels and space charge	MAR 7 Continue p-n junction space charge	MAR 9 NO CLASS (EOH)
MAR 12 p-n junction current flow	MAR 14 Carrier injection and the diode equation	MAR 16 Minority and majority carrier currents
3/19-3/23 Spring Break MAR 26 Reverse-bias breakdown	MAR 28 Stored charge, diffusion and junction capacitance	MAR 30 Photodiodes, I-V under illumination

Subject to Change

Schedule & Policies

Important Information

- Course Website:
  - http://courses.engr.illinois.edu/ece340/
- Download and Review Syllabus / Course Information from Website!
- Course Coordinator: Prof. John Dallesasse
  - jdallesa@illinois.edu
  - Coordinates schedule, policies, absence issues, homework, quizzes, exams, etc.
- Contact Information and Office Hours for All ECE340 Professors & TAs in Syllabus
- Lecture Slides: Click on "(Sec. X)" next to my name in instructor list
- DRES Students: Contact Prof. Dallesasse ASAP
- Textbook:
  - "Solid State Electronic Devices," Streetman & Banerjee, 7th Edition
  - Supplemental: "Semiconductor Device Fundamentals," Pierret
  - Additional reference texts listed in syllabus

Key Points

- Attend Class!
  - 3 unannounced quizzes, each worth 5% of your grade
  - **You must take the quiz in your section**
  - Excused absences must be **pre-arranged** with the course director
  - Absences for illness, etc. need a note from the Dean
    - See policy on absences in the syllabus
- No Late Homework
  - Homework due on the date of an excused absence must be turned in ahead of time
  - You must turn in homework in your section
  - No excused absences for homework assignments
  - Top 10 of 11 homework assignments used in calculation of course grade
    - Do all of them to best prepare for the exams!
- No Cheating
  - Penalties are severe and will be enforced
- Turn Off Your Phone
  - No video recording, audio recording, or photography

Homework

- Assigned Friday, Due Following Friday
  - Due dates shown in syllabus
- Due at Start of Class
- Follow Guidelines in Syllabus
- Peer Discussions Related to Homework are Acceptable and Encouraged
- Directly Copying Someone Else's Homework is Not Acceptable
  - Graders have been instructed to watch for evidence of plagiarism
  - Both parties will receive a "0" on the problem or assignment

Absences

- The absence policy in the syllabus will be strictly enforced
- To receive an excused absence (quiz), you must:
  - Pre-arrange the absence with the course director (valid reason and proof required)
  - Complete an Excused Absence Form at the Undergraduate College Office, Room 207 Engineering Hall (333-0050)
    - The form must be signed by a physician, medical official, or the Emergency Dean (Office of the Dean of Students)
    - The Dean's Office has recently put a strict policy in place (3 documented days of illness)
  - Excused quiz score will be prorated based upon average of completed scores
  - No excused absences are given for homework, but only the best 10 of 11 are used to calculate your final grade
  - Excused absences are not given for exams, except in accordance with the UIUC Student Code
  - Unexcused work will receive a "0"
- Failure to take the final will result in an "incomplete" grade (if excused) or a "0" (if unexcused)

Exams

- Exam I: Tuesday February 27th, 7:30-8:30 pm
- Exam II: Thursday April 12th, 7:30-8:30 pm
- Final Exam: Date/Time To Be Announced
  - Determined by University F&S

Grading

Grading Criterion

Homework	10 %
Quizzes	15 %
Hour Exam I	20 %
Hour Exam II	20 %
Final Exam	35 %
Total	100 %

Historical Grade Trends*

	Spring 2016	Fall 2016	Spring 2017
A's	27 %	28 %	27 %
B's	37 %	26 %	38 %
C's	27 %	25 %	27%
D's	6 %	16 %	4 %
F's	3 %	5 %	4 %

*Past performance is not necessarily indicative of future results

My Recommendations

- Read the syllabus and information posted on the course website
- **Attend class** & participate
- Attend office hours (TA and Professors)
- **Read the book**
- Re-read the book
- Look at and read selected portions of the supplemental texts
- Form study groups to review concepts and discuss high-level approaches for solving homework problems
  - Don't form study groups to copy homework solutions
- **Don't miss any homework, quizzes, or exams**
  - It's hard to overcome a zero
- Ask questions in class!

Instructional Objectives (1)

By the time of exam No. 1 (after 17 lectures), the students should be able to do the following:

✔1. Outline the classification of solids as metals, semiconductors, and insulators and distinguish direct and indirect semiconductors.

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✔4. Apply the Fermi-Dirac distribution function to determine the occupation of electron and hole states in a semiconductor.

✔5. Calculate the electron and hole concentrations if the Fermi level is given; determine the Fermi level in a semiconductor if the carrier concentration is given.

✔6. Determine the variation of electron and hole mobility in a semiconductor with temperature, impurity concentration, and electrical field.

✔7. Apply the concept of compensation and space charge neutrality to calculate the electron and hole concentrations in compensated semiconductor samples.

✔8. Determine the current density and resistivity from given carrier densities and mobilities.

✔9. Calculate the recombination characteristics and excess carrier concentrations as a function of time for both low level and high level injection conditions in a semiconductor.

✔10. Use quasi-Fermi levels to calculate the non-equilibrium concentrations of electrons and holes in a semiconductor under uniform photoexcitation.

✔11. Calculate the drift and diffusion components of electron and hole currents.

✔12. Calculate the diffusion coefficients from given values of carrier mobility through the Einstein's relationship and determine the built-in field in a non-uniformly doped sample.

Plus continuity equation, steady-state carrier injection, and diffusion length

https://my.ece.illinois.edu/courses/description.asp?ECE340

Quiz 1 Statistics

- Average: 8.65
- Standard Deviation: 1.49

Quiz 2 Statistics

- Average: 4.59
- Standard Deviation: 1.86

Exam I Statistics

- Average (All Sections): 71.88
- Standard Deviation (All Sections): 15.44

Streetman Errata (6th Edition)

- Equation 4-30: “ΔxA” not δxA
- Equation 4-33b: “τ_p” not “τ_n”

Final Exam Schedule

Course	Section	CRN	Date	Day	Start Time	End Time	Room	Exam Type
ECE 340	ALL	ALL	05/04/2018	F	1:30 PM	4:30 PM	1002 Electrical & Computer Eng Bldg	Combined
ECE 340	ALL	ALL	05/04/2018	F	7:00 PM	10:00 PM	2015 Electrical & Computer Eng Bldg	Conflict