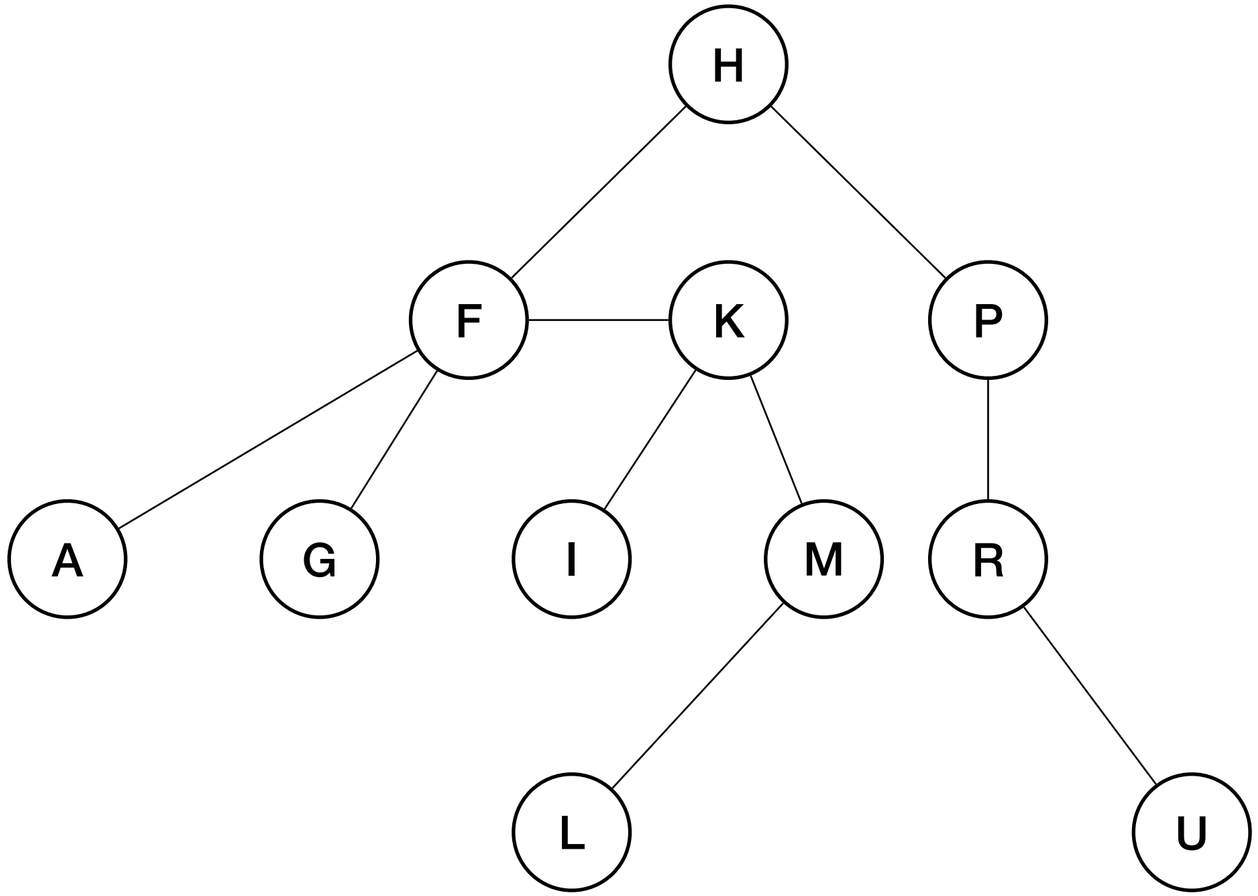
ECE 220

Lecture x0019 - 12/03
Recap & Interrupts in LC3

Post-break recall



Recap + reminders

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    - Concepts & properties

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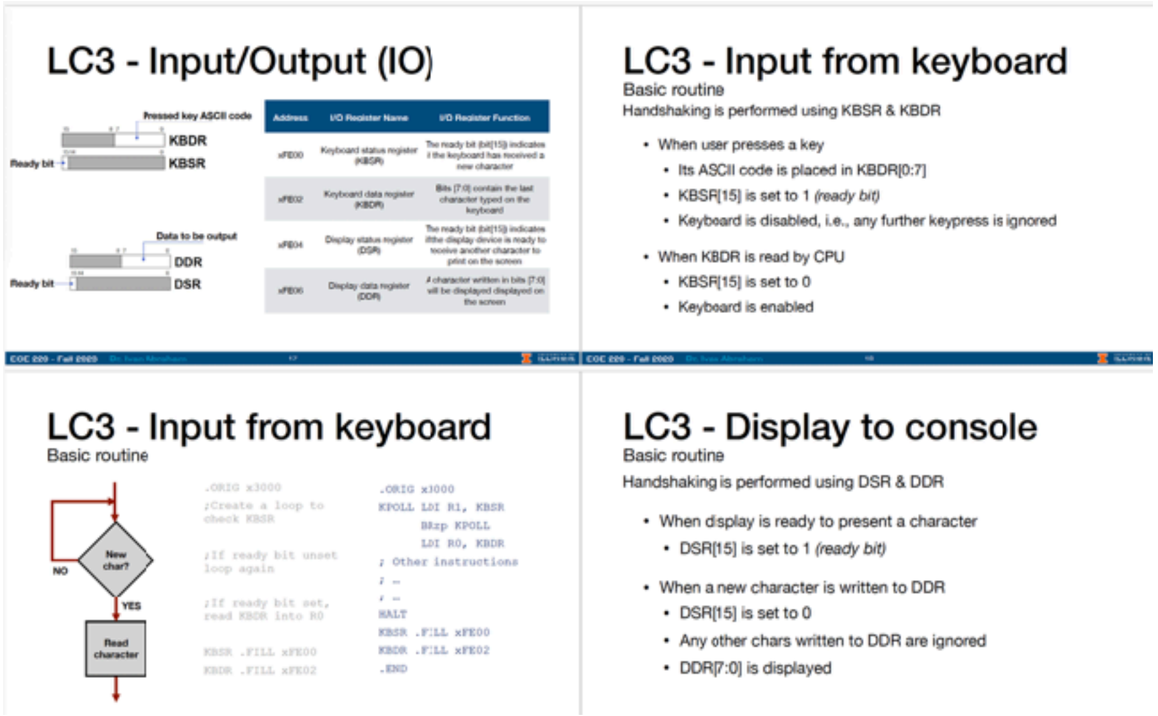

Slides from Lecture #1

Previously - I/O using Polling or TRAPs

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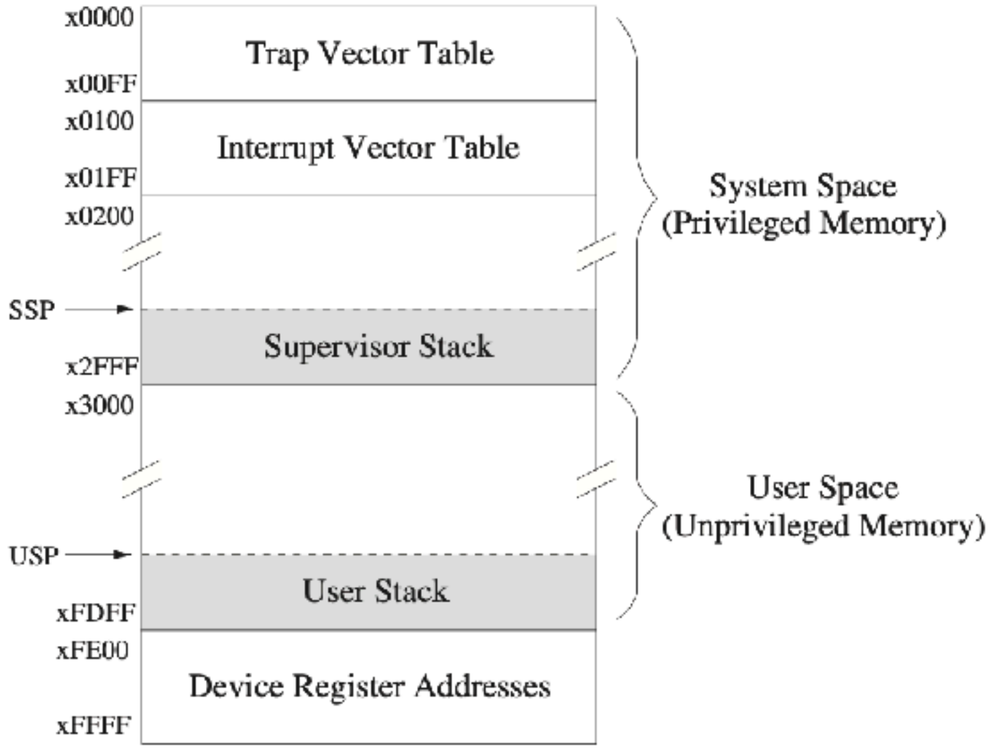

Figure A.1 - P&P 3rd Ed.

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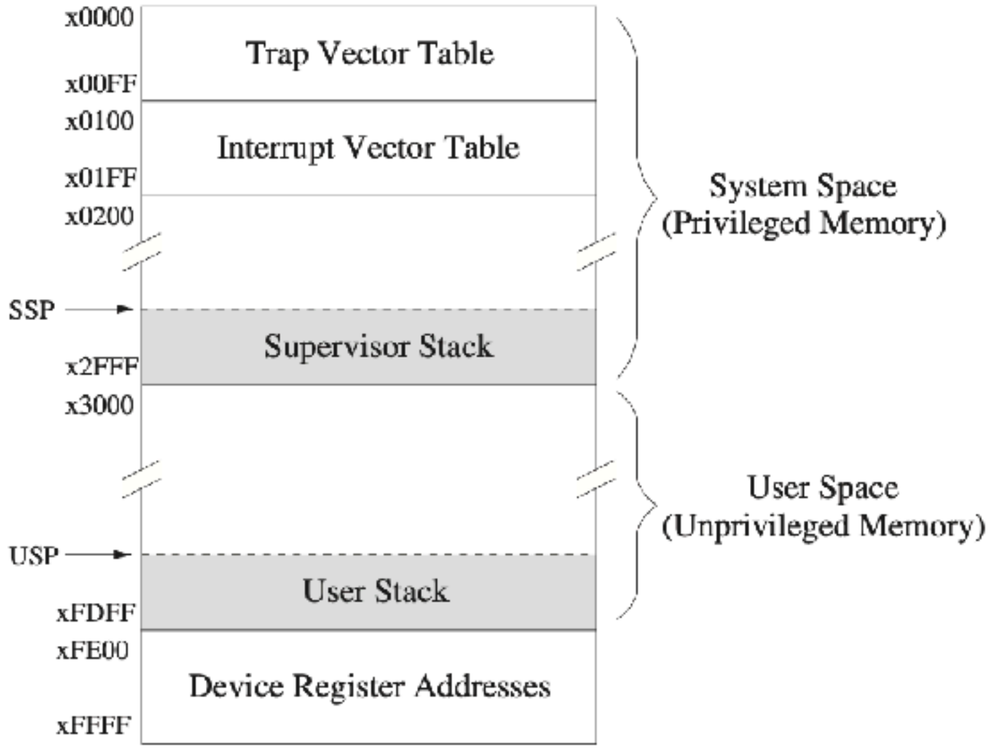

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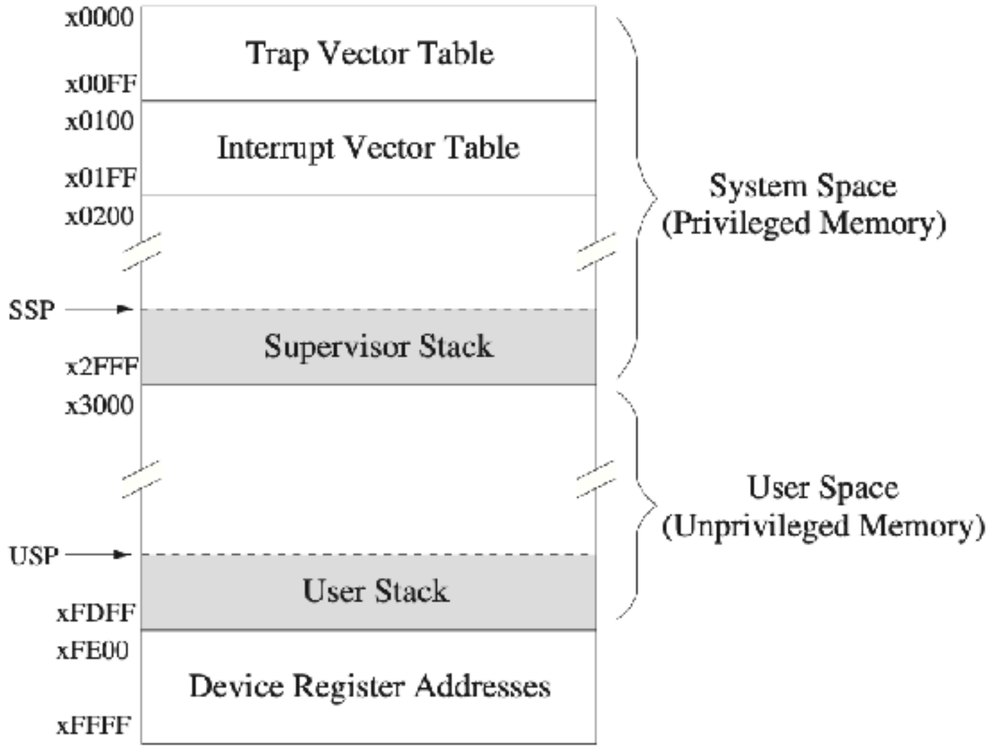

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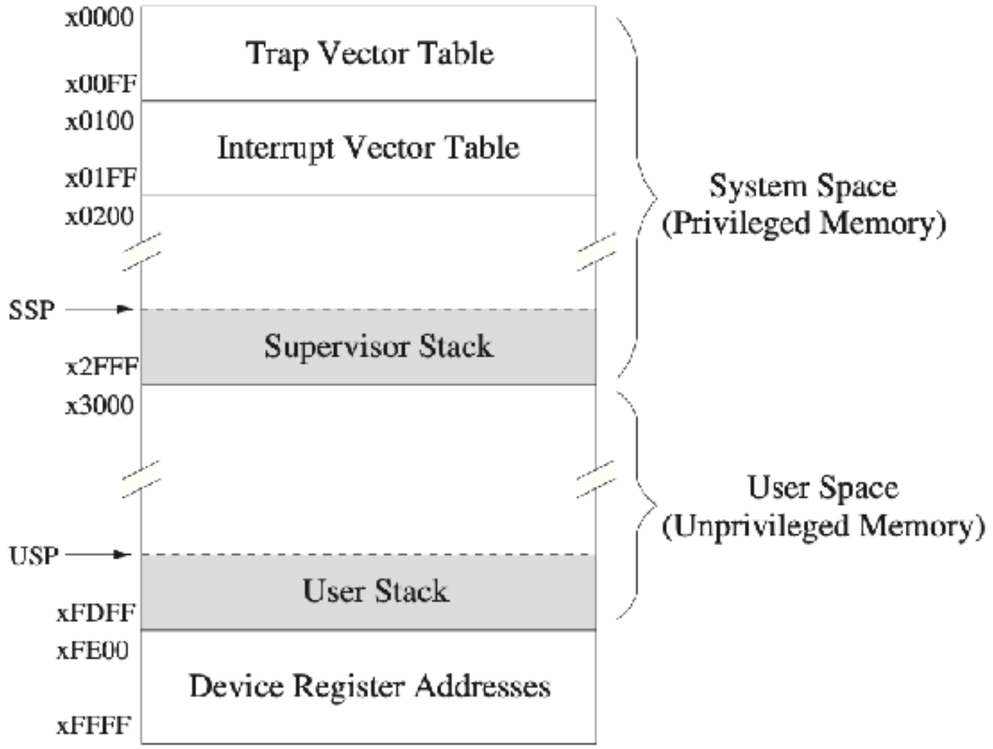

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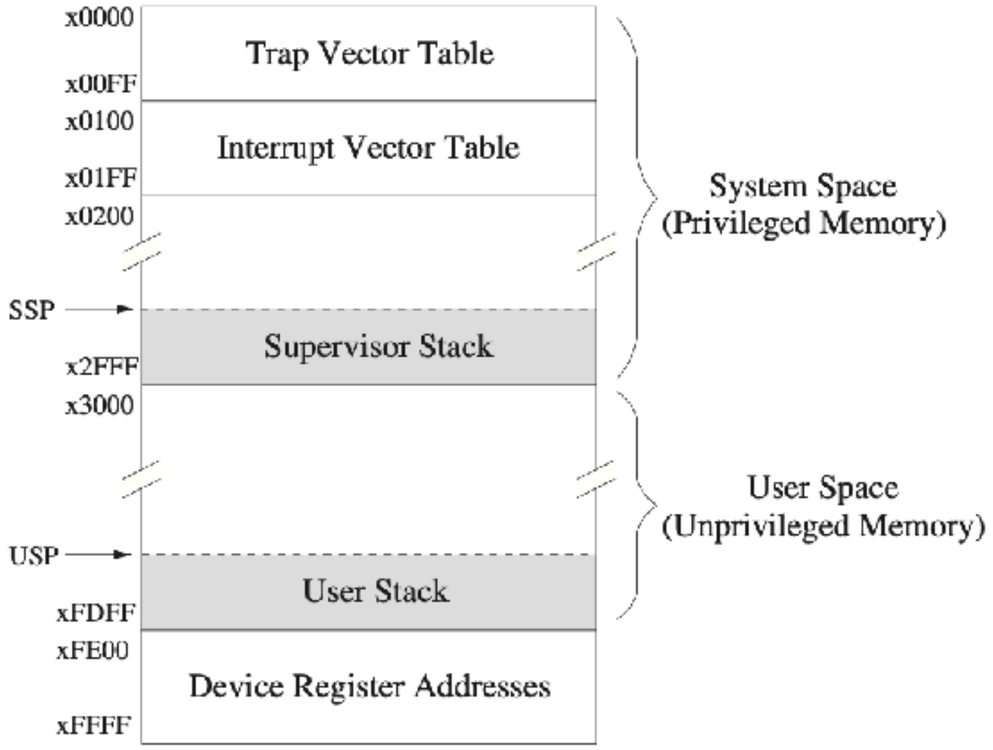

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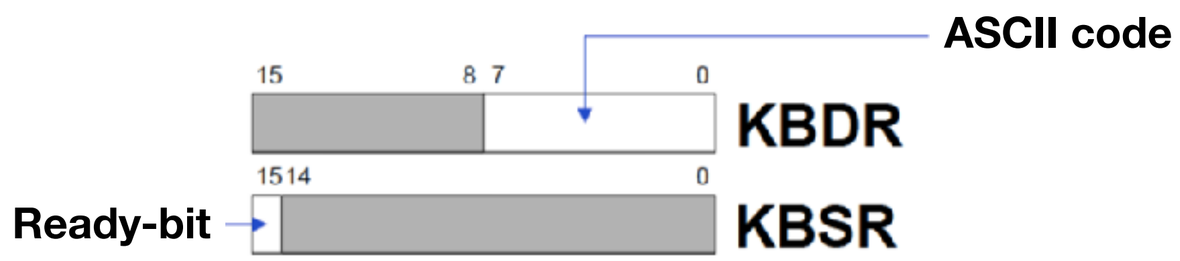

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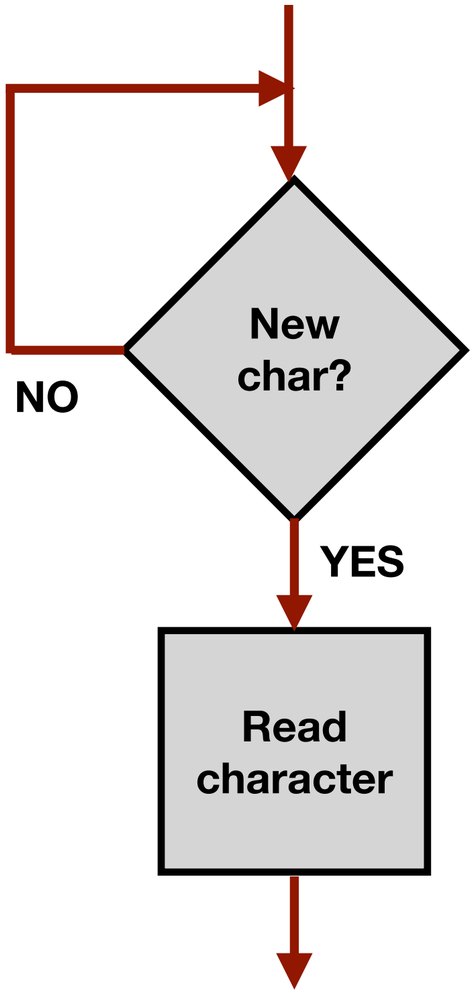

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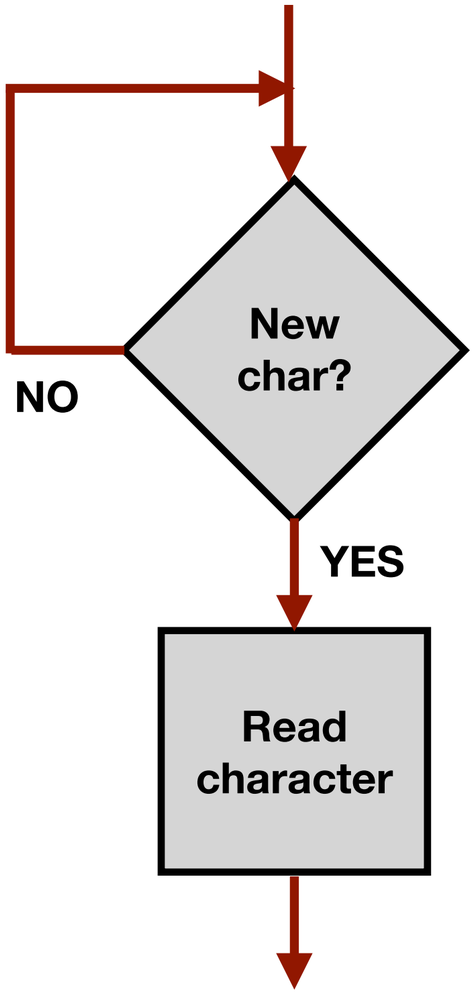

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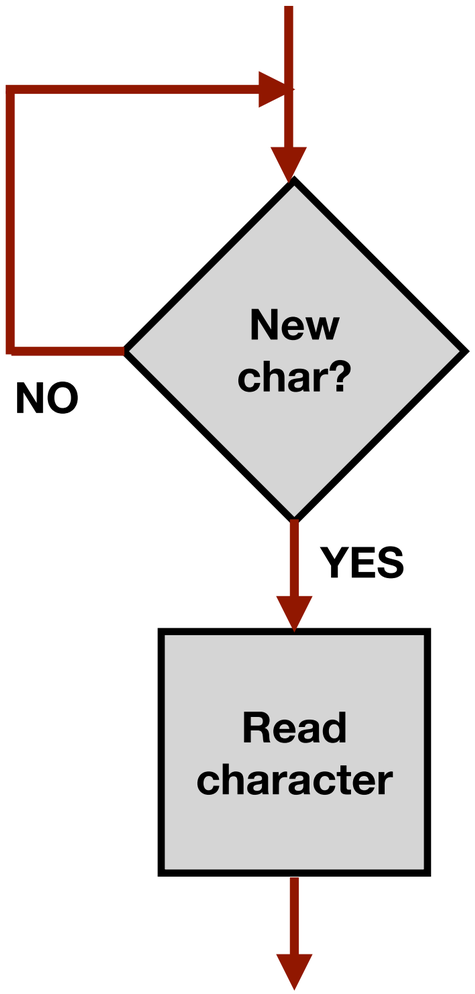

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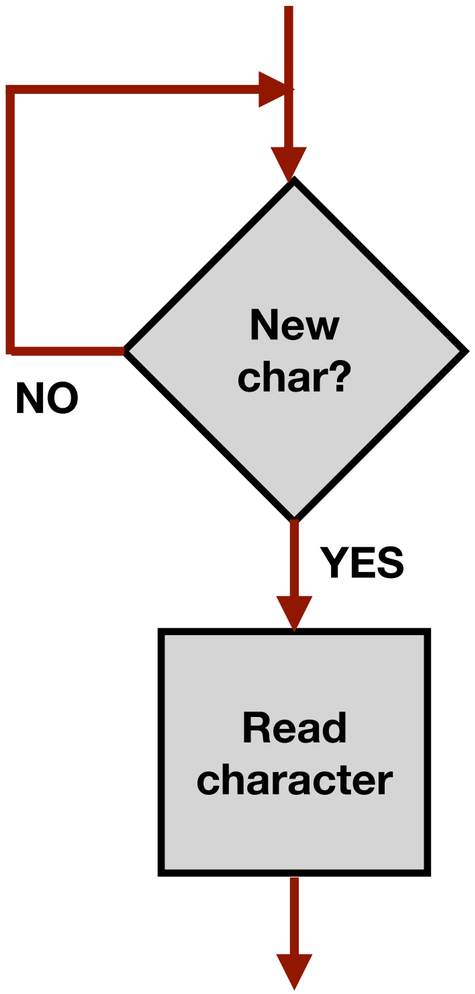

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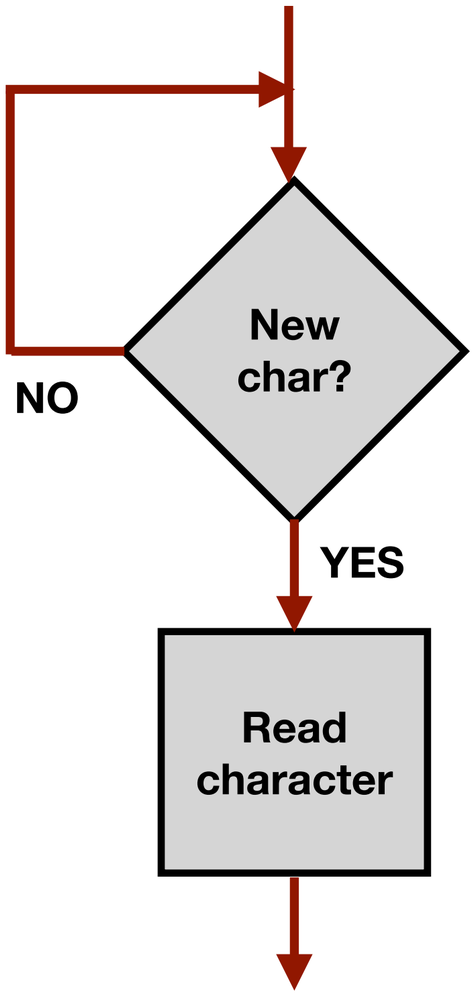

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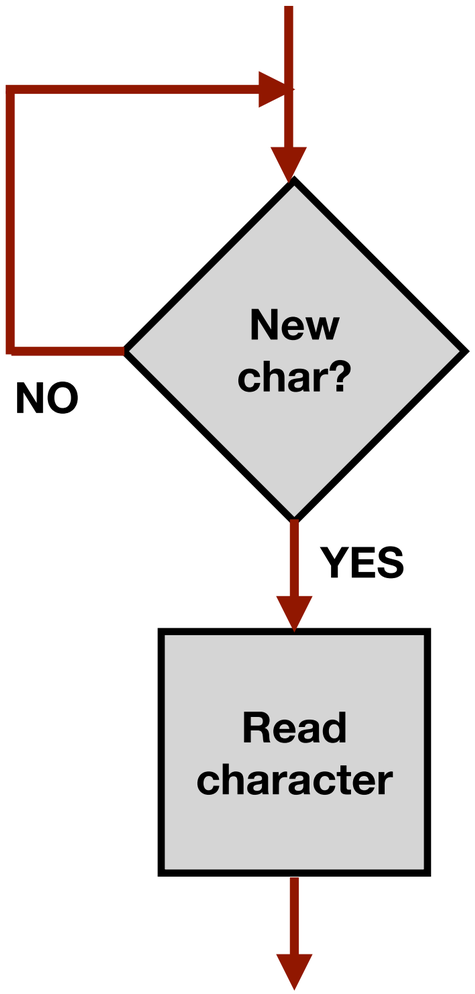

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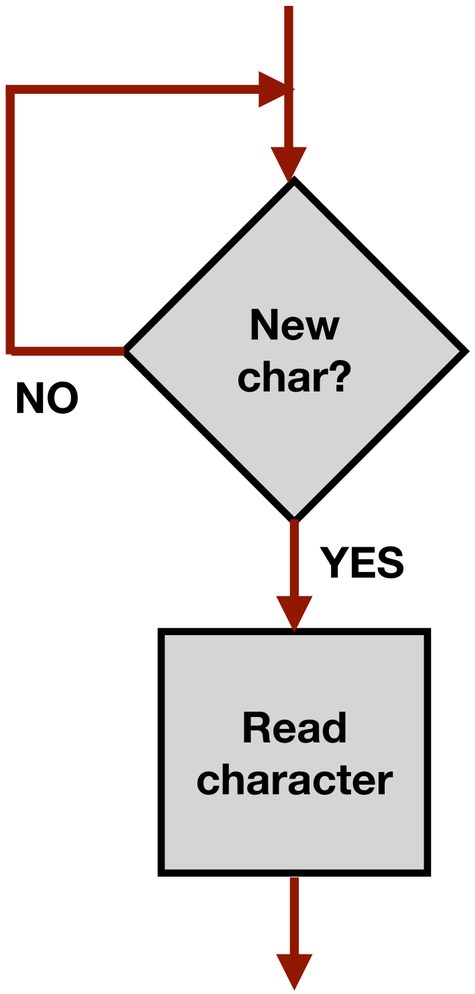

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- How can we free up the processor to do other tasks?

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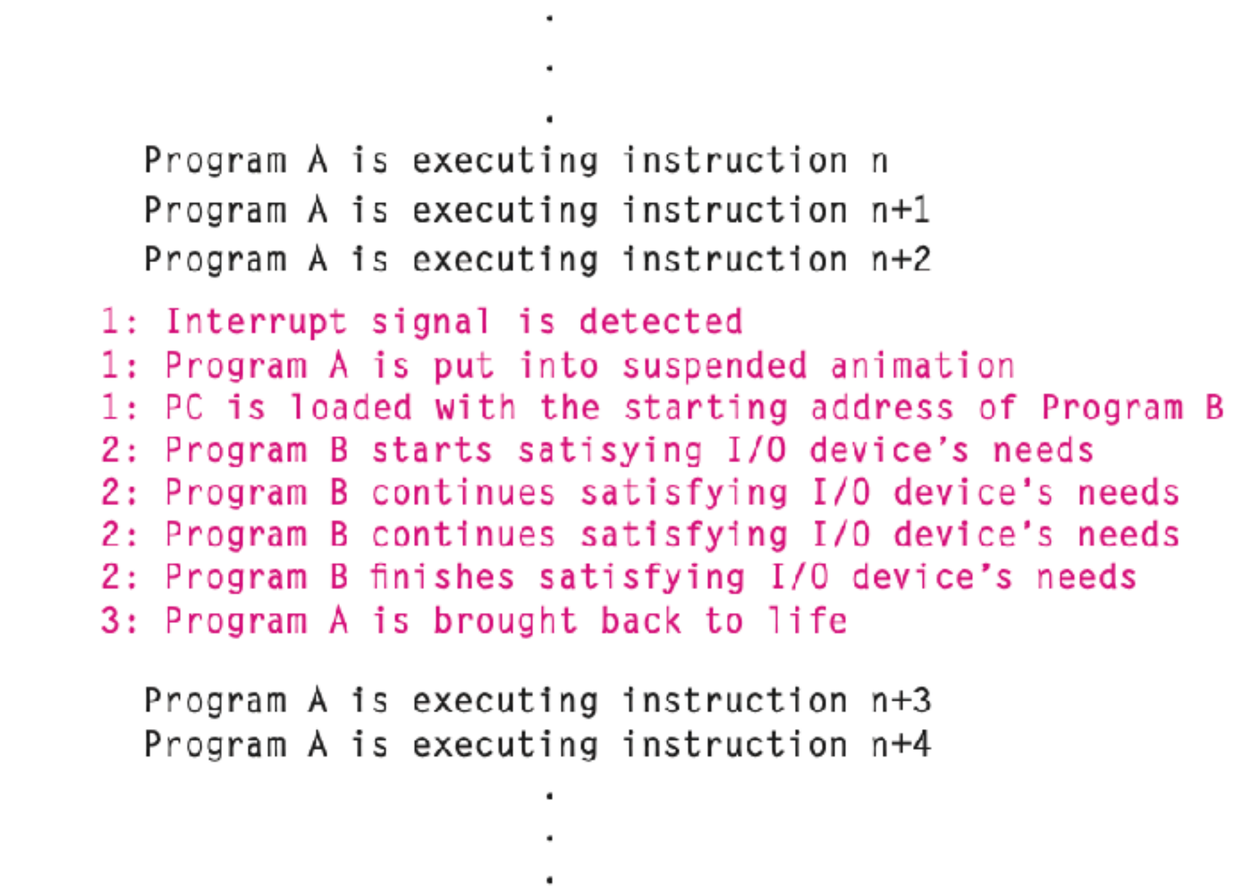
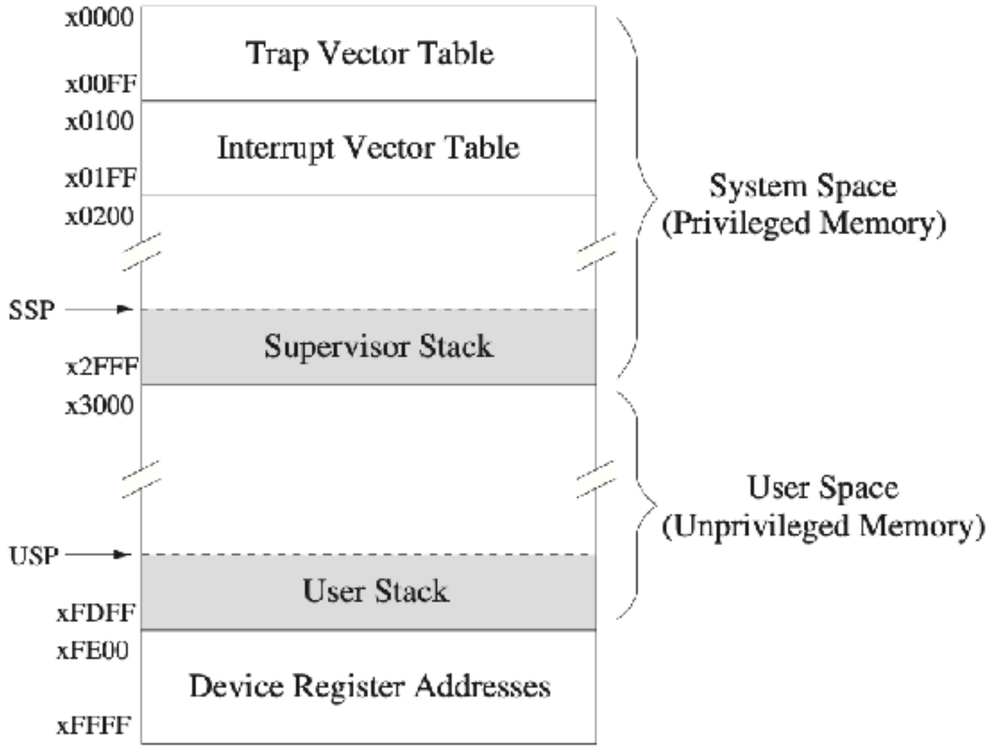


Figure 9.17 Instruction execution flow for interrupt-driven I/O.

Now - I/O using interrupts



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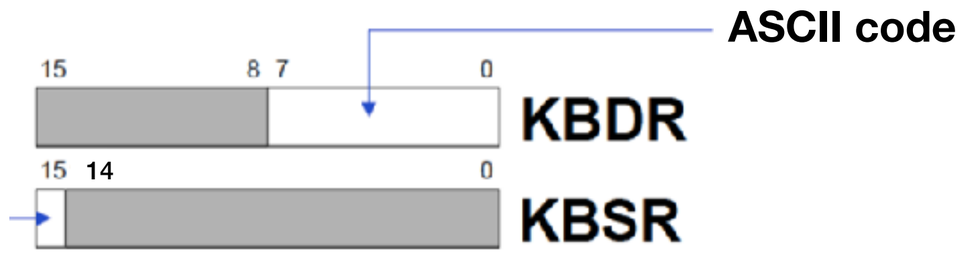

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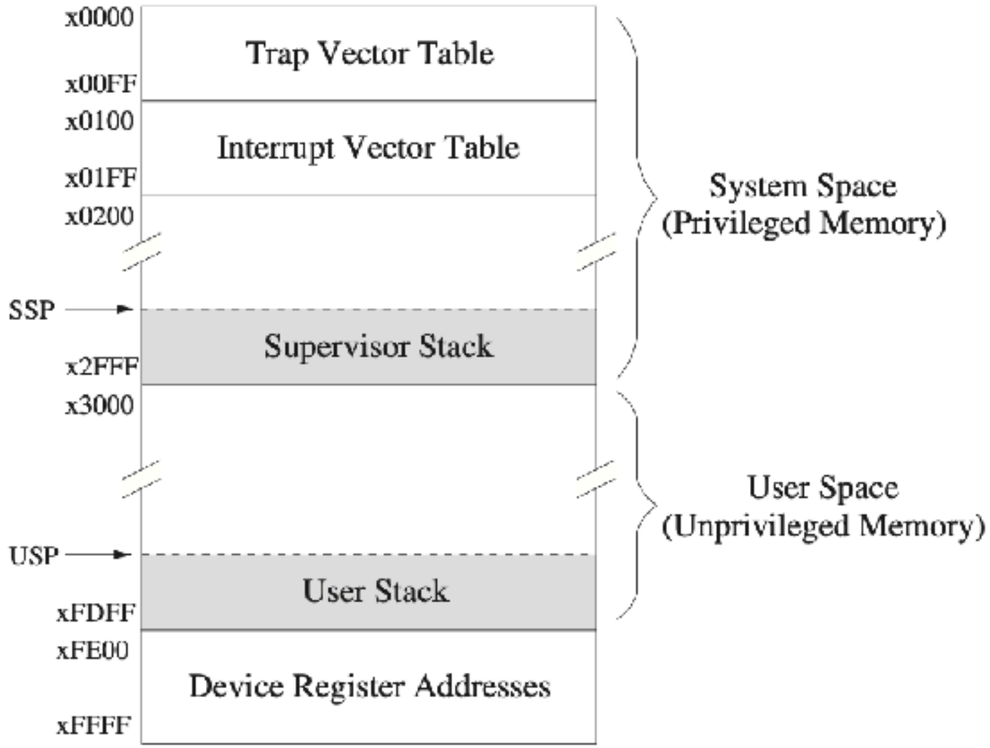

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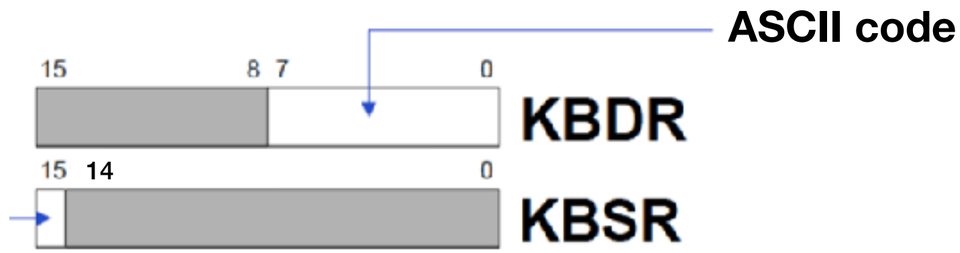

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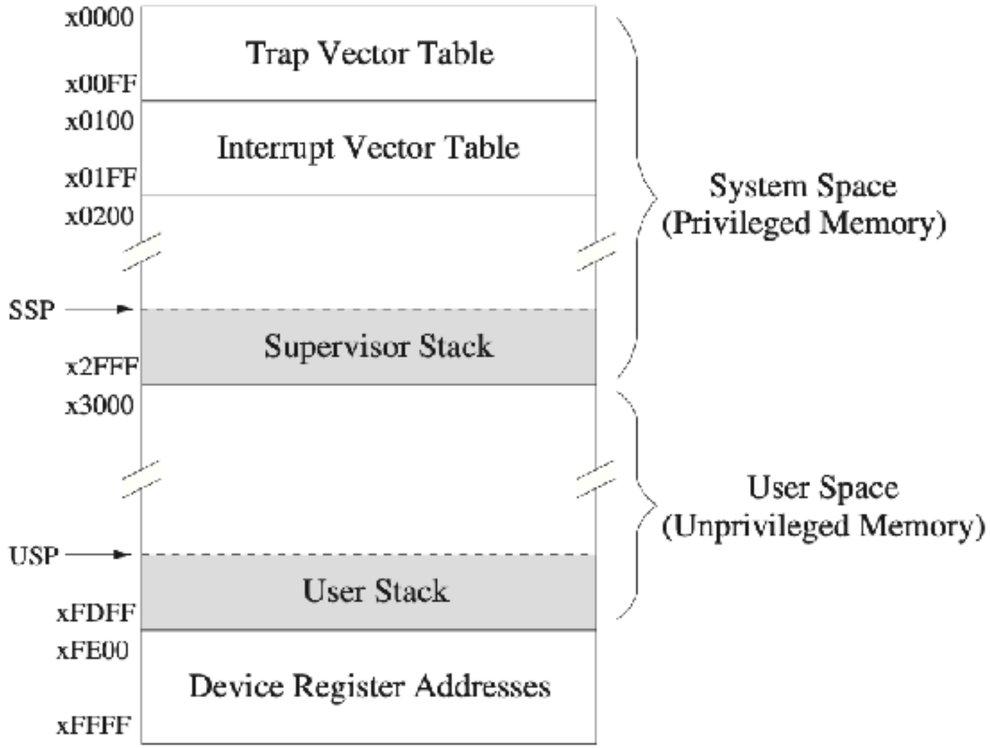

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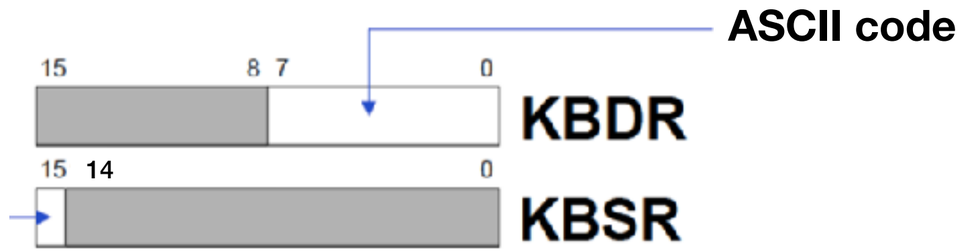

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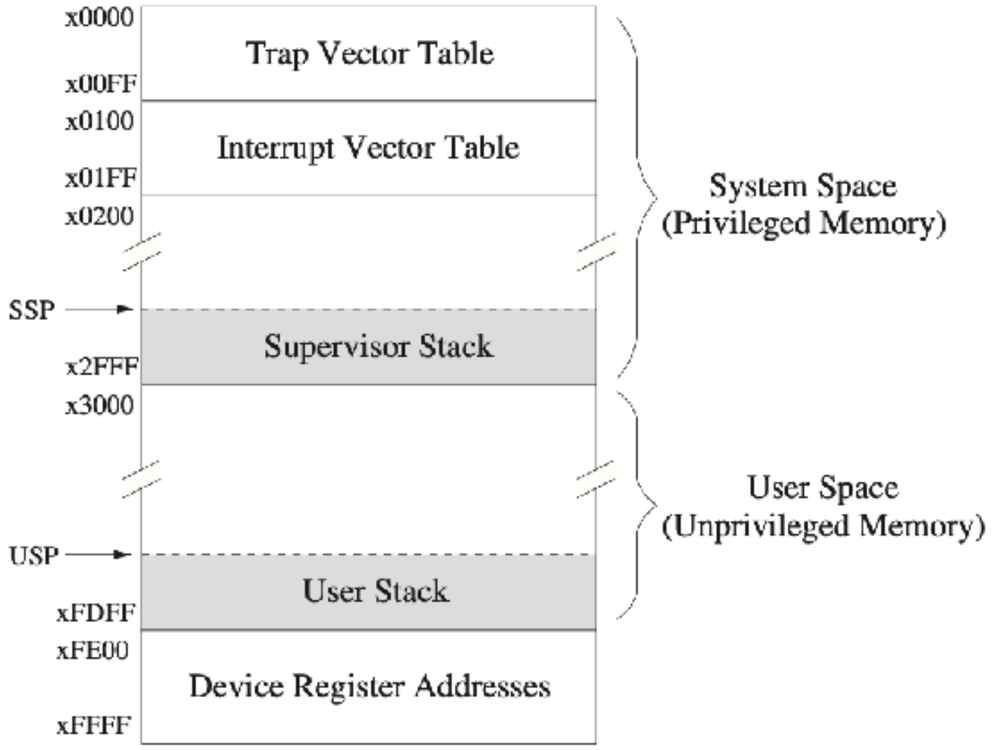

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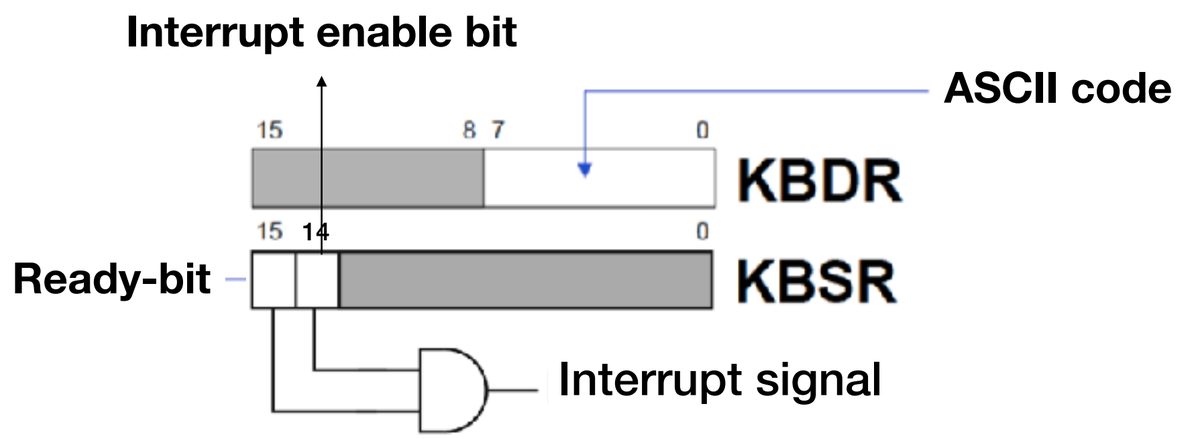

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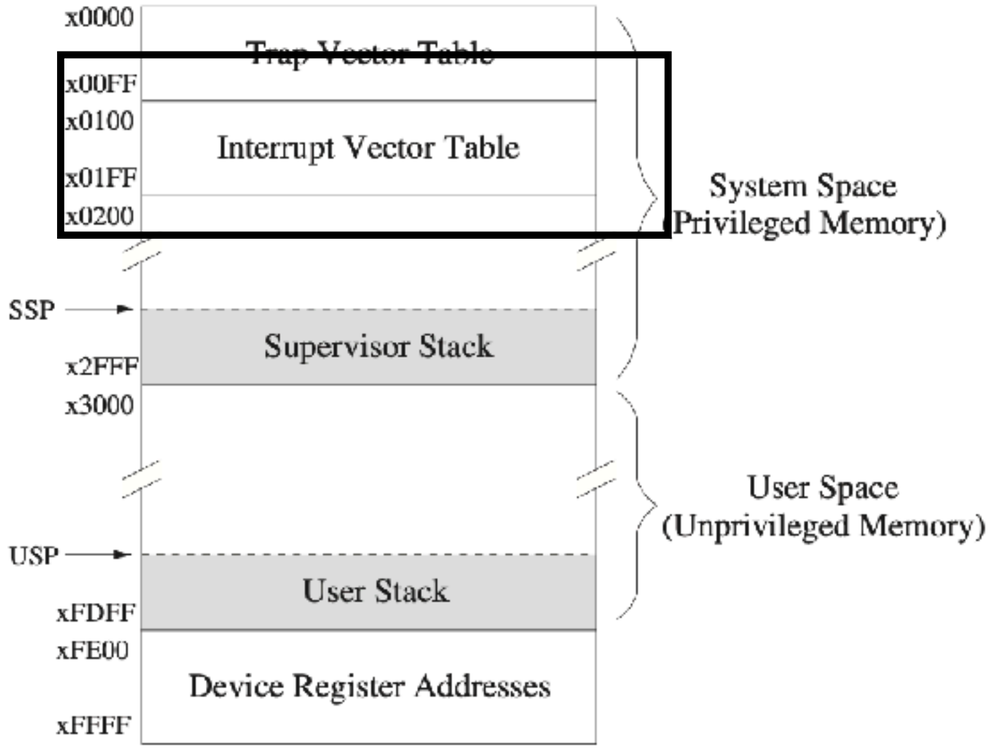

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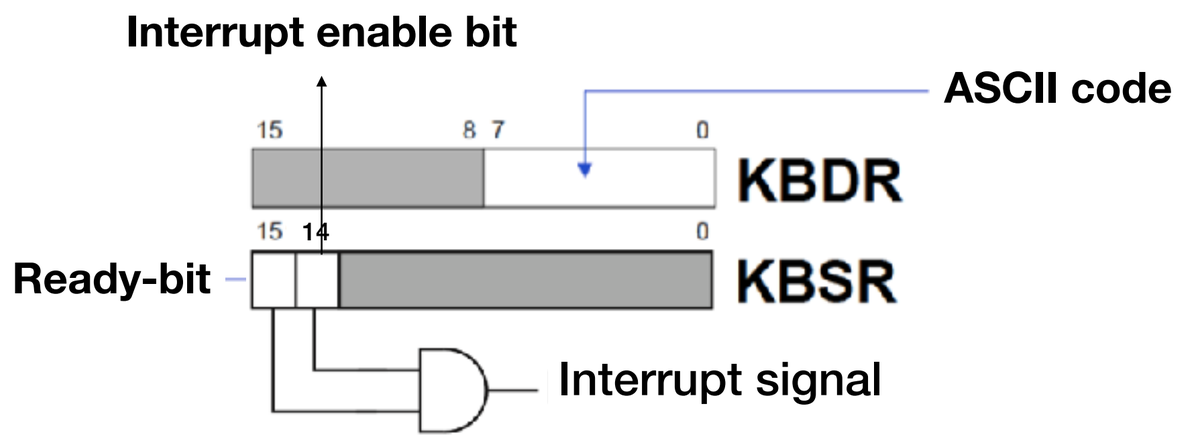

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   - ***Priority levels*:** PL0 < PL1 < … < PL6

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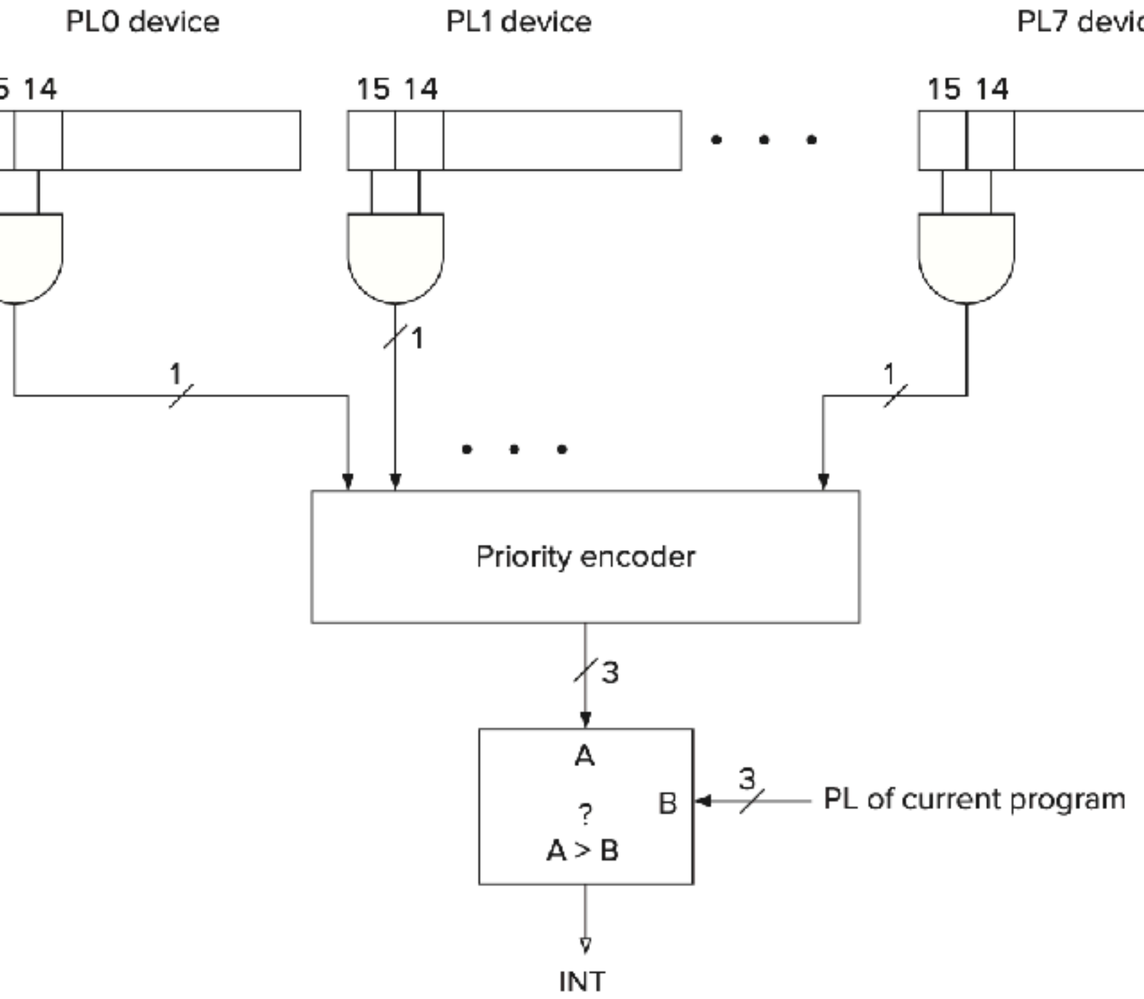

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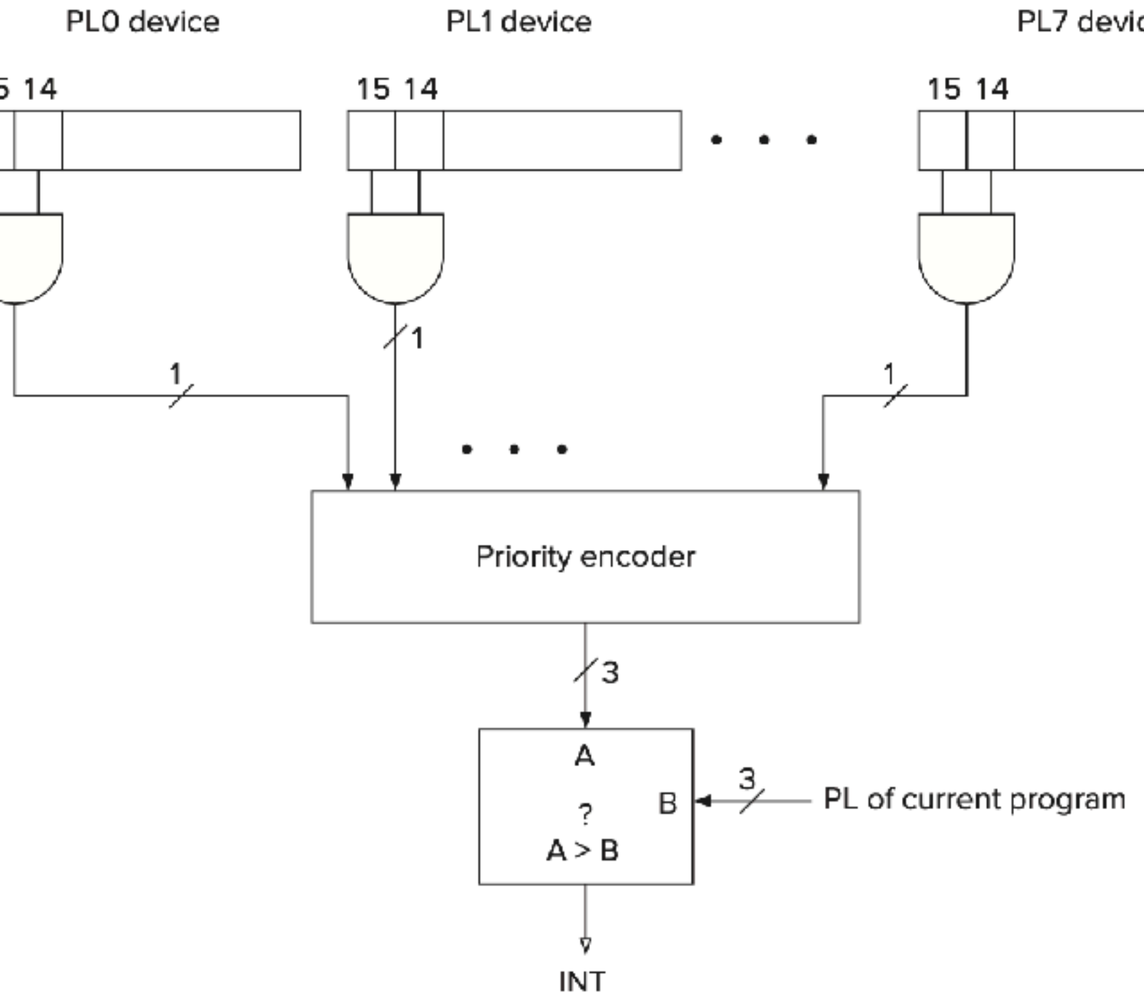

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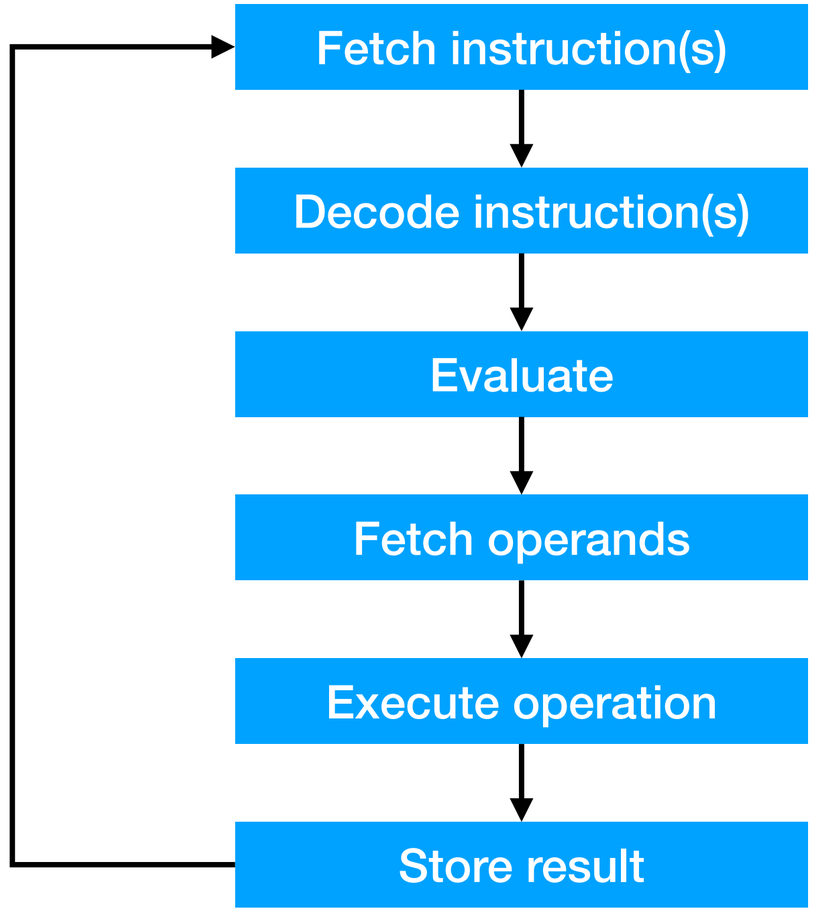

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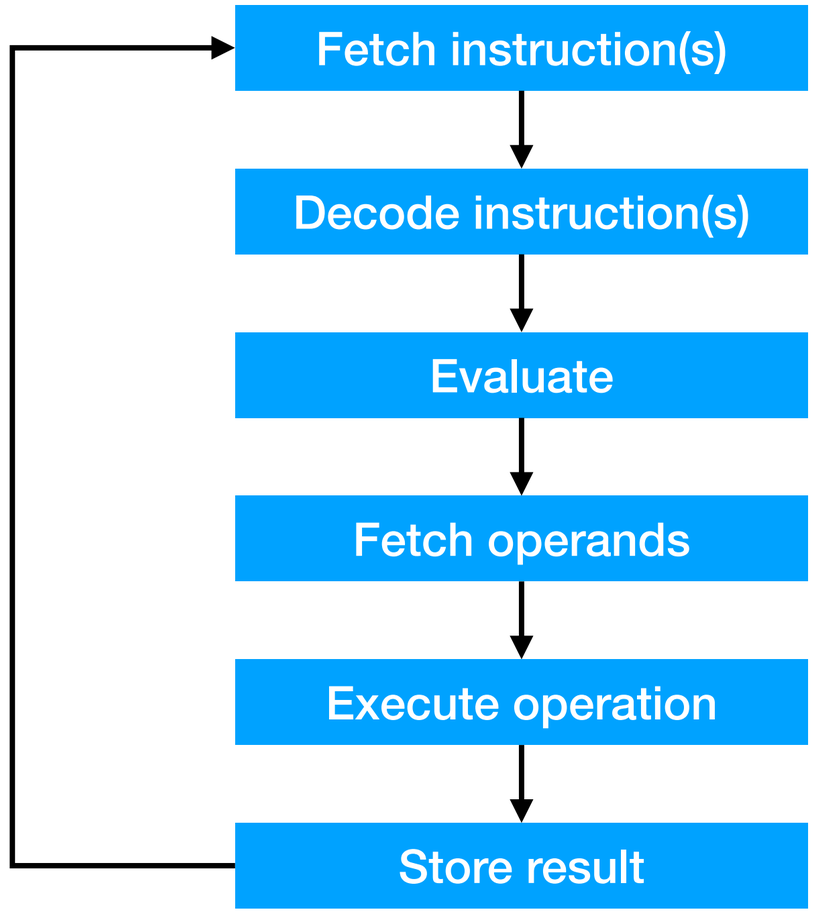

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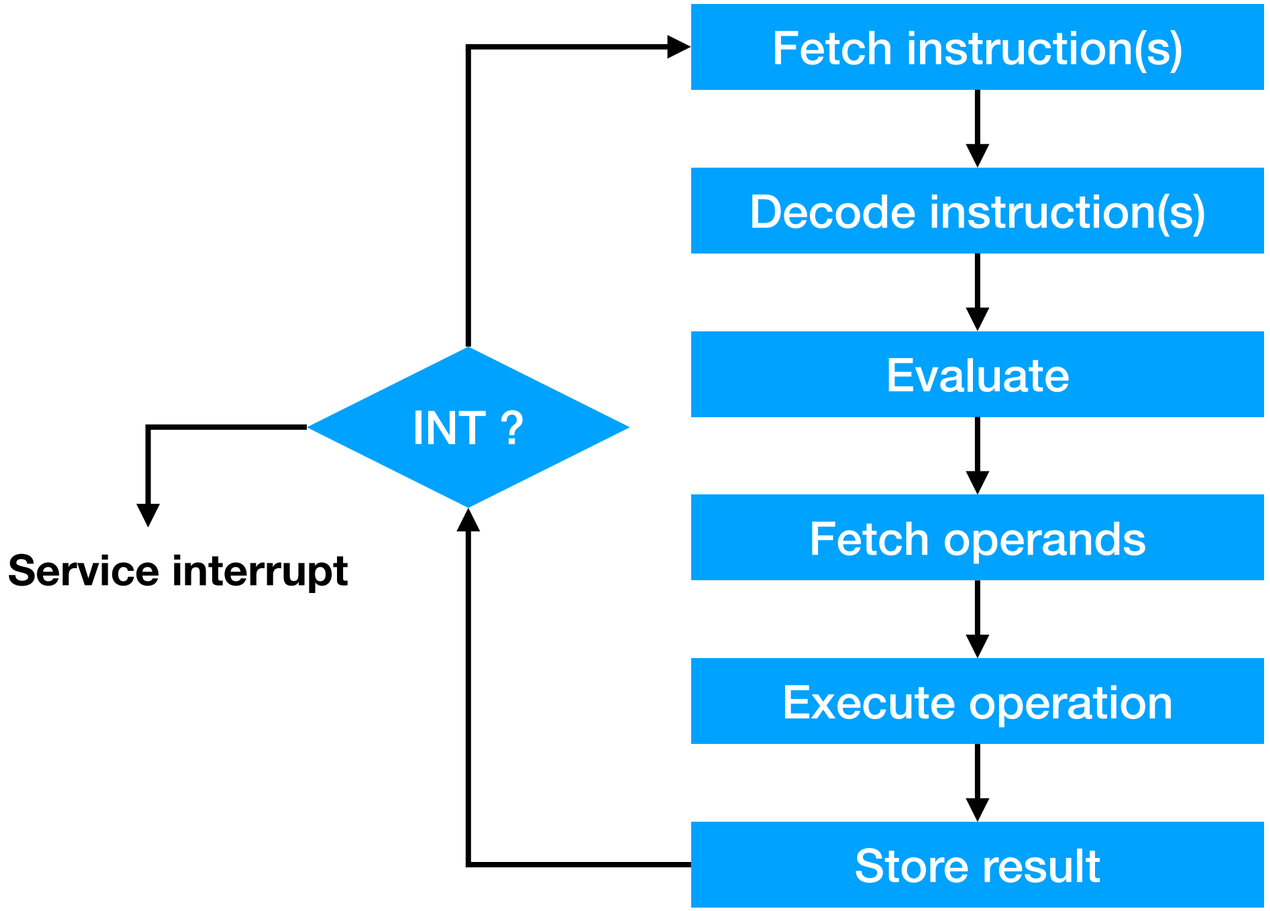

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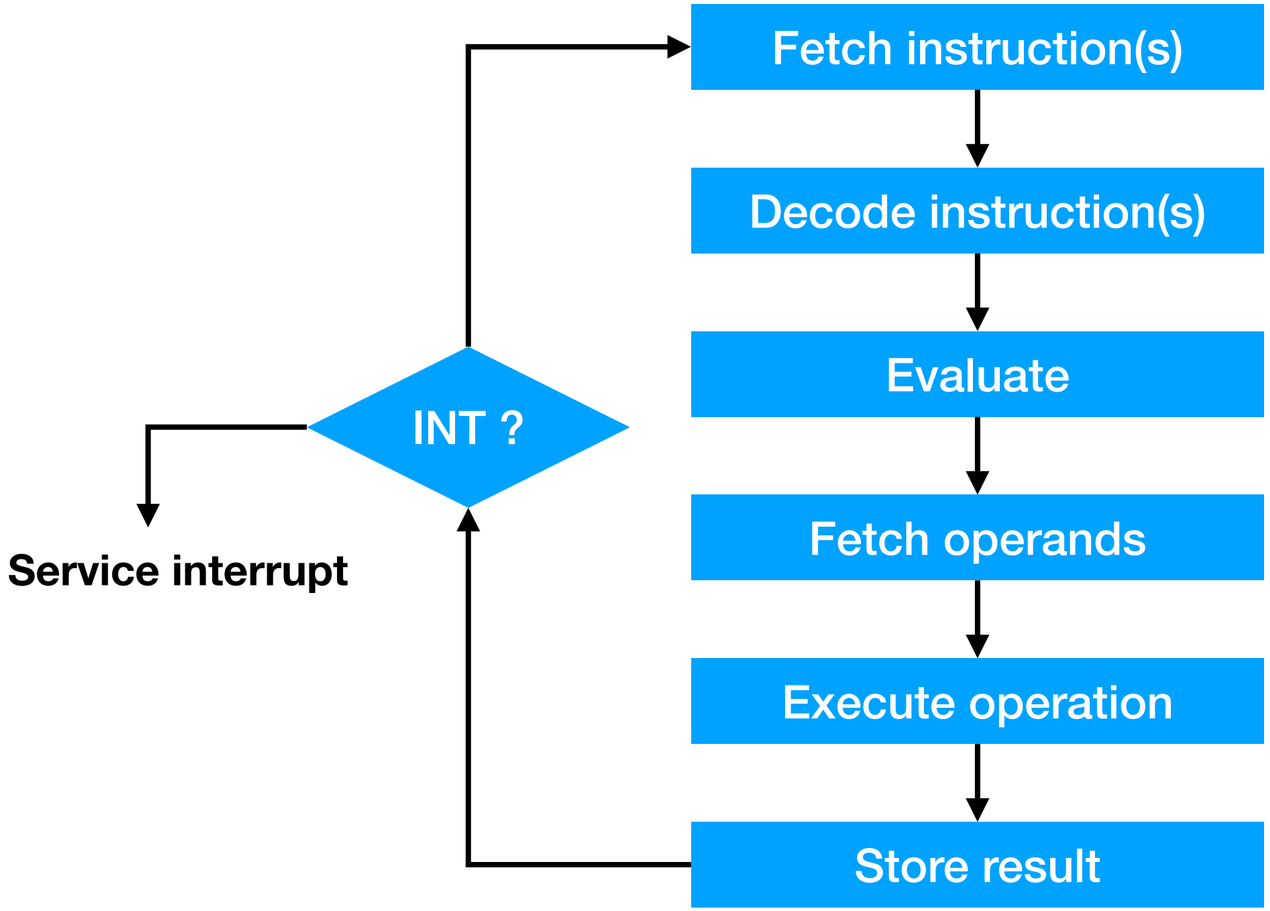

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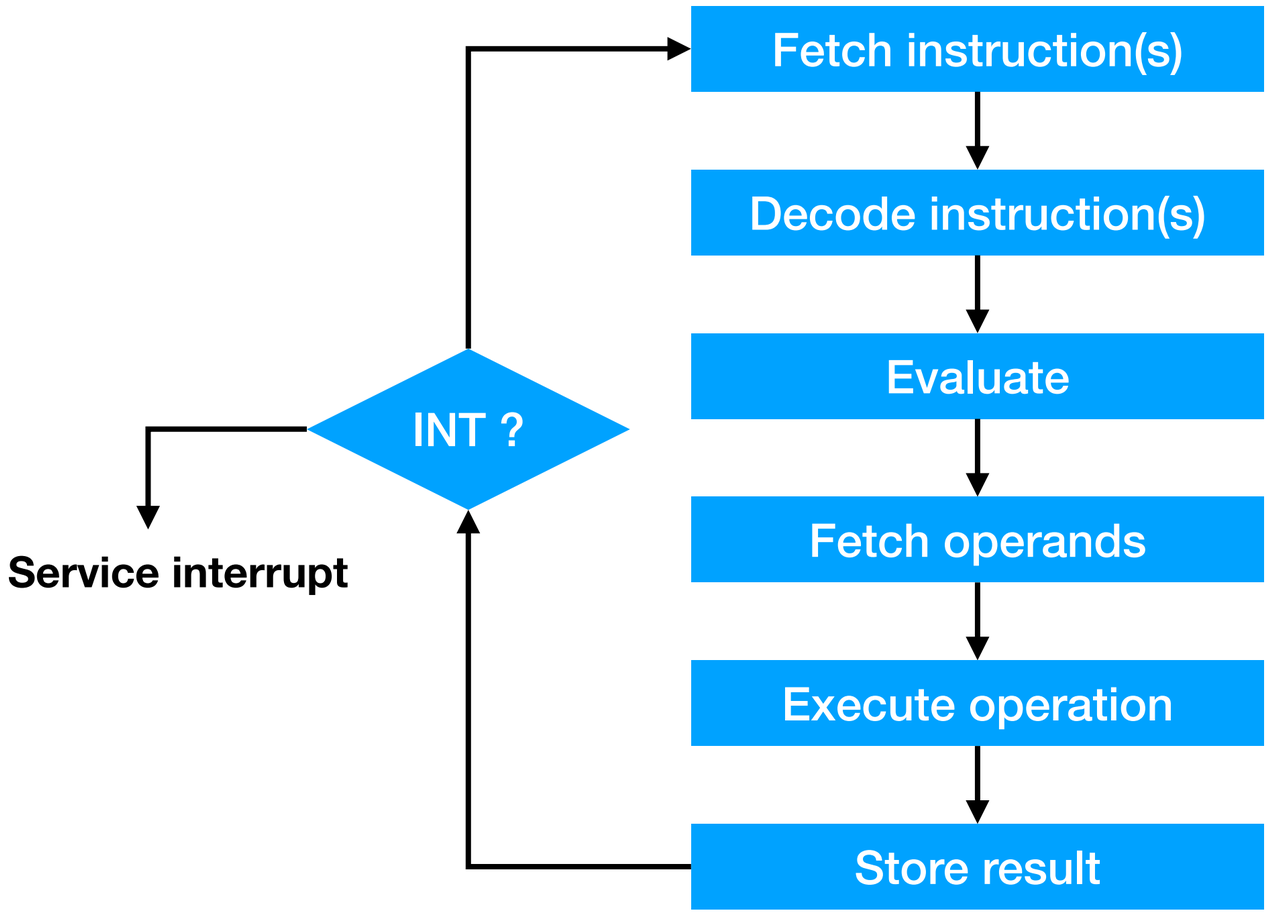

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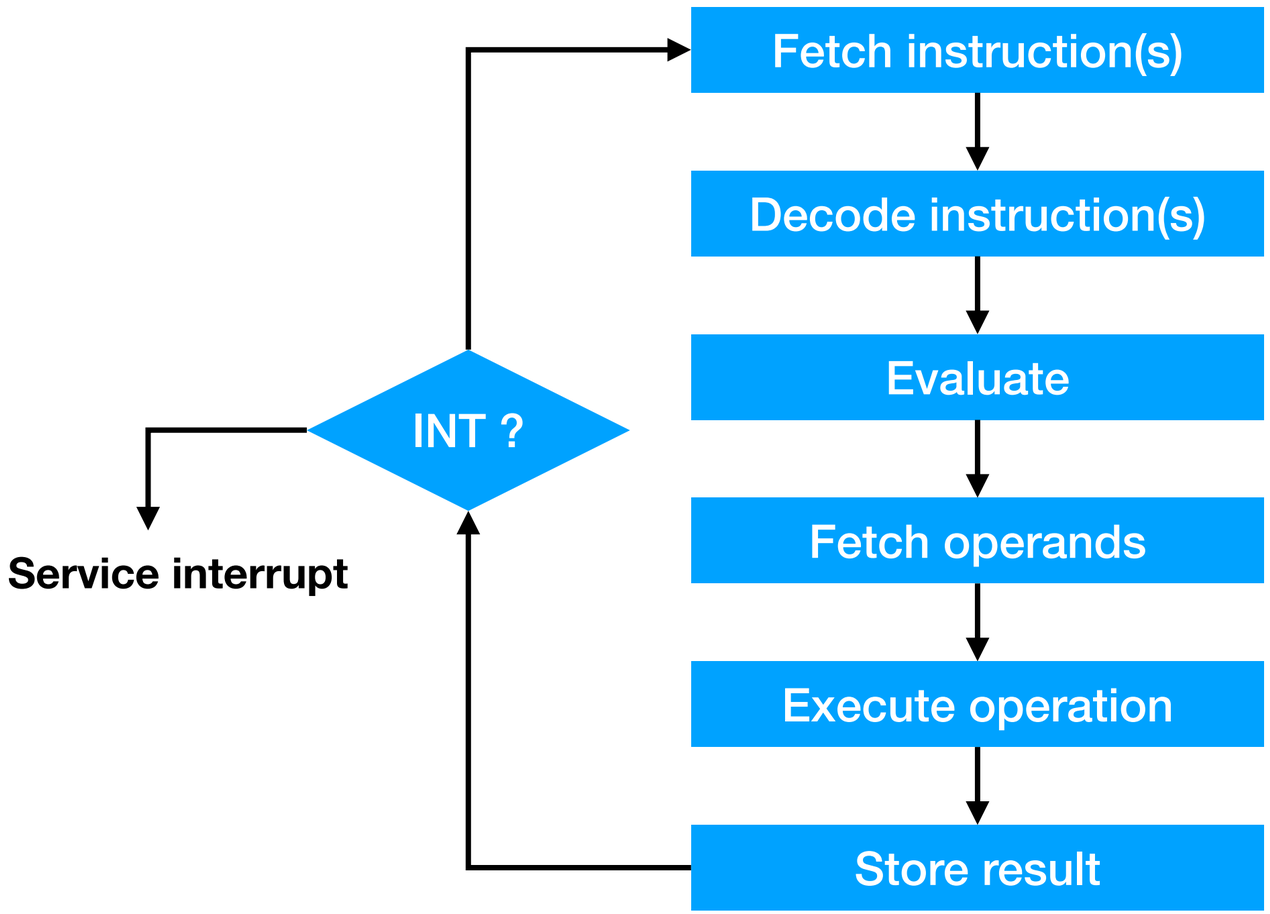

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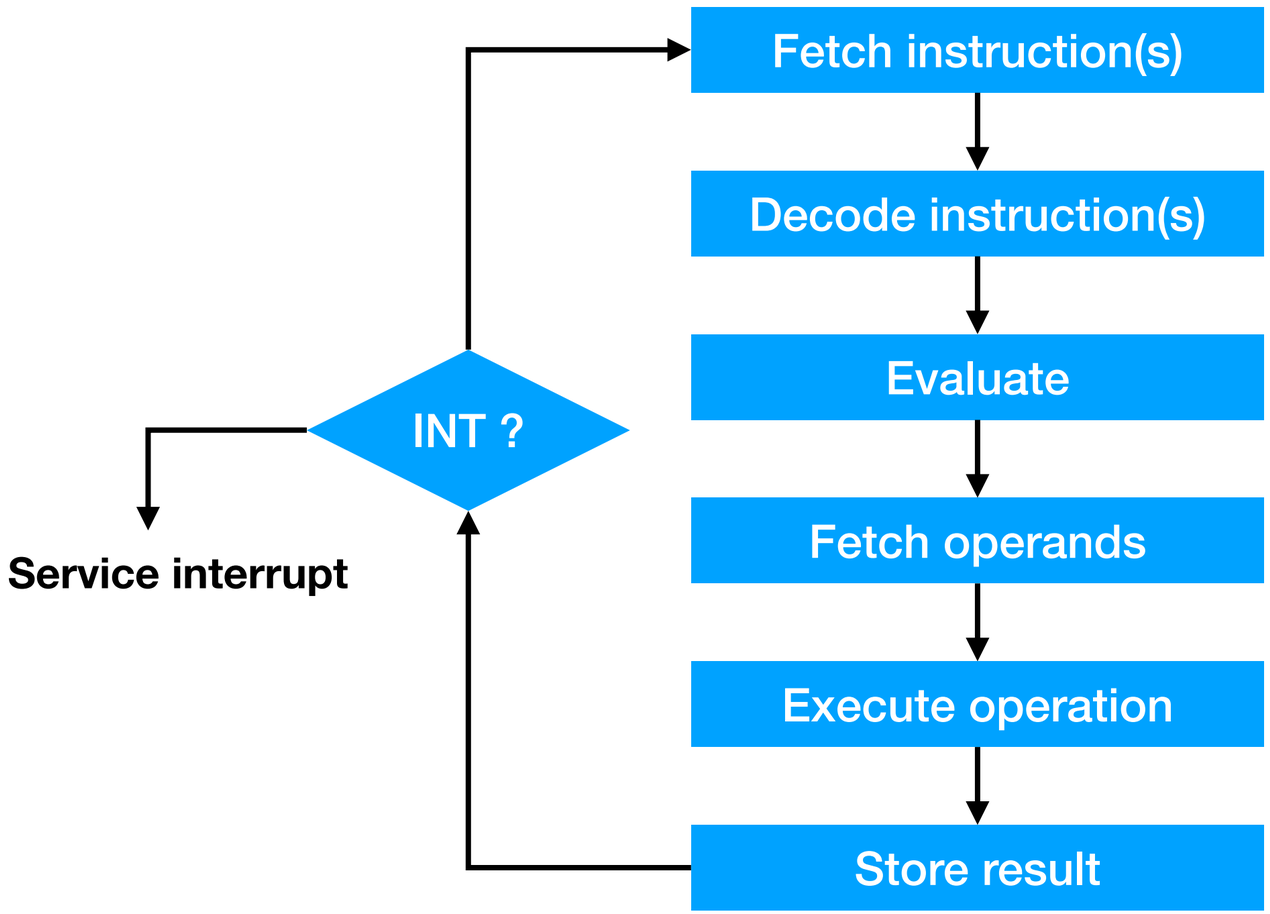
  - resume old process on RTI (coming later)



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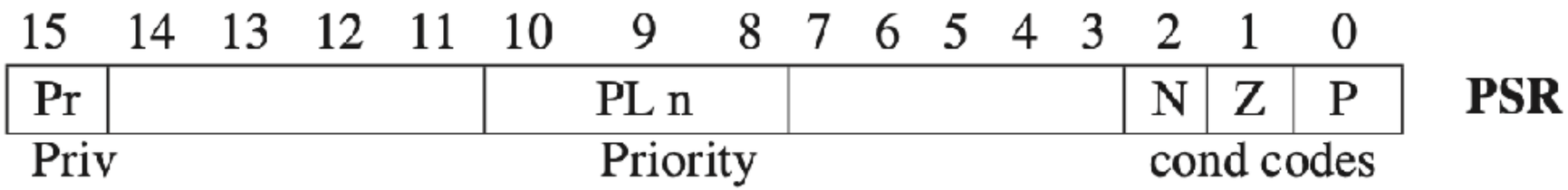

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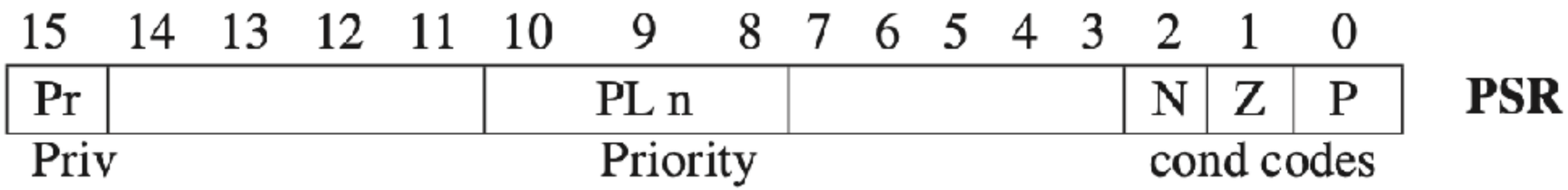

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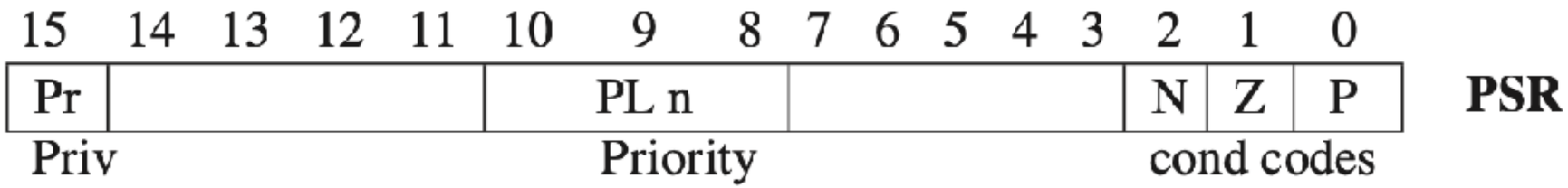

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User stack vs. supervisor stack

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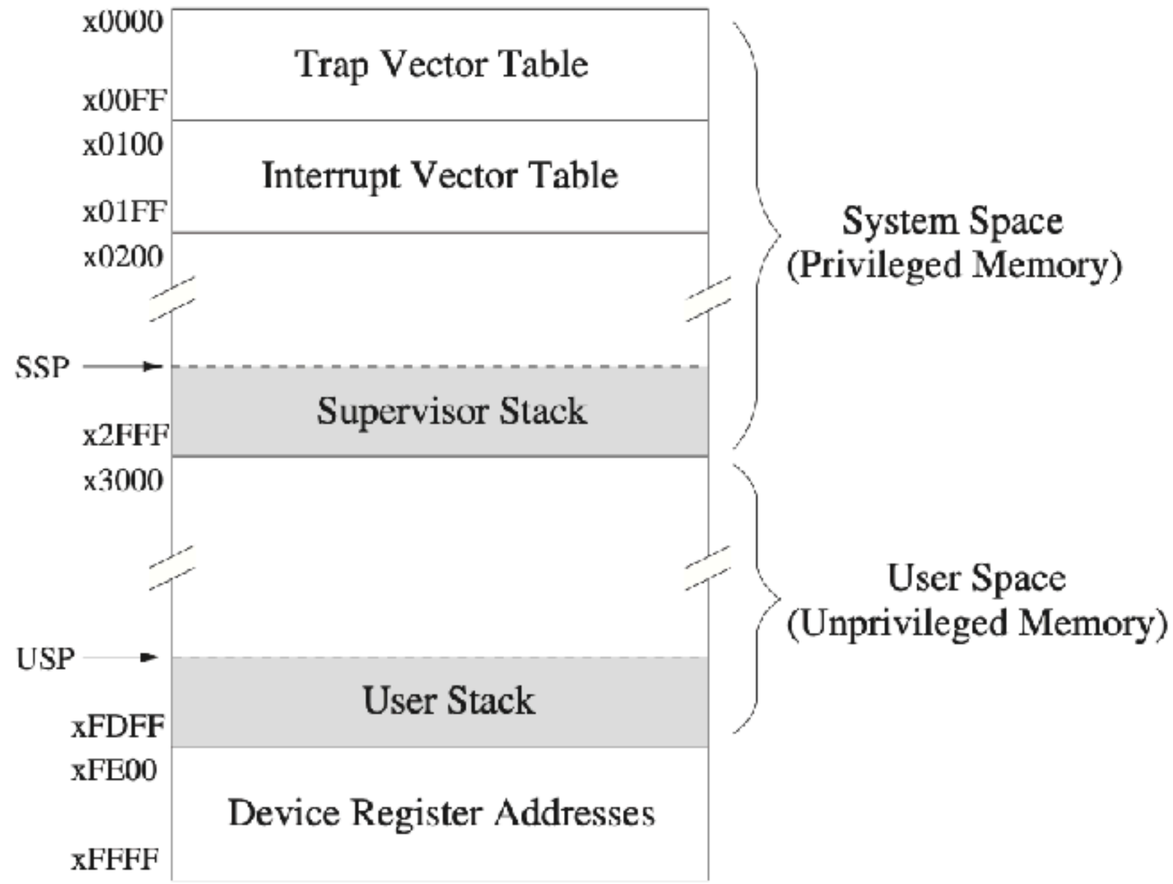

Figure A.1 - P&P 3rd Ed.

User stack vs. supervisor stack

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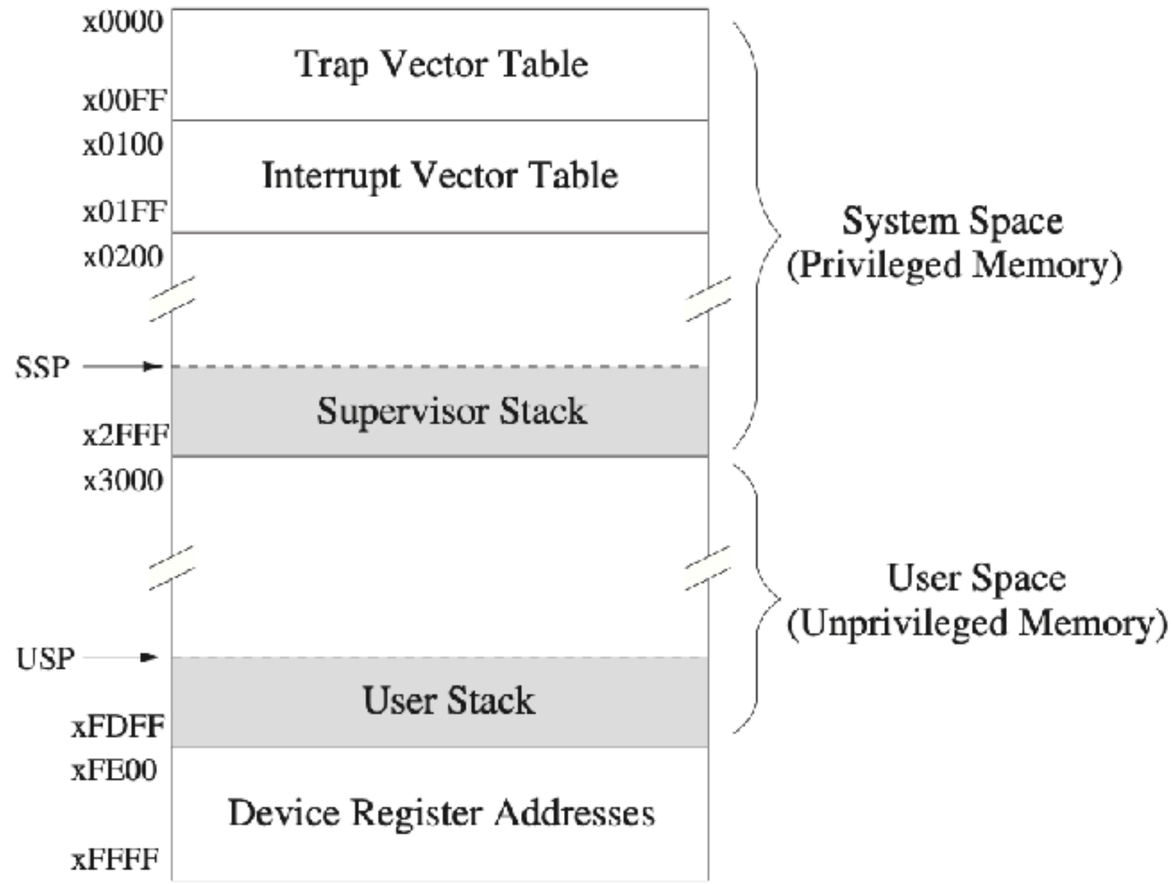

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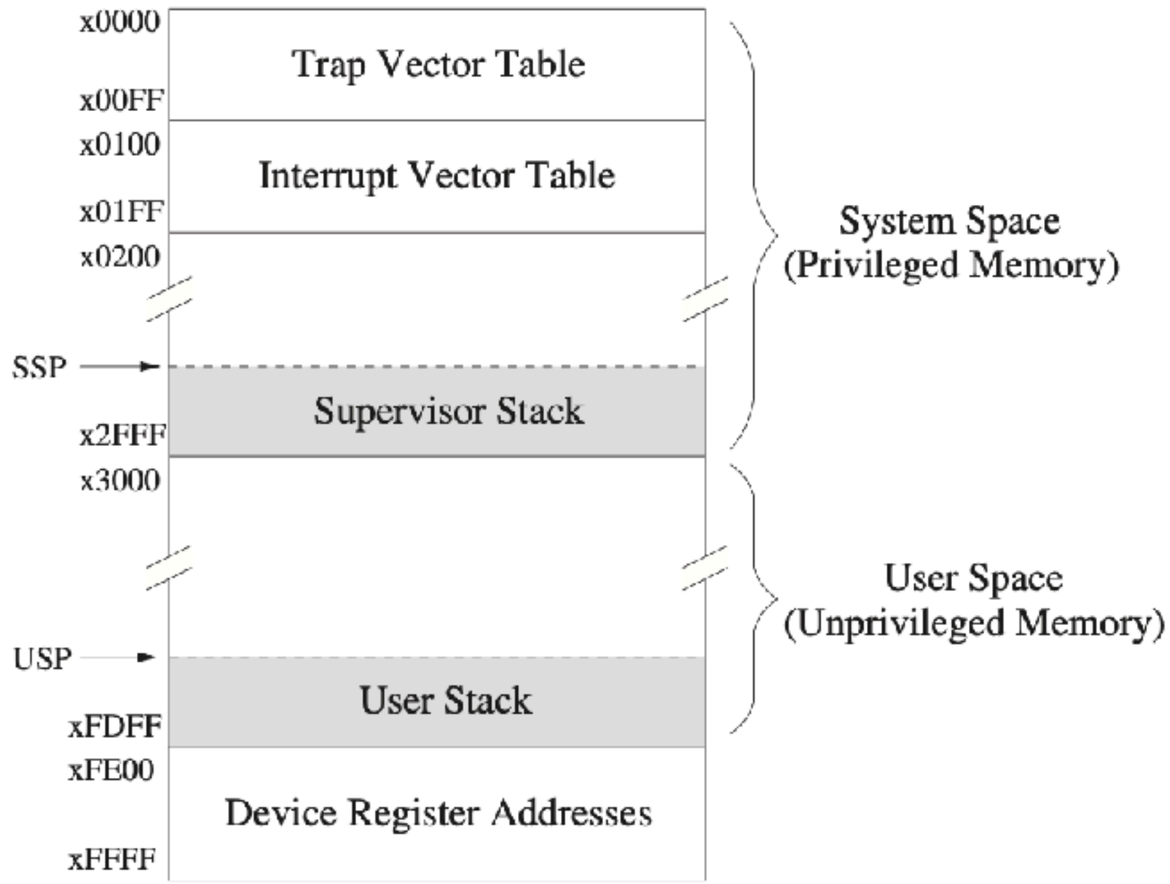

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- Portion of privileged memory reserved for stack in supervisor mode (why?)
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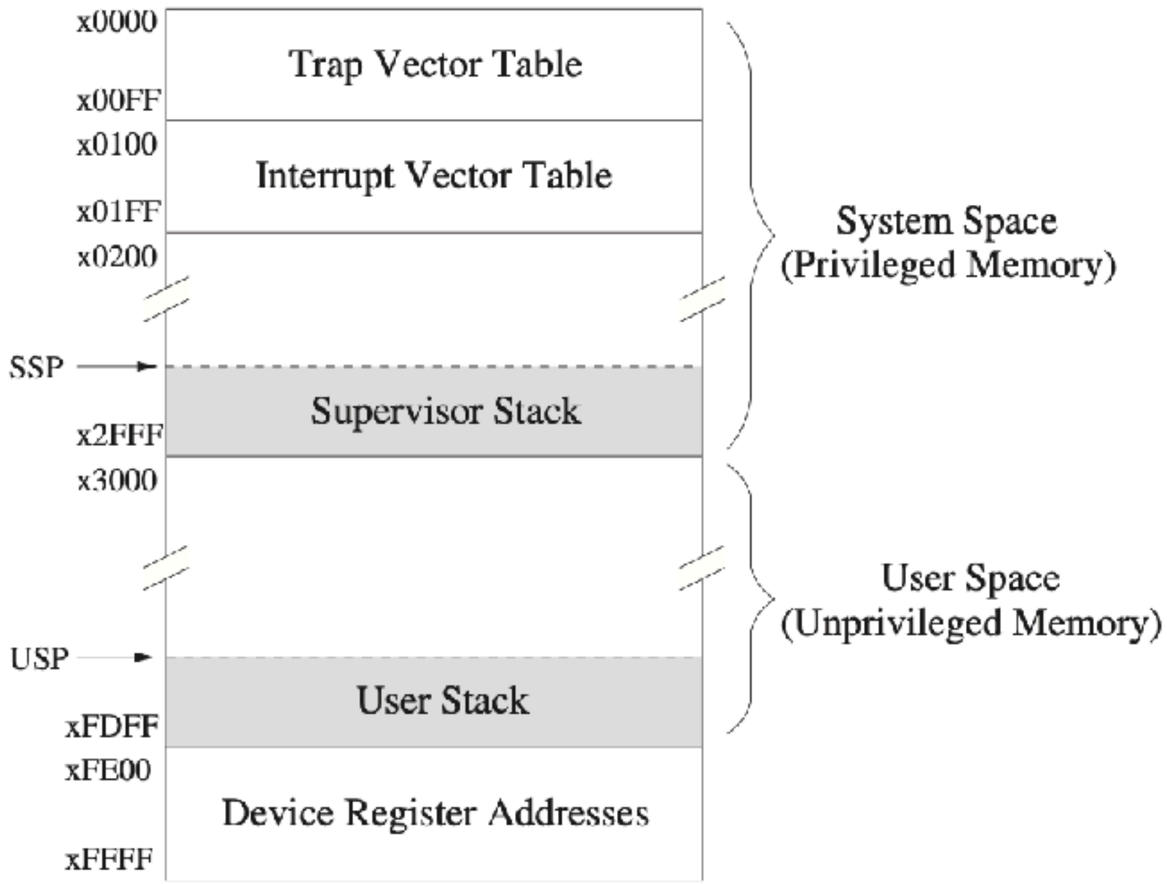
  - Save `R6` on switching modes using (built-in) registers, `Saved_SSP` and `Saved_USP`



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    - Similar to `TRAP` vector table we have seen previously

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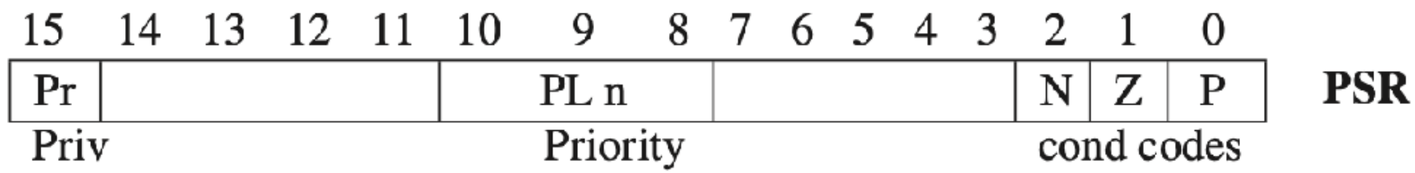

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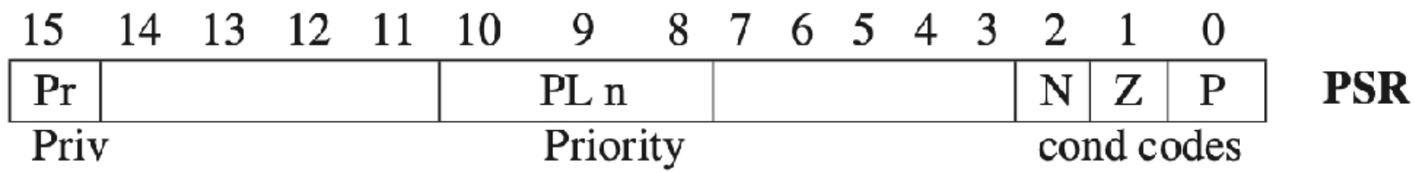

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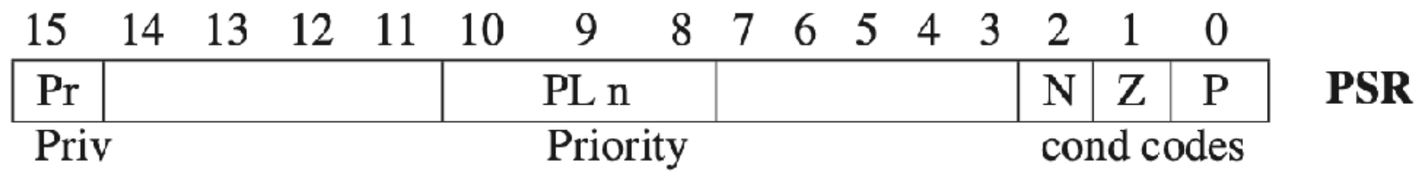

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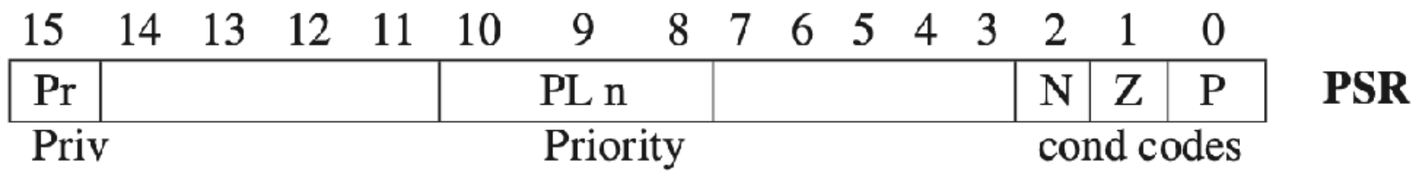

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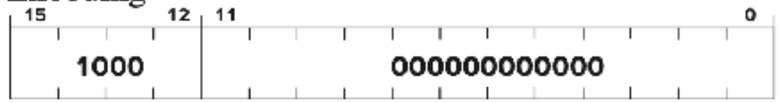
RTI

Return from Trap or Interrupt

Assembler Format

```
RTI
```

Encoding



Operation

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if (PSR[15] == 1)
   Initiate a privilege mode exception;
else
   PC=mem[R6]; R6 is the SSP, PC is restored
   R6=R6+1;
   TEMP=mem[R6];
   R6=R6+1; system stack completes POP before saved PSR is restored
   PSR=TEMP; PSR is restored
   if (PSR[15] == 1)
      Saved_SSP=R6 and R6=Saved_USP;
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If the processor is running in User mode, a privilege mode exception occurs. If in Supervisor mode, the top two elements on the system stack are popped and loaded into PC, PSR. After PSR is restored, if the processor is running in User mode, the SSP is saved in Saved_SSP, and R6 is loaded with Saved_USP.

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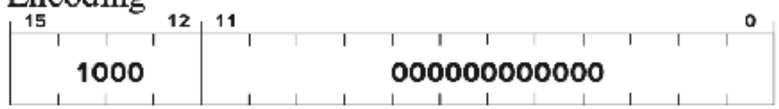

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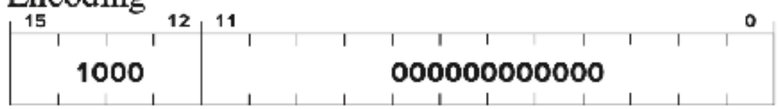

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RTI

Return from Trap or Interrupt

Assembler Format

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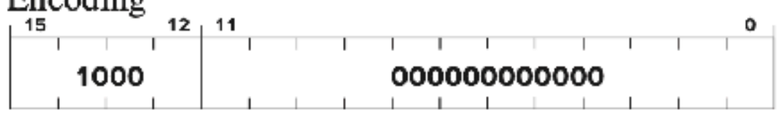

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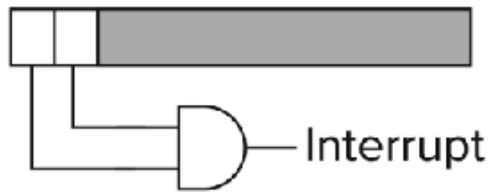

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        LEA     R0, ISR_KB
        STI     R0, KBINTV  ; load ISR address to INTV
        LD      R3, EN_IE
        STI     R3, KBSR    ; set IE bit of KBSR
AGAIN   LD      R0, NUM2
        OUT
        BRnzp   AGAIN
ISR_KB  ST      R0, SaveR0  ; callee-save R0
        LDI     R0, KBDR    ; read a char from KB and clear ready bit
        OUT
        LD      R0, SaveR0  ; callee-restore R0
        HALT
;
EN_IE   .FILL   x4000 ; To enable the IE bit
NUM2    .FILL   x0032 ; ASCII Code for '2'
KBSR    .FILL   xFE00
KBDR    .FILL   xFE02
KBINTV  .FILL   x0180 ; INT vector table address for keyboard
SaveR0  .BLKW   #1
.END
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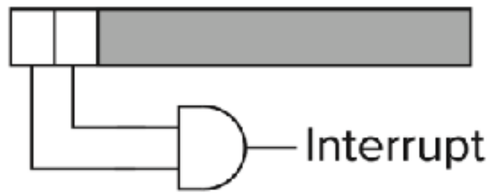

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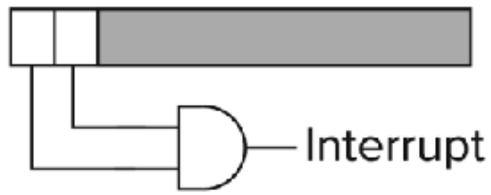

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See Appendix C7 for more details.

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  - Priority level is **not changed.**

Next lecture(s)

- Examples
- Course review: https://surveys.illinois.edu/sec/1742038613
  - So far only C++ and recursion
- Exam preparation tips
- ICES forms