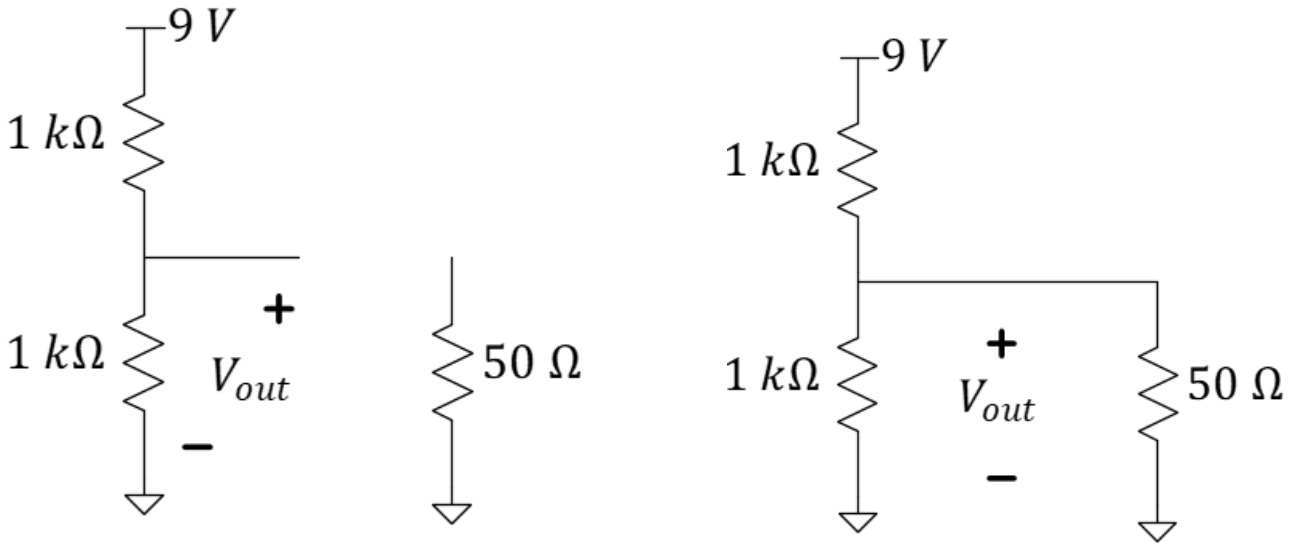
Name:_____ UIN: | | | | | | | | | | Section AB/BB: |

Experiment 8: Coupling *Balance* with *Speed* Control

Laboratory Outline:

We have built several circuits to do specific tasks. Examples include the oscillator to generate a PWM signal and the MOSFET-based motor-drive circuit. We have also learned that a cascade of circuits, a series of sub-circuits combined to achieve a "larger" goal, might require *buffering* elements to prevent loading effects. For example, suppose you want to record the voltage of a voltage divider, but the instrument you plan to use to collect this information has an internal resistance of $50\ \Omega$. Figure 1 explains the issue in some detail.



(a) *(b)*

***Figure 1**: The voltage V_{out} changes from the intended value, $4.5\ V$ in (a) to an unintended value of $0.4\ V$ in (b) due to the lack of an appropriate "buffer" between the voltage divider circuit and the measurement device.*

Notes:

Recall this is why we used an extra inverter after our oscillator to protect the oscillation when connecting it to the voltage divider of the motor-drive circuit (recall Experiment 5, Figure 3).

Other times, an intermediate circuit is required to strategically **combine** or couple two signals. This may involve, for example, simply adding a DC offset to a time-varying signal or merging two digital signals using Boolean-logic principles.

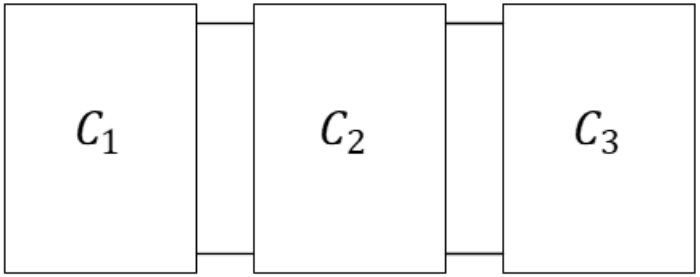


***Figure 2**: Coupling two circuits, C_1 and C_3, often requires the aid of a buffer or other coupling circuit, C_2.*

Today, we will investigate one Boolean logic method of combining two inputs to control a single output. We will be using the logical AND circuit constructed in prelab to combine two signals into a single control signal for each of the two car wheels. The fact that we are dealing with binary (two) voltages only aides us in our task by allowing us to use simpler "logical" circuitry that does not require careful preservation of more-intricate voltage waveforms.

Breakout Session

Consider the circuit schematic of a single button plus its resistor and the battery designed to produce a "logical", two-valued, input as shown in the figure below.

Notes:

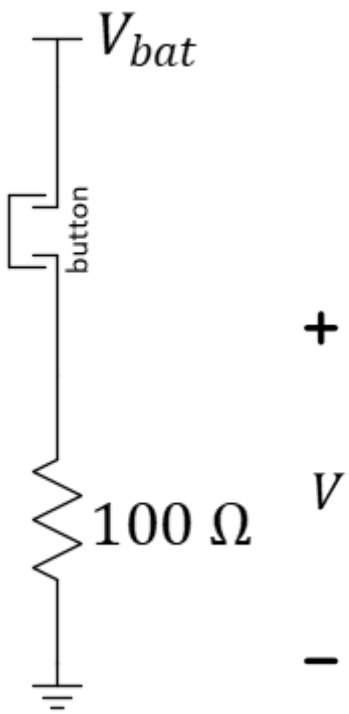


***Figure 3**: An easy circuit to generate a logical input.*

Question 1: Explain, *using KVL, KCL, and/or Ohm's Law circuit theory,* how this button circuit produces a "low" voltage at V when not pressed and a "high" voltage when pressed. Show your circuit solutions.

Now add the $1\ k\Omega$ resistor plus the pushbutton switches to imitate the two inputs. The blue LED should only illuminate when both buttons are pressed.

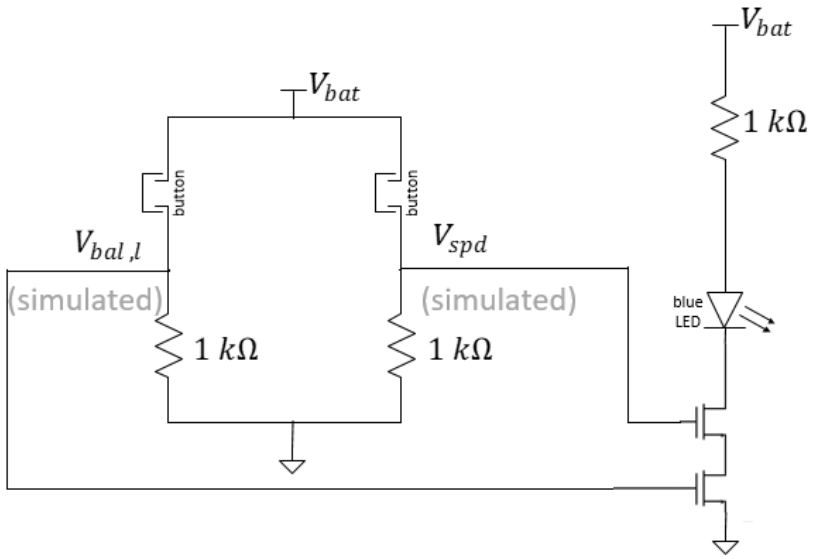
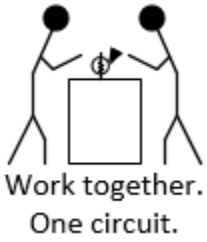


***Figure 4**: Circuit schematic of a two-input logical AND using buttons for inputs.*

Help your peers achieve a working logical-AND circuit as well. Once all of the group's logical-AND circuits are working, show your TA and then you may continue back at your work bench.

At Your Bench



Notes:

If there is only one pushbutton in your kit, it is okay to work with your lab partner and just produce one of these circuits in the breakout session.

Notes:

Modify your motor-control circuit as shown below to include an adjustable wheel-speed balance potentiometer combined with speed control. You should recognize the familiar motor-drive circuits as well as two oscillators and two copies of the logical AND.

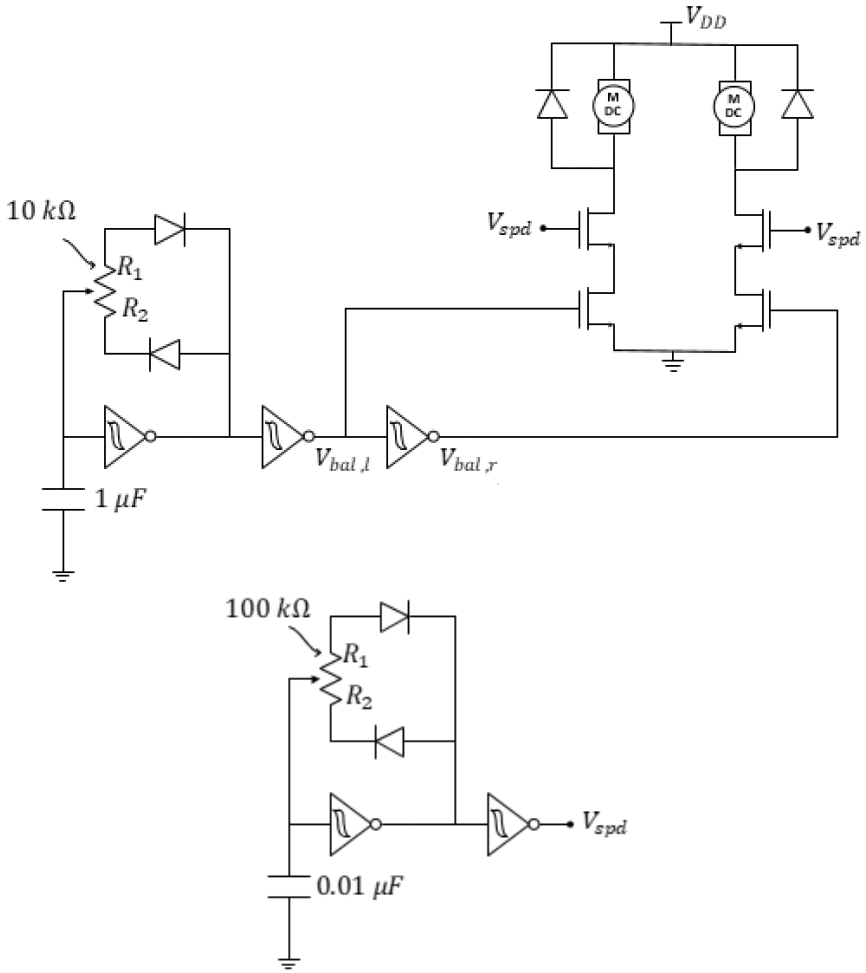


Figure 5: *PWM-based wheel balancer plus speed control. The speed control circuit is drawn separately for clarity, but notice that the nodes labeled* V_{spd} *must all be connected.*

Use the oscilloscope to verify proper oscillation. Set both oscillators to an approximate duty cycle of 50%.

Question 2: Use the oscilloscope to measure the frequency of $V_{bal,l}$. Record that frequency here.

Use the oscilloscope to measure the frequency of V_{spd}. The frequency of V_{spd} should be **8-20 times higher** than the frequency of $V_{bal,l}$. If it is not**, replace the $0.01\ \mu F$ capacitor with something more appropriate from your kit**. When you are satisfied with the frequency of V_{spd}, you may continue.

Question 3: Record the frequency of V_{spd} here.

Mini-Project Modules

Mini-Project modules provide students with options to investigate new concepts! As time allows, do one or more of the modules before returning to the laboratory's core procedure.

This week, we highly recommend the following ***Mini-Project modules:***

***Mini-Project* 8B The Clipping Circuit**	***Mini-Project* 7F: Schmitt Trigger IV**	***Mini-Project* 9B: Voltage-Follower Buffer**

Store your motor-drive circuit in the locker with your car chassis for next week as we complete the autonomous navigation portion of ECE110!

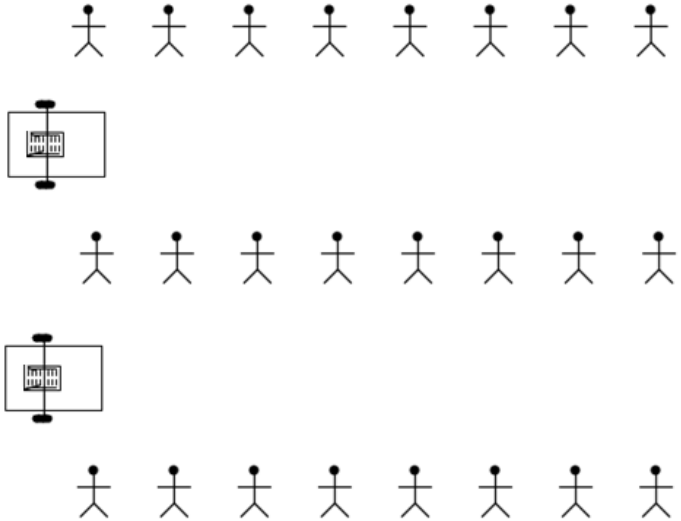
Notes:

Oscilloscope Hint: Please remember to start the oscilloscope from its **default setup** to make it easier to get to the configuration you desire.

Notes:

Breakout Discussion Session

When called back to the breakout, you may race your cars in straight-line paths using the two potentiometers to adjust for both speed and wheel balance.



Learning Objectives

- Deeper skills in building cascaded circuits useful for future design projects.

You are now ready to build a self-navigating vehicle. In the process, you have learned to model devices, predict behavior, build circuits, analyze circuit behavior, measure circuit parameters, and troubleshoot using the oscilloscope as a window into your work.

Lab 8 Summary

Question 4: In the procedure prior to Question 3, *if* the frequency of V_{spd} had been too low, should you have tried a (larger) $0.1\ \mu F$ capacitor or a (smaller) $0.001\ \mu F$ capacitor? Explain.

Question 5: Discuss why the frequencies of V_{bal} and V_{spd} need to be different. In doing so, also discuss what could go wrong if the two frequencies were the same but incoherent. HINT: There are two figures below. The first has V_spd and V_bal with the same frequency, but "in phase" where they are both high around the same time. The logical AND seems to make sense. Now sketch what the output of the logical AND would be when the two signals are "out of synch" as in the bottom diagram...

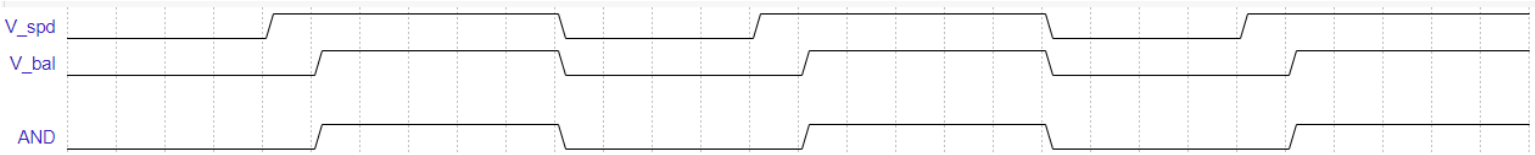


***Figure 4**: The logical AND looks good when V_spd and V_bal are in "in synch".*

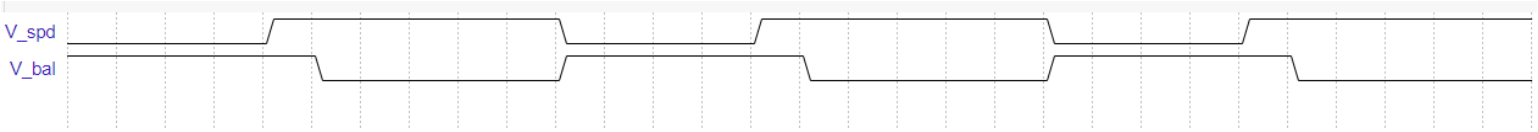


***Figure 5**: Sketch the logical AND when V_spd and V_bal are "out of synch" above.*

Notes:

Return your borrowed equipment, clean up your benchtop, and submit your lab summary before leaving for the day. Thank you!