**ECE 110**
**Professors Brunet and Loui** **October 20, 2008**

# HOUR EXAMINATION #2

**1) Write your official:**
**Last Name (use capital letters):** Solutions (2 versions,
**First Name (use capital letters):**
**NetId & UIN:** one from each professor)

**2) Write your name and section at the *back* of the test**

**DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD**

**Make sure to write your name AGAIN at the top of every page of your exam.**

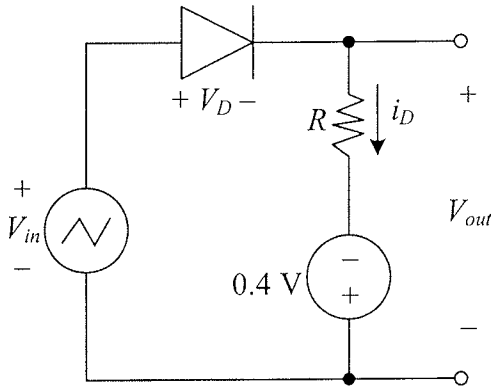
A. Write or print clearly. Answer each problem on the exam itself. If you need extra paper, there is an extra sheet at the end of this exam. Clearly identify the problem number on any additional pages. The Boolean Algebra identities are also attached to the exam.

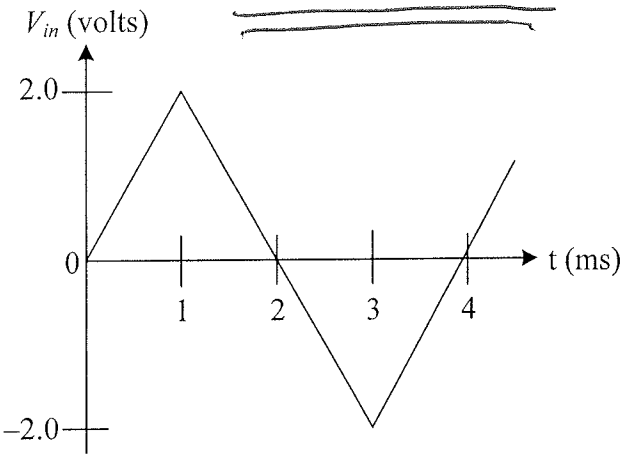
B. In order to receive partial or full credit, **you must show all your work**, e.g., your solution process, the equation(s) that you use, the values of the variables used in the equation(s), etc. **You must also include the unit of measurement in each answer.**

**Students caught cheating on this exam will earn a grade of F for the entire course. Other penalties may include suspension and/or dismissal from the university.**

M.-C. Brunet

**Problem 1** *(20 points)* The circuit below has a sawtooth wave voltage source with period 4 ms, a diode with $V_{on} = 0.6$ V, and a resistor $R = 9$ kΩ. By KVL and Ohm's Law, $V_{in} = V_D + V_{out}$, and $V_{out} = i_D R - 0.4$. To analyze this circuit, use the **large signal model**. $V_D = 0.6$ when ON




**(a)** *[7 pts.]* Express $V_{out}$ in terms of $V_{in}$ when the diode is **on**, and the range of $V_{in}$ when the diode is on. **Show your work.**

- $V_D = V_{ON} = 0.6V \Rightarrow V_{in} = 0.6 + V_{out}$
  $\Rightarrow V_{out} = V_{in} - 0.6$
- check that $i_D > 0$:
  $i_D = (V_{out} + 0.4)/R = V_{in} - 0.6 + 0.4$
  $i_D = \frac{V_{in} - 0.2}{R}$ $i_D > 0$ for $V_{in} > 0.2$

$V_{out} =$ $V_{in} - 0.6$

when $0.2 < V_{in} < \infty$

**(b)** *[7 pts.]* Express $V_{out}$ in terms of $V_{in}$ when the diode is **off**, and the range of $V_{in}$ when the diode is off. **Show your work.**

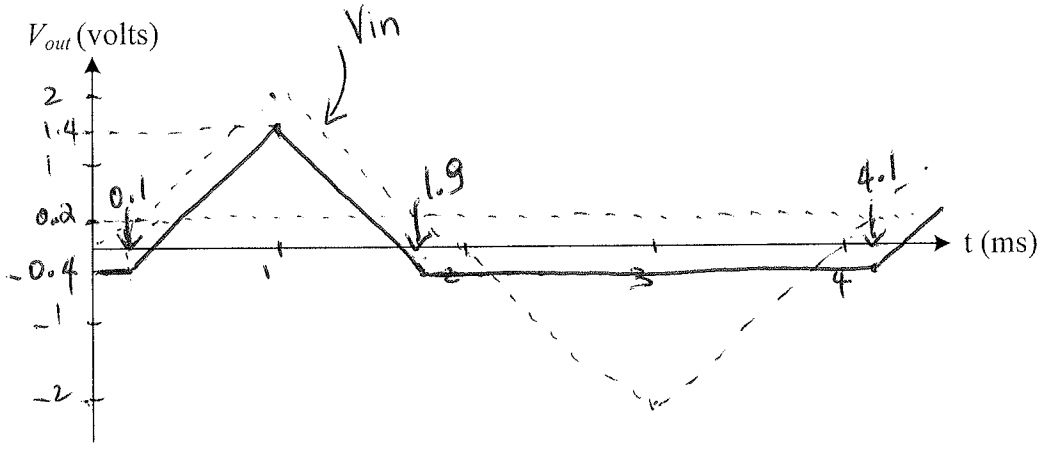
- $i_D = 0 \Rightarrow V_{out} = 0 \times R - 0.4 = -0.4$
- check that $V_D < 0.6$:
  $V_D = V_{in} - V_{out} = V_{in} + 0.4$
  so $V_D < 0.6$ when $V_{in} + 0.4 < 0.6$
  $\Rightarrow$ when $V_{in} < 0.2$

$V_{out} =$ $-0.4$

when $-\infty < V_{in} < 0.2$

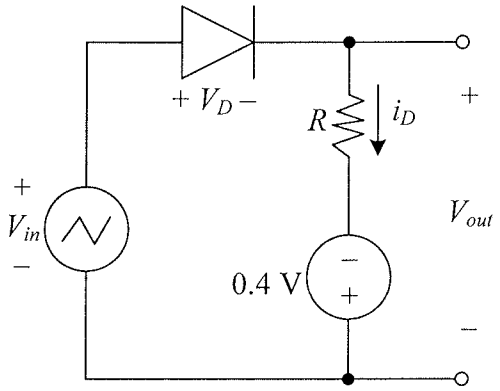
use all these.

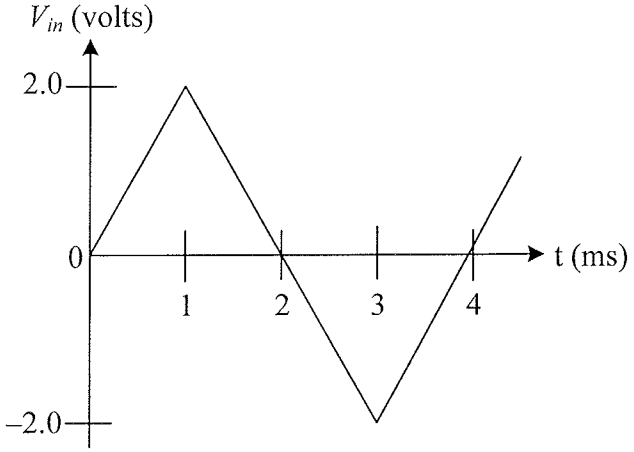
**(c)** *[6 pts.]* Plot the output voltage $V_{out}$ for one period. Label the vertical axis with the voltages, and the horizontal axis with the times at which the behavior of the output changes.



N. Loui

**Problem 1** *(20 points)* The circuit below has a sawtooth wave voltage source with period 4 ms, a diode with $V_{on} = 0.6$ V, and a resistor $R = 9$ kΩ. By KVL and Ohm's Law, $V_{in} = V_D + V_{out}$, and $V_{out} = i_D R - 0.4$. To analyze this circuit, use the **large signal model**.




**(a)** *[7 pts.]* Express $V_{out}$ in terms of $V_{in}$ when the diode is **on**, and the range of $V_{in}$ when the diode is on. **Show your work.**

When the diode is on, $i_D > 0$ and $V_D = V_{on} = 0.6$. Thus

$V_{out} = V_{in} - V_D = V_{in} - 0.6$.

And $i_D = \frac{V_{out} + 0.4}{R} = \frac{V_{in} + 0.4 - 0.6}{R} > 0$

when $V_{in} > 0.6 - 0.4 = 0.2$

$V_{out} =$ $V_{in} - 0.6V$

when $0.2V$ $< V_{in} <$ _____

**(b)** *[7 pts.]* Express $V_{out}$ in terms of $V_{in}$ when the diode is **off**, and the range of $V_{in}$ when the diode is off. **Show your work.**

When the diode is off, $i_D = 0$ and $V_D < V_{on} = 0.6$. So

$V_{out} = i_D R - 0.4 = 0 - 0.4 = -0.4$

And $V_D = V_{in} - V_{out} = V_{in} - (i_D R - 0.4)$

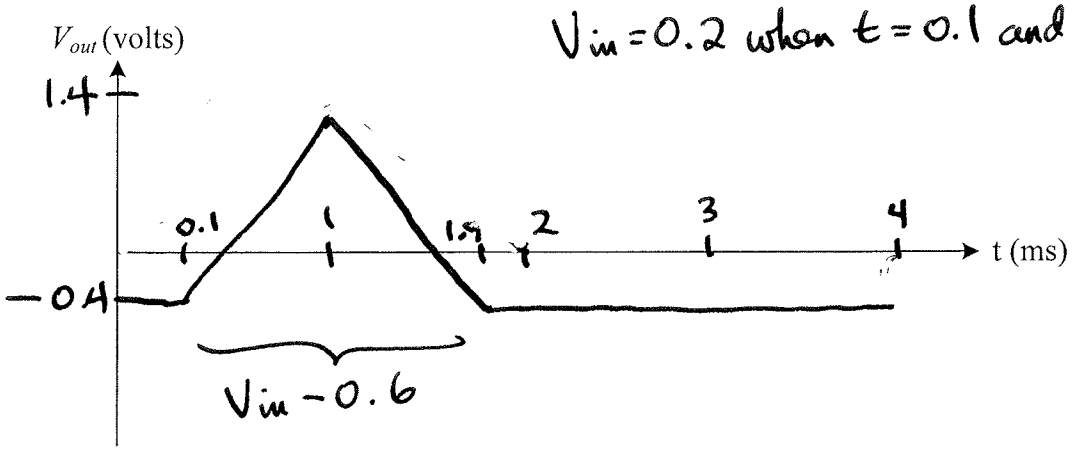
$= V_{in} + 0.4 < 0.6$ when $V_{in} < 0.2$

$V_{out} =$ $-0.4V$

when _____ $< V_{in} <$ $0.2V$

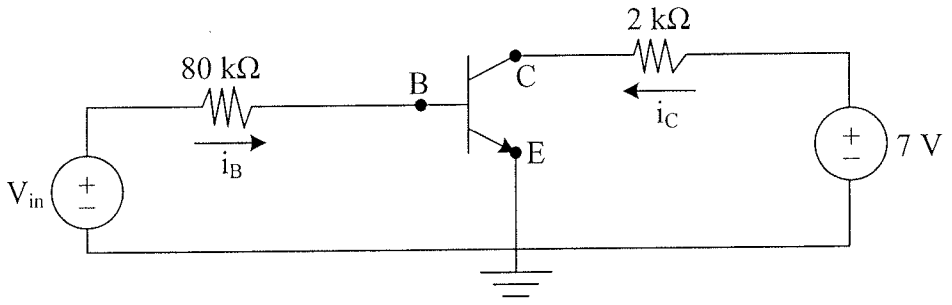
**(c)** *[6 pts.]* Plot the output voltage $V_{out}$ for one period. Label the vertical axis with the voltages, and the horizontal axis with the times at which the behavior of the output changes.

$V_{in} = 0.2$ when $t = 0.1$ and $t = 1.9$



M.-C. Brunet

**Problem 2** *(20 points)*




$V_{BEON} = 0.6$ V; $\beta = 100$; $V_{CESAT} = 0.2$ V

For both parts below, use the information above to find the requested quantities and the transistor state.

**(a)** *[10 pts.]* Assume $V_{in} = 1$ V. **Show your work.**

- since $V_{in} > V_{BEON}$, the transistor is ON - $V_{BE} = V_{BEON}$
  $i_B = \frac{1-0.6}{80k} = \frac{0.4}{80} = 5\mu A$. (or since $i_B > 0$, then it is really ON)
- Assume the transistor is active: $i_C = \beta i_B = 100 \times 5\mu A = 0.5$ mA
  By KVL $V_{CE} = 7 - i_C \times 2k = 7 - 0.5m \times 2k = 6$V
  since $V_{CE} > 0$ ($> V_{CESAT}$) it was correct to assume active.

$i_B =$ 5μA  $i_C =$ 0.5mA  $V_{CE} =$ 6V  State active

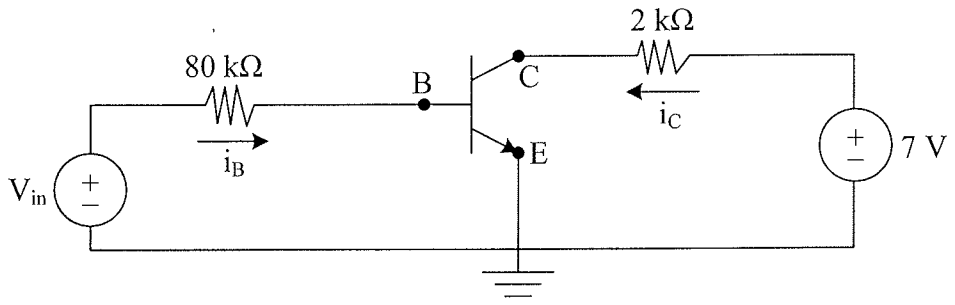
**(b)** *[10 pts.]* Assume $i_C/i_B = 80$. **Show your work.**

- since $i_C/i_B = 80$, this is less than $\beta$ (100)
  ⇒ the transistor must be saturated.
- so $V_{CE} = V_{CESAT} = 0.2$V ; By KVL $i_C = \frac{7-0.2}{2k} = 3.4$mA
- $i_C/i_B = 80 \Rightarrow i_B = i_C/80 = 3.4\text{mA}/80 = 42.5\mu A$

$i_B =$ 42.5μA  $i_C =$ 3.4mA  $V_{CE} =$ 0.2V  State saturated

M. Lowi

**Problem 2** *(20 points)*




$V_{BEON} = 0.6$ V; $\beta = 100$; $V_{CESAT} = 0.2$ V

For both parts below, use the information above to find the requested quantities and the transistor state.

**(a)** *[10 pts.]* Assume $V_{in} = 1$ V. **Show your work.**

By KVL and Ohm's Law, $(2k)\,i_C + V_{CE} = 7$, $V_{in} = (80k)\,i_B + V_{BE}$.

Since $V_{in} > V_{BEon}$, the transistor is active or saturated.

$$i_B = \frac{V_{in} - V_{BEon}}{(80k)} = \frac{1 - 0.6}{(80k)} = \frac{0.4\,V}{80\,k\Omega} = 5\,\mu A$$

If active, $i_C = 100\,i_B = 100 \times 5\,\mu A = 0.5\,mA$

$$V_{CE} = 7 - (2k)\,i_C = 7 - (2k\Omega)(0.5\,mA) = 6V < V_{CESAT}$$

$i_B =$ 5 μA  $i_C =$ 0.5 mA  $V_{CE} =$ 6V  State: active

**(b)** *[10 pts.]* Assume $i_C/i_B = 80$. **Show your work.**

Since $i_C/i_B = 80 < \beta$, the transistor must be saturated.

So $V_{CE} = V_{CESAT} = 0.2\,V$

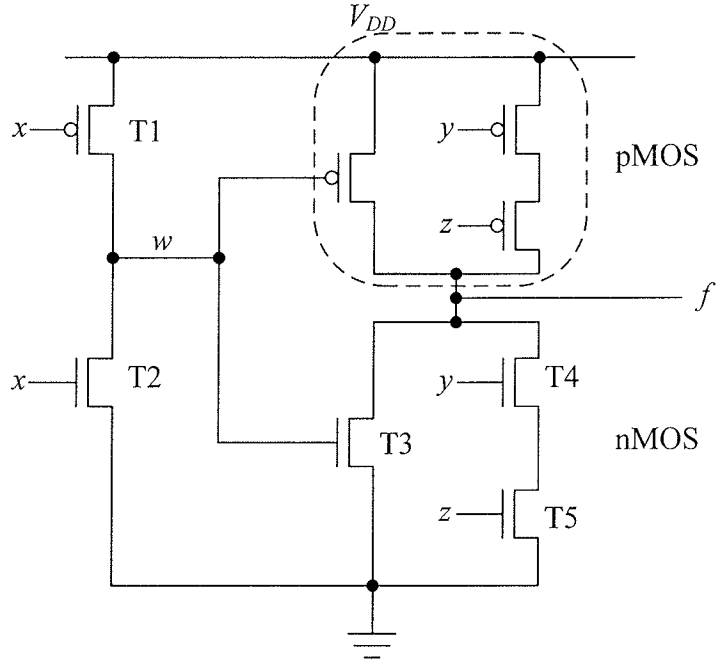
$$i_C = \frac{7 - V_{CE}}{(2k)} = \frac{7 - 0.2}{(2k)} = \frac{6.8\,V}{2k\Omega} = 3.4\,mA$$

$$i_B = \frac{i_C}{(80k)} = \frac{3.4\,mA}{80\,k\Omega} = 42.5\,\mu A$$

$i_B =$ 42.5 μA  $i_C =$ 3.4 mA  $V_{CE} =$ 0.2V  State: saturated

M.-C. Brunet

**Problem 3** *(20 points)* In the CMOS circuit below, the nMOS part is correct, but the enclosed pMOS part is incorrect.




| x | y | z | w | f |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | {not defined (0 with correct) |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | {not defined (0 with correct) |

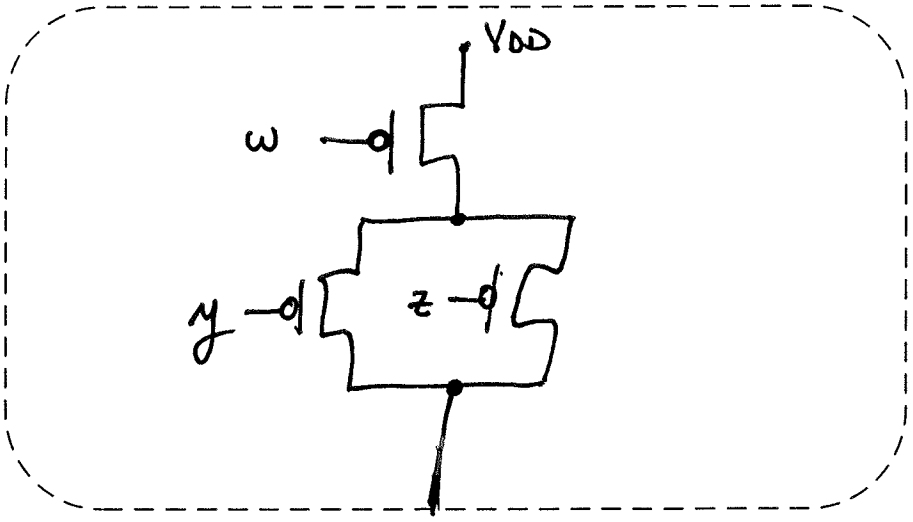
**(a)** *[8 pts.]* Complete the truth table for the value of *f*.

**(b)** *[4 pts.]* Explain **in words** how the table for *w* was obtained.

*w* is high (1) when x is low (0) because T1 is ON & T2 is OFF

*w* is low (0) when x is high (1) because T1 is OFF & T2 is ON

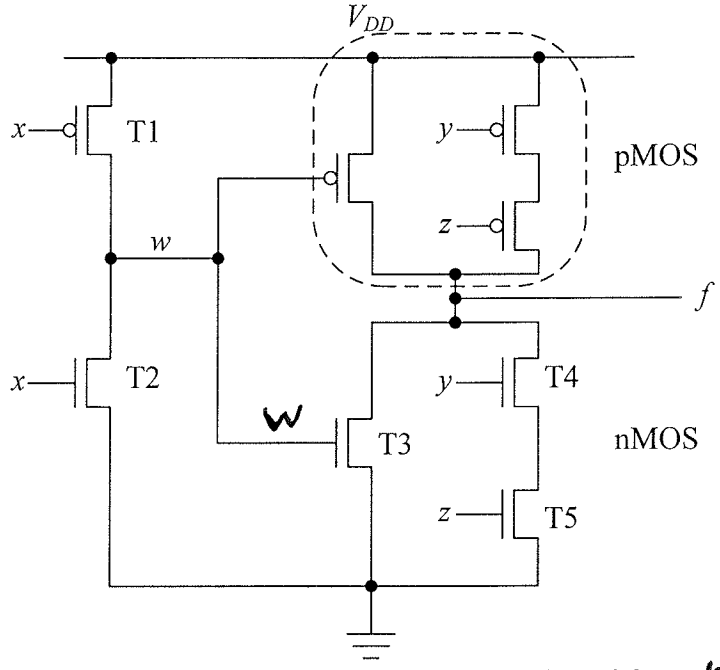
**(c)** *[8 pts.]* Draw the correct pMOS portion of the circuit that corresponds to the nMOS portion. Label the inputs *w*, *y*, and *z* clearly.



M. Loui

(a) From the nMOS part, f = low (0) when w = 1 or y = z = 1

**Problem 3** *(20 points)* In the CMOS circuit below, the nMOS part is correct, but the enclosed pMOS part is incorrect.




| x | y | z | w | f |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |

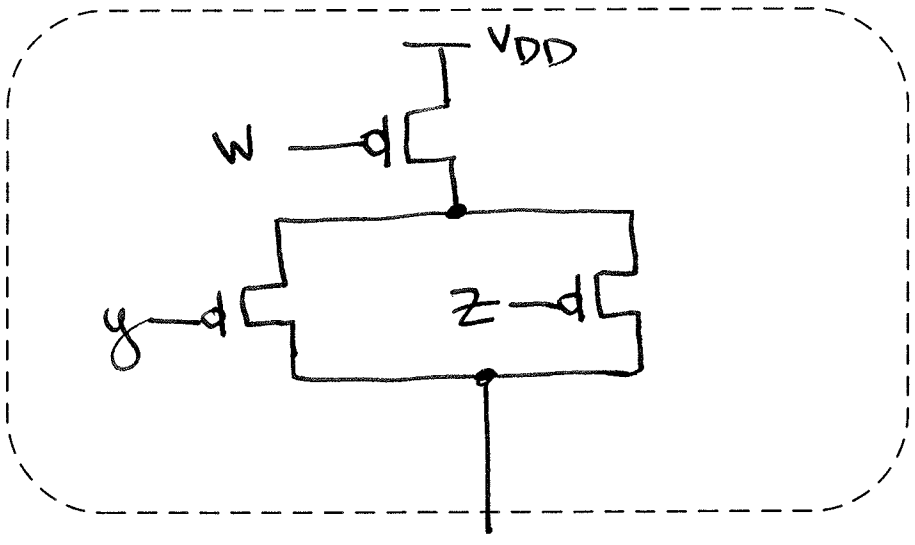
**(a)** *[8 pts.]* Complete the truth table for the value of *f* — after the pMOS part has been corrected (as in part (c) below)

**(b)** *[4 pts.]* Explain **in words** how the table for *w* was obtained.

*w* is high (1) when x is low (0) because T1 is on and T2 is off, so W is connected to $V_{DD}$ = high

*w* is low (0) when x is high (1) because T1 is off and T2 is on, so W is connected to ground (low)

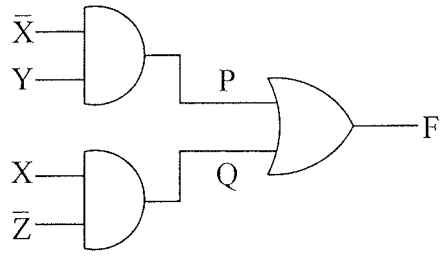
**(c)** *[8 pts.]* Draw the correct pMOS portion of the circuit that corresponds to the nMOS portion. Label the inputs *w*, *y*, and *z* clearly.



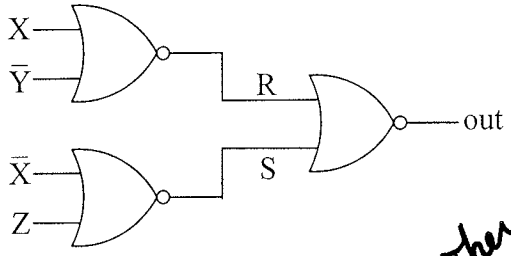

f = high (1) when W = 0 and either y = 0 or z = 0

M.-C. Brunet

**Problem 4** *(10 points)*



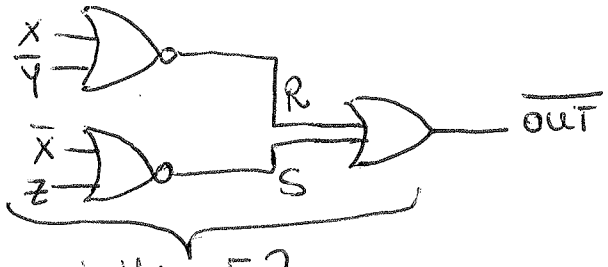

Can $\bar{F}$ (not F) be implemented with the circuit:




note: There are many different ways (Truth table for $\bar{F}$, Br out) (Boolean identities)

☒ Yes ☐ No

**Clearly** and **fully** justify your answer (write neatly):




is this $\bar{F}$?

So we need to prove that $R = P$ and $S = Q$.

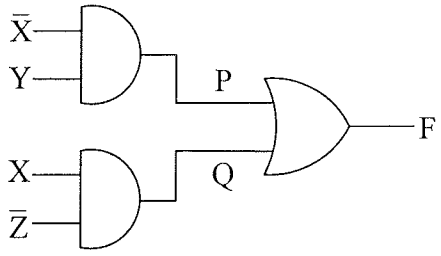


(exactly same for $S = Q$)

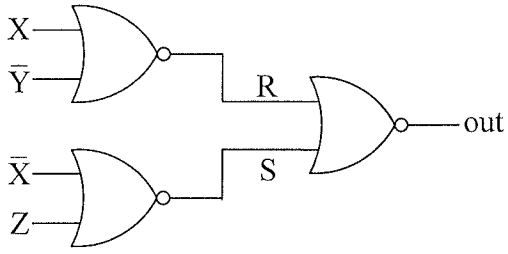
So $R = P$ and $S = Q$ and therefore $\bar{F} = \overline{out}$ indeed.

M. Lolli

**Problem 4** *(10 points)*




Can $\bar{F}$ (not F) be implemented with the circuit:




☑ Yes ☐ No

**Clearly** and **fully** justify your answer (write neatly):

$F = \bar{x}y + x\bar{z}$

$\bar{F} = \overline{(\bar{x}y + x\bar{z})} = \overline{(\bar{x}y)} \cdot \overline{(x\bar{z})}$ by DeMorgan

$= (\bar{\bar{x}} + \bar{y})(\bar{x} + \bar{\bar{z}})$ by DeMorgan again

$= (x + \bar{y})(\bar{x} + z)$ by Involution

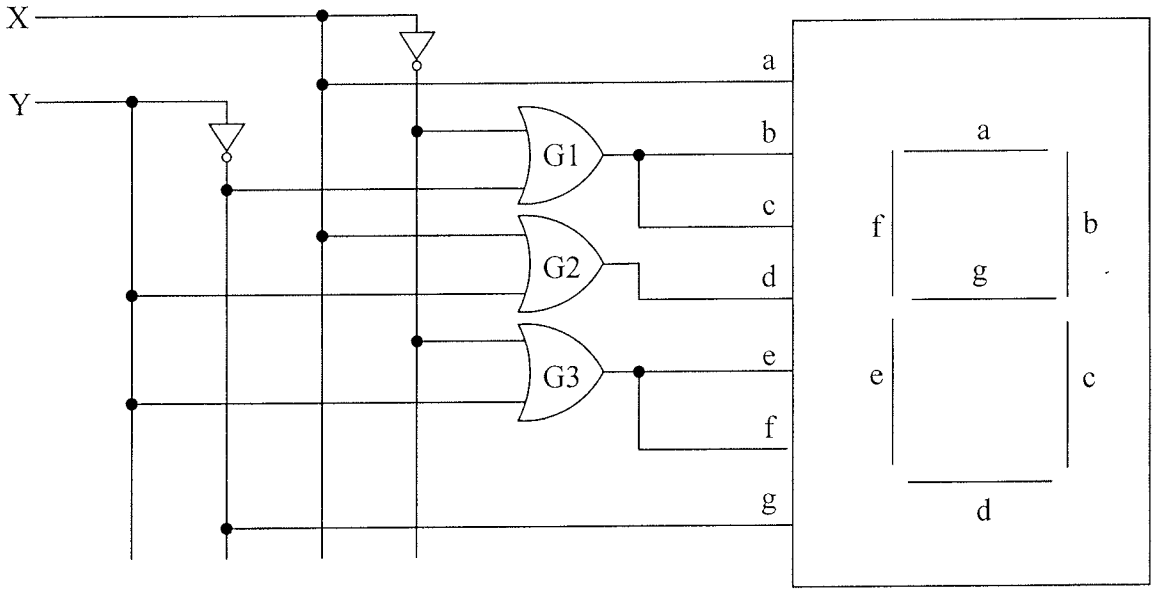
$Out = \overline{(R+S)} = \bar{R} \cdot \bar{S} = \overline{\overline{(x+\bar{y})}} \cdot \overline{\overline{(\bar{x}+z)}}$

$= (x + \bar{y})(\bar{x} + z)$ by Involution

$= \bar{F}$

M.-C. Brunet

**Problem 5** *(15 points)*




Complete the table below. Show your work.

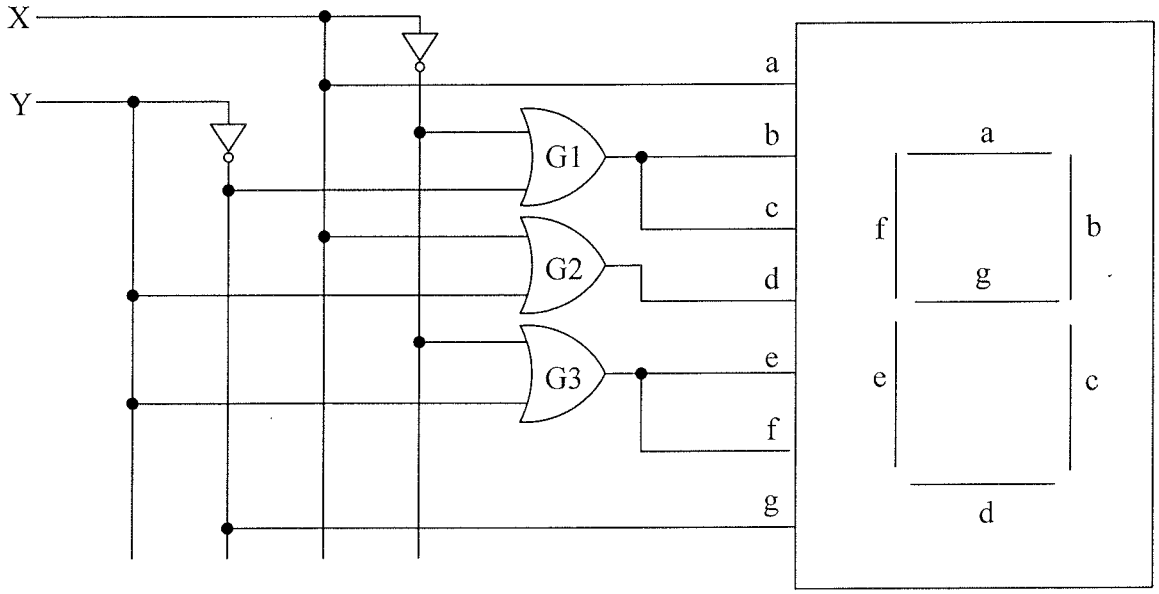
| X | Y | a | b | c | d | e | f | g | display |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | H |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | H |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | E |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | E |

$a = X$ $\quad d = X+Y$ $\quad g = \overline{Y}$

$b = c = \overline{X}+\overline{Y}$ $\quad e = f = \overline{X}+Y$

M. Iowi

**Problem 5** *(15 points)*




Complete the table below. Show your work.

| X | Y | a | b | c | d | e | f | g | display |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | |

$a = X$

$b = c = \overline{X} + \overline{Y}$

$d = X + Y$

$e = f = \overline{X} + Y$

$g = \overline{Y}$

**Problem 6** *(15 points)*

For each of the following questions, check the most correct answer.

**(a)** It is possible to implement any Boolean function using only NOR gates (and no other kinds of gates).

☒ True ☐ False

just like NAND (we can make NOT, AND, OR gates)

**(b)** It is possible to implement any Boolean function using only XNOR gates (and no other kinds of gates).

☐ True ☒ False

**(c)** $(ABC)_{16}$ is an even number.

A B C
1010 1011 1100
↑ even

☒ True ☐ False

**(d)** Adding $(A2)_{16}$ and $(5F)_{16}$ leads to overflow on an 8-bit parallel adder.

```
  1
 A2
 5F
---
101
```

we would need 9 bits

☒ True ☐ False

**(e)** A seven-segment display can be used to display any decimal digit.

☒ True ☐ False

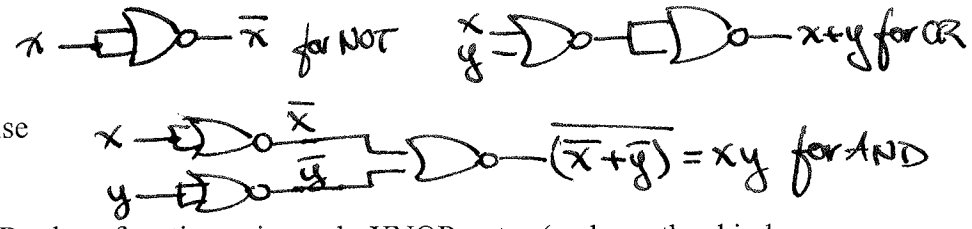
0 → 9 possible (all).

M. Loui

**Problem 6** *(15 points)*

For each of the following questions, check the most correct answer.

**(a)** It is possible to implement any Boolean function using only NOR gates (and no other kinds of gates).




☑ True ☐ False

**(b)** It is possible to implement any Boolean function using only XNOR gates (and no other kinds of gates).

☐ True ☑ False

**(c)** $(ABC)_{16}$ is an even number.

$(ABC)_{16} = (1010\,1011\,1100)_2$

$= 2^2 + 2^3 + \ldots$ (no $2^0$)

Rightmost bit is 0, so must be even

☑ True ☐ False

**(d)** Adding $(A2)_{16}$ and $(5F)_{16}$ leads to overflow on an 8-bit parallel adder.

$$\begin{array}{r} 1\,1\,\;\;\;\;\;\;\;\; \\ 1010\;0010 \\ +\;0101\;1111 \\ \hline 100000001 \end{array}$$

☑ True ☐ False

**(e)** A seven-segment display can be used to display any decimal digit.

☑ True ☐ False