ECE 110
Professors Brunet and Loui **October 20, 2008**

HOUR EXAMINATION #2

1) Write your official:

Last Name (use capital letters):_____
First Name (use capital letters):_____
NetId & UIN:_____

2) Write your name and section at the *back* of the test

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD

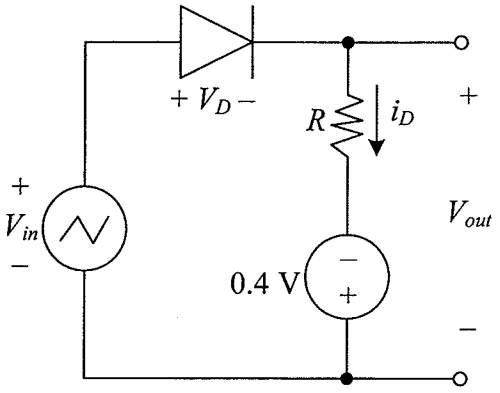
Make sure to write your name AGAIN at the top of every page of your exam.

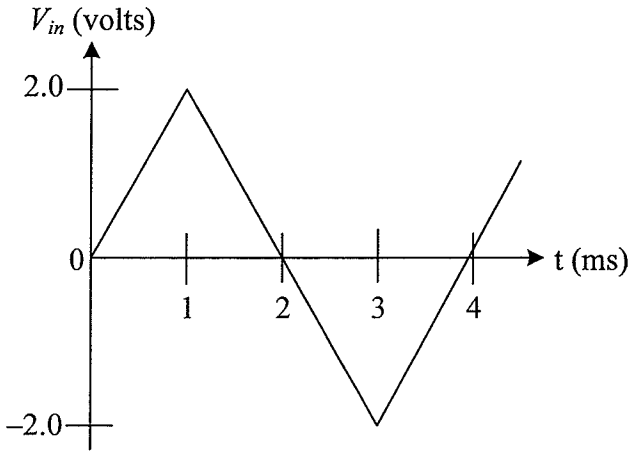
A. Write or print clearly. Answer each problem on the exam itself. If you need extra paper, there is an extra sheet at the end of this exam. Clearly identify the problem number on any additional pages. The Boolean Algebra identities are also attached to the exam.

B. In order to receive partial or full credit, **you must show all your work**, e.g., your solution process, the equation(s) that you use, the values of the variables used in the equation(s), etc. **You must also include the unit of measurement in each answer.**

Students caught cheating on this exam will earn a grade of F for the entire course. Other penalties may include suspension and/or dismissal from the university.

Problem 1 *(20 points)* The circuit below has a sawtooth wave voltage source with period 4 ms, a diode with $V_{on} = 0.6$ V, and a resistor $R = 9$ kΩ. By KVL and Ohm's Law, $V_{in} = V_D + V_{out}$, and $V_{out} = i_D R - 0.4$. To analyze this circuit, use the **large signal model**.





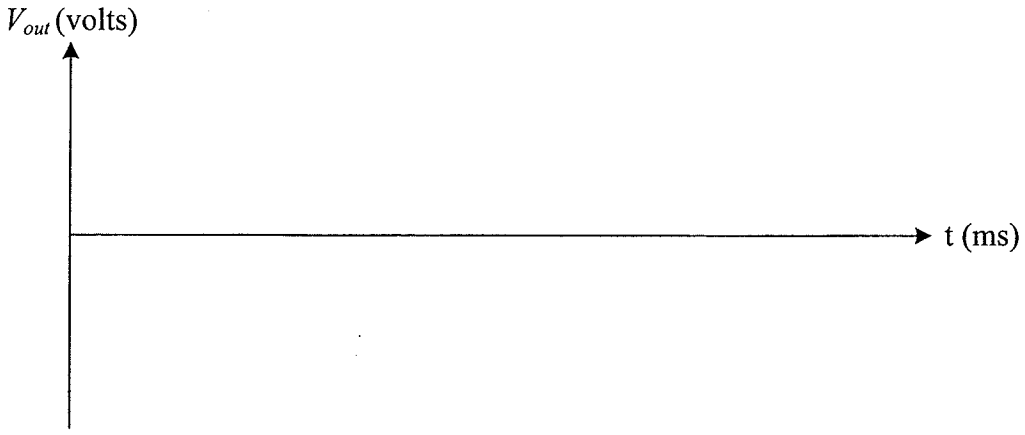
(a) *[7 pts.]* Express V_{out} in terms of V_{in} when the diode is **on**, and the range of V_{in} when the diode is on. **Show your work.**

(b) *[7 pts.]* Express V_{out} in terms of V_{in} when the diode is **off**, and the range of V_{in} when the diode is off. **Show your work.**

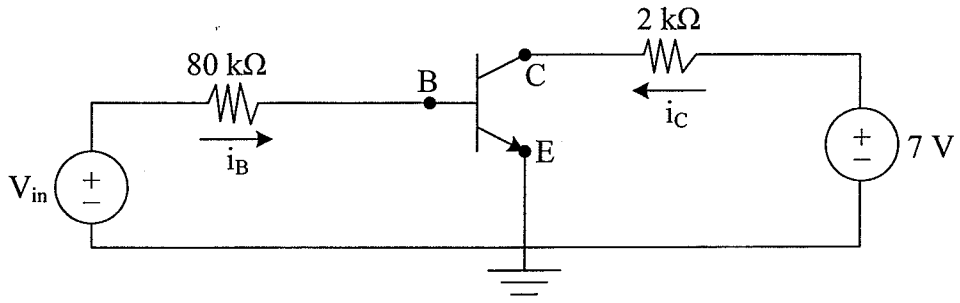
$V_{out} =$ _____ when _____ $< V_{in} <$ _____

$V_{out} =$ _____ when _____ $< V_{in} <$ _____

(c) *[6 pts.]* Plot the output voltage V_{out} for one period. Label the vertical axis with the voltages, and the horizontal axis with the times at which the behavior of the output changes.



Problem 2 *(20 points)*



$V_{BEON} = 0.6$ V; $\beta = 100$; $V_{CESAT} = 0.2$ V

For both parts below, use the information above to find the requested quantities and the transistor state.

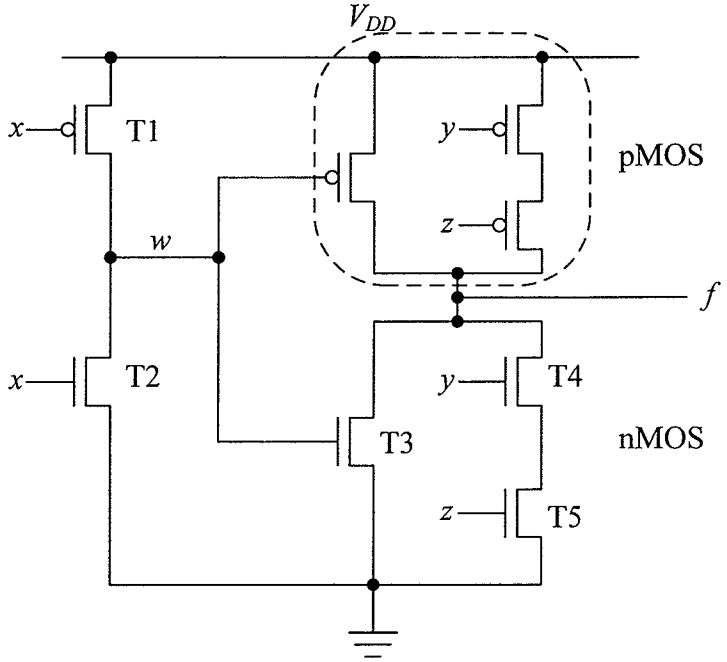
(a) *[10 pts.]* Assume $V_{in} = 1$ V. **Show your work.**

$i_B =$ ____ $i_C =$ ____ $V_{CE} =$ ____ State ____

(b) *[10 pts.]* Assume $i_C/i_B = 80$. **Show your work.**

$i_B =$ ____ $i_C =$ ____ $V_{CE} =$ ____ State ____

Problem 3 *(20 points)* In the CMOS circuit below, the nMOS part is correct, but the enclosed pMOS part is incorrect.



x	y	z	w	f
0	0	0	1	
0	0	1	1	
0	1	0	1	
0	1	1	1	
1	0	0	0	
1	0	1	0	
1	1	0	0	
1	1	1	0	

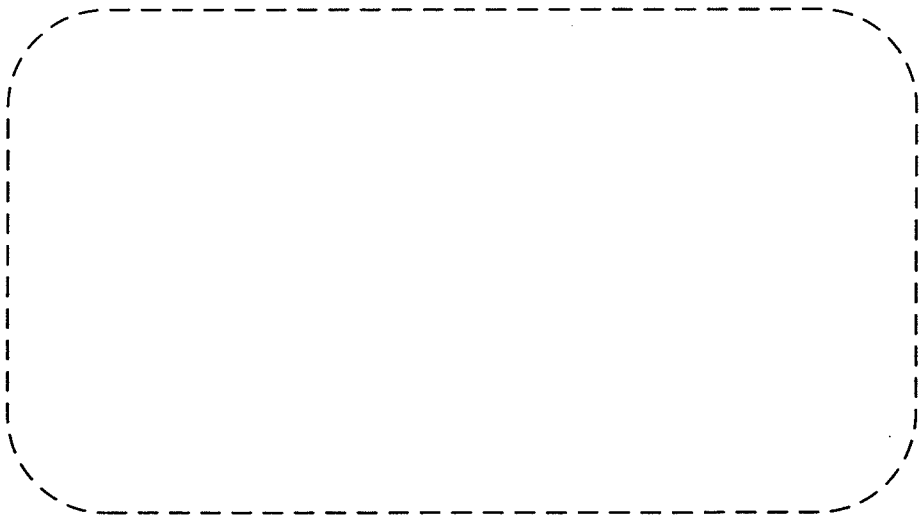
(a) *[8 pts.]* Complete the truth table for the value of f.

(b) *[4 pts.]* Explain **in words** how the table for w was obtained.

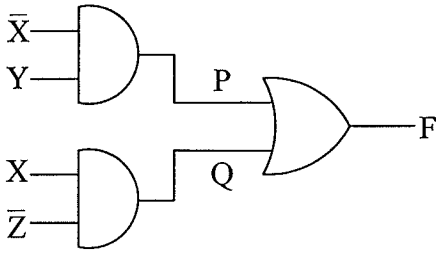
w is high (1) when because

w is low (0) when because

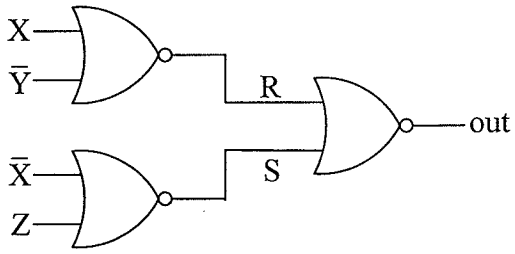
(c) *[8 pts.]* Draw the correct pMOS portion of the circuit that corresponds to the nMOS portion. Label the inputs w, y, and z clearly.



Problem 4 *(10 points)*



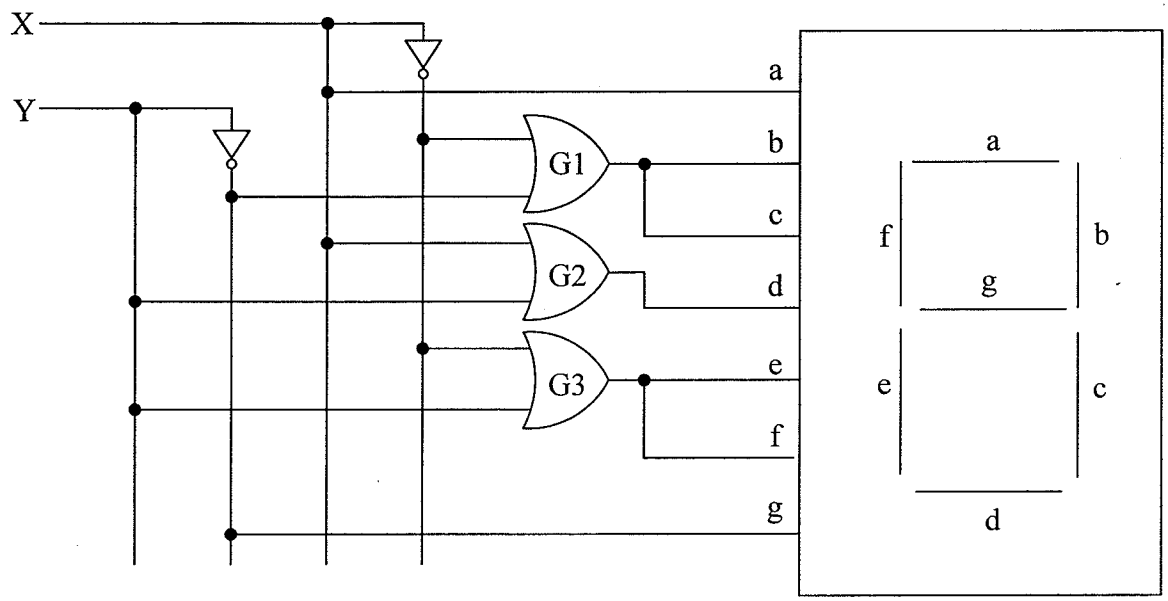
Can $\bar{F}$ (not F) be implemented with the circuit:



☐ Yes ☐ No

Clearly and **fully** justify your answer (write neatly):

Problem 5 *(15 points)*



Complete the table below. Show your work.

X	Y	a	b	c	d	e	f	g	display
0	0								
0	1								
1	0								
1	1								

Problem 6 *(15 points)*

For each of the following questions, check the most correct answer.

(a) It is possible to implement any Boolean function using only NOR gates (and no other kinds of gates).

☐ True ☐ False

(b) It is possible to implement any Boolean function using only XNOR gates (and no other kinds of gates).

☐ True ☐ False

(c) $(ABC)_{16}$ is an even number.

☐ True ☐ False

(d) Adding $(A2)_{16}$ and $(5F)_{16}$ leads to overflow on an 8-bit parallel adder.

☐ True ☐ False

(e) A seven-segment display can be used to display any decimal digit.

☐ True ☐ False