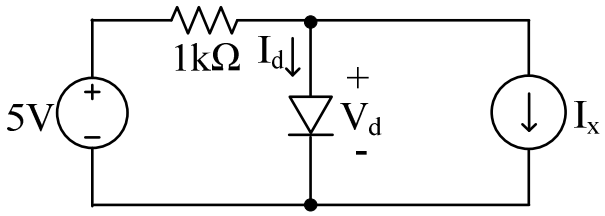
SP'11

Problem 1 *(20 points)*

The diode in the following circuit has a value for V_{ON} of 0.7 V.



(a) *(10 pts)* Determine I_d and V_d for I_x = 7 mA.

V_d = −2 V

I_d = 0 mA

(b) *(10 pts)* Determine I_d and V_d for I_x = 4 mA.

V_d = 0.7 V

I_d = 0.3 mA

Problem 2 *(20 points)*

Multiple choice problem. Mark the box adjacent to the answer(s) that are correct.

(a) *(5 pts)* Mark all correct expressions for the F given in the truth table below.

X	Y	Z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

- ☐ $F = \overline{X}Y\overline{Z} + \overline{X}YZ + X\overline{Y}Z + XYZ$
- ☒ $F = \overline{X}Y\overline{Z} + \overline{X}YZ + XY\overline{Z} + XYZ$
- ☐ $F = \overline{X}Y\overline{Z} + X\overline{Y}Z + XY\overline{Z} + XYZ$
- ☐ $F = \overline{X}Y + YZ$
- ☒ $F = Y\overline{Z} + YZ$
- ☒ $F = \overline{X}Y + XY$
- ☐ $F = X$
- ☒ $F = Y$
- ☐ $F = Z$

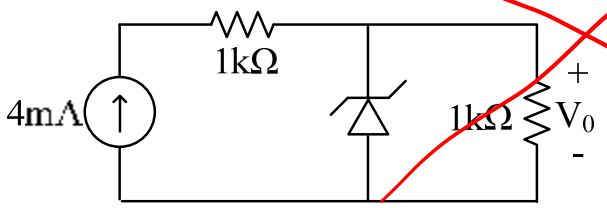
(b) *(5 pts)* Determine the sum (expressed in binary) of $(101)_2$ and $(011)_2$.

- ☐ 1 0 0
- ☐ 1 1 0
- ☐ 0 1 1
- ☒ 1 0 0 0
- ☐ 1 1 0 0
- ☐ 1 1 1 0

(c) *(5 pts)* Considering X as the only input, check all of the following that can be used to yield $\overline{X}$.

- ☐ XNOR gate
- ☒ NAND gate
- ☐ AND and OR gates
- ☒ OR and NOT gates
- ☐ AND and XOR gates
- ☐ None of the above

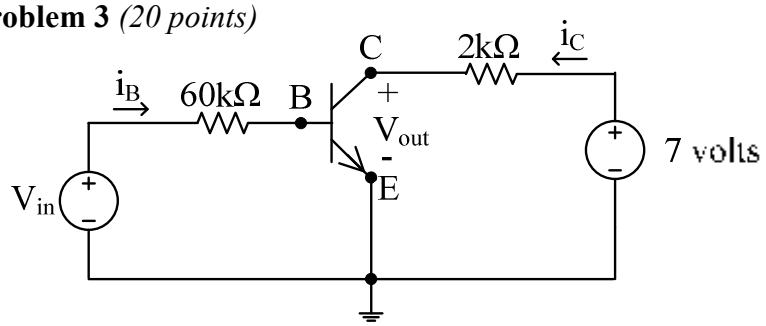
(d) *(5 pts)* Determine V_O if the zener diode in the following circuit has a zener voltage, $V_Z = 5$ V.



- ☐ $V_0 = 8$V
- ☐ $V_0 = -8$V
- ☐ $V_0 = 5$V
- ☐ $V_0 = -5$V
- ☐ $V_0 = 4$V
- ☐ $V_0 = -4$V

zener diodes no longer covered -

Problem 3 *(20 points)*



BJT parameters
V_{BEON} = 0.5volts
V_{CESAT} = 0.3volts
β = 100

(a) *(14 pts)* Fill out the table below for the value of V_{in} provided. For each part, show all of your work to justify your results.

V_{in}	i_B (µA)	i_C (mA)	V_{OUT} (volts)	BJT state
0.2	0	0	7	OFF
2	25	2.5	2	active
3	41.67	3.35	0.3	saturated

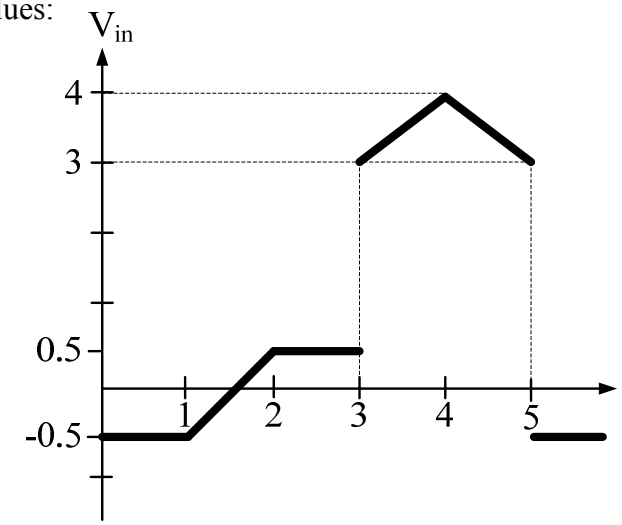
use space for work

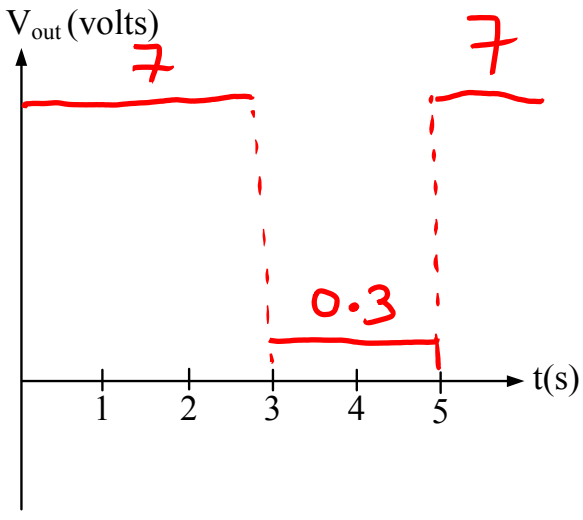
V_{in} = 0.2volts

V_{in} = 2volts

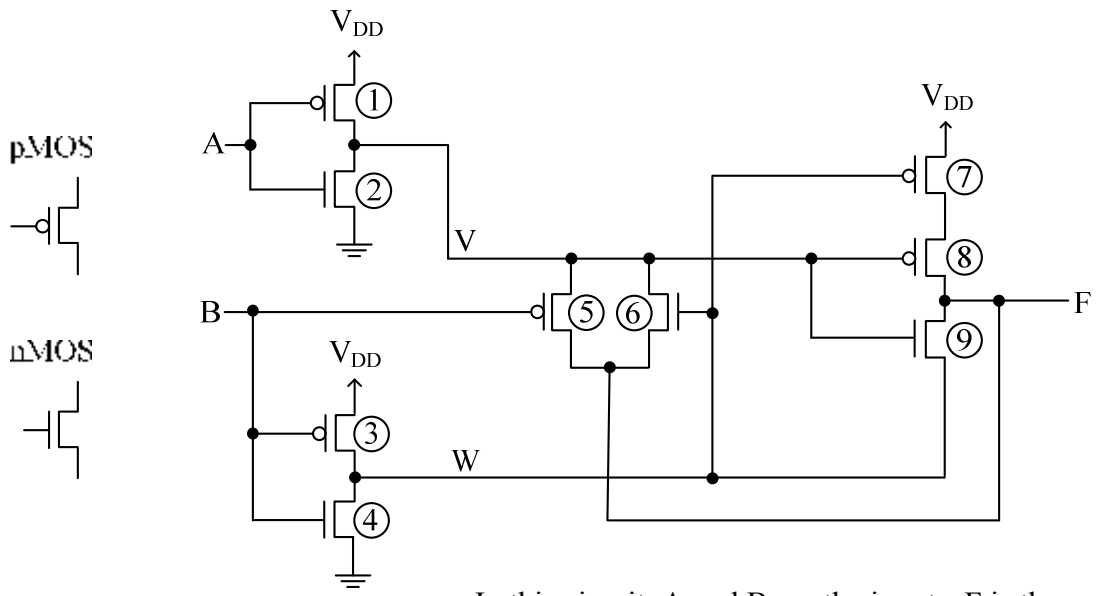
V_{in} = 3volts

(b) *(6 pts)* For the given graph for V_{in}, draw the graph for V_{OUT}. Show work; label relevant values:





Problem 4 *(20 points)*



In this circuit, A and B are the inputs, F is the output. There are 9 transistors, labeled 1-9.

(a) *(4 pts)* Write the values for V and W in the table below.

A B	V W	pMOS Low	nMOS High
0 0	11	135	69
0 1	10	17	49
1 0	01	358	26
1 1	00	78	24

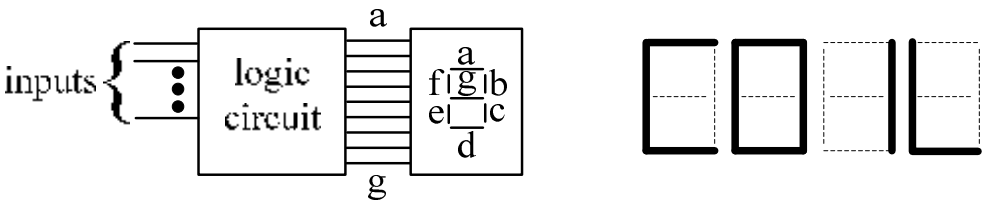
(b) *(8 pts)* In the right side of the table above, list all the pMOS transistors that have low values at their control input, and all the nMOS transistors that have high values at their control input. (Write the number of each transistor, they are labeled in the circuit.)

(c) *(8 pts)* The circuit implements an exclusive-nor gate. When F=1, F is connected to V_{DD} by one of two paths: either through pMOS transistors 1 and 5, or pMOS transistors 7 and 8. When F=0, F is connected to ground by one of two paths: either through nMOS transistors 2 and 6, or nMOS transistors 4 and 9. Complete the truth table below (fill in F), and also for each line on the truth table, put a checkmark in the column labeled with the two transistors that connect F to V_{DD} or ground.

A B	F	1 & 5	7 & 8	2 & 6	4 & 9
0 0	1	✓			
0 1	0				✓
1 0	0			✓	
1 1	1		✓		

Problem 5 *(20 points)*

In this problem, you will design a logic circuit that allows to eventually display COIL.



(a) *(2 pts)* How many input lines are needed for the design? Justify answer.

2

(b) *(4 pts)* Fill out the truth tables below for your circuit. Make sure to name and include in the first column as many inputs as you claimed in (a).

inputs	outputs						
x y	a	b	c	d	e	f	g
0 0	1	0	0	1	1	1	0
0 1	1	1	1	1	1	1	0
1 0	0	1	1	0	0	0	0
1 1	0	0	0	1	1	1	0

(c) *(3 pts)* From your table in (b), considering the design of the entire circuit (for all seven outputs), how many different circuits would you really need to design? Justify your answer.

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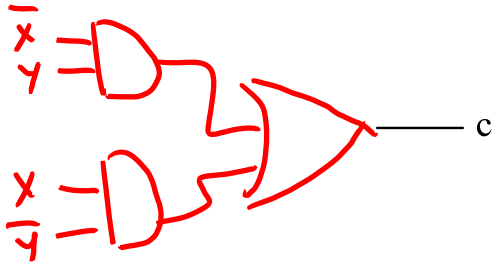
(d) *(7 pts)* From your table in (b), give the canonical SOP for outputs c and d. Use input names you defined in part (b). Draw the non optimized AND OR circuit for output c below.

c = $\bar{x}y + x\bar{y}$

d = $\bar{x}\bar{y} + \bar{x}y + xy$



(e) *(4 pts)* Assuming complemented inputs are available, suggest an implementation for c and d using at most one gate each. Give the corresponding Boolean expressions. Use input names you defined in part (b).

c = $x \oplus y$ d = $\bar{x} + y$