Hour Examination #3

1) Write your official:
   Last Name (use capital letters):_____KEY_____

   First Name (use capital letters):_____

   NetID:_____

   UIN:_____

2) Fill in the Orange bubble sheet with all the information requested:
   a. LAST NAME, FIRST INITIAL *example*: SCHMITZ C
   b. STUDENT NUMBER (UIN) *example*: 678912345
   c. SECTION (AL1 9am enter **111**, AL2 1pm enter **222**, AL3 3pm enter **333**)
   d. NETWORK ID (NetID) *example*: cdschmit
   e. Also, fill out the hand-written center of the sheet with course, instructor, section and your signature.

DO NOT TURN THIS PAGE UNTIL YOU ARE TOLD

A. Write or print clearly in this exam booklet for your own benefit. Circle the correct answer within the exam booklet and then mark it on the orange bubble sheet. You may not argue for points because you marked one answer in the exam and another on the bubble sheet, so be careful when marking your answers.

B. All problems are equally weighted.

C. Your grade will be determined based on the answers submitted on your bubble sheet. ***Submit both the bubble sheet AND the complete exam booklet***.

Students caught cheating on this exam will earn a grade of F for the entire course. Other penalties may include suspension and /or dismissal from the university.

I have read and acknowledge the above statements. Furthermore, I promise not to give or receive help on this or any other exam.

_____

Signature

You have TEST FORM :

A

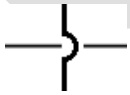
Please enter this in the lower right corner of the orange bubble sheet in the location marked TEST FORM.

The **FACT SHEET** is the last page of the exam. It may be removed from the exam for your convenience.

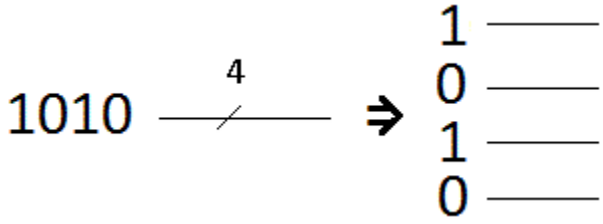
Comments on the exam circuit diagrams:

- The solid dot represents a split (connection, node) on a wire. Not all diagrams use the solid-dot notation if the intended meaning is thought to be clear.

- The semicircle represents that a wire that is being crossed without an electrical connection. The wire beneath is "shadowed" and not actually broken.



- A slashed wire with a number over it represents a bundle ("bus") of wires. For example, the following symbol actually means that four wires (not one) are carrying the voltages of the binary signals 1,0,1, and 0:



1. The decimal sum of 1001_2 and 12_{16} is

    a. 14
    b. 20
    c. 21
    d. $27 = 9 + 18$
    e. 36

2. A 4-bit adder with 4-bit output computes the HEX sum: $A_{16} + x$. What is the smallest value of x for which the adder overflows?

    a. $x = 5_{16}$
    b. $x = 6_{16}$ *because* $10 + 6 = 16 \Rightarrow$ *needs* 5 *bits*
    c. $x = 8_{16}$
    d. $x = A_{16}$
    e. $x = F_{16}$

3. Which are the correct hex values for the ASCII encoding for "Hi"? Assume an **even** parity has been added to the right end (least significant bit) of each 7 bit ASCII word.

    a. D0 D2
    b. D1 D2
    c. D0 D3
    d. **90 D2 ⇒ 1001000 1101001**
    e. 91 D3

4. In a digital error detection scheme, each 3-bit word has an odd parity bit added in the most-significant bit location. What is the original 9-bit message of this received data steam? Received data: **001011100110**

    a. 001011100
    b. 001111011
    c. 010110110
    d. 010111110
    e. It is impossible to reproduce the entire original sequence. There is an error in the last four bits 0110 has even parity, but which bit flipped? Only error detection is available, not error correction.

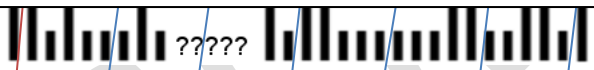
The following information pertains to the next question:

Four 7-bit words were encoded for transmission with even parity added to each word, and a redundancy check code word (odd parity) added at the end. This is the data that was received:

0 0 1 0 1 1 0 1
1 0 1 1 0 0 0 1
0 1 0 0 1 0 1 0 ← error in this row
1 0 0 1 1 1 0 0
1 0 1 1 0 0 0 1

5. A single-bit error has occurred in transmission of the third row. What would the third row be if there had been no single-bit error?
   a. 1 1 0 0 1 1 1 0
   b. 0 0 0 0 1 1 1 0
   c. 0 1 1 0 1 1 1 0
   d. 0 1 0 1 1 1 1 0
   e. 0 1 0 0 1 1 1 0 because the 5th column does not have odd parity. Correcting this bit fixes both parity problems and is the most likely error. This code allows for single error correction. THINK: Could we have found and corrected errors in other rows/columns too?

T 7 4 2 10 742 10 74210 74210 742 10 74 210 T...$[9 + x + y + 0 + 1 + 3]_{mod10} = 0$



6. What is the missing portion of this USPS bar code?

A quick inspection that each digit must have two 1's (tall bars) tells us that only c or e can be the correct answer. We also see that $x = 4$ *or* 5 and $y > 1$. Both c and e give $x = 4$, so we see that $[9 + 4 + y + 0 + 1 + 3]_{mod10} = [y + 17]_{mod10} = 0 \Rightarrow y = 3$ and answer c is correct.

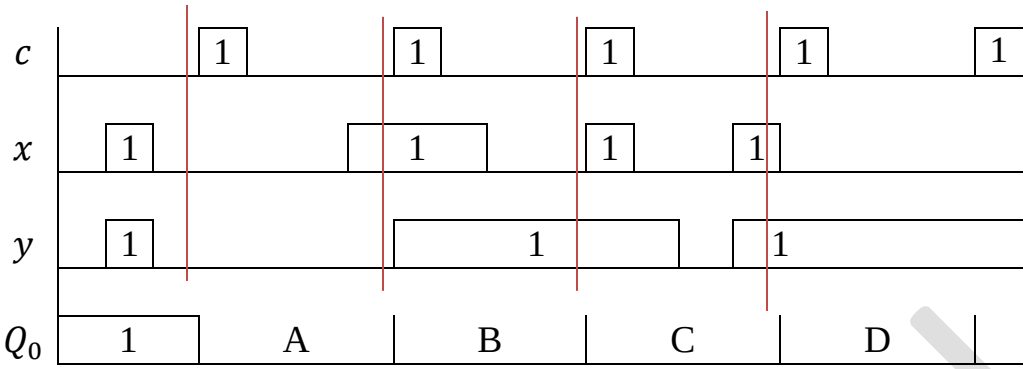
a. 

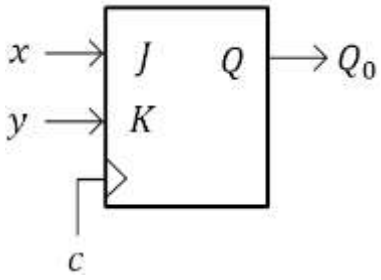
b. 

c. 

d. 

e. 





7. Given the partial timing diagram above for the given circuit, what are the values of Q_0 in the labeled regions, A, B, C and D?

   a. 0110
   b. 1111
   c. 1010
   d. 0001
   e. 1101 because JK are 00 (stay), 10 (set), 01 (reset), 11 (toggle) just before rising edges.

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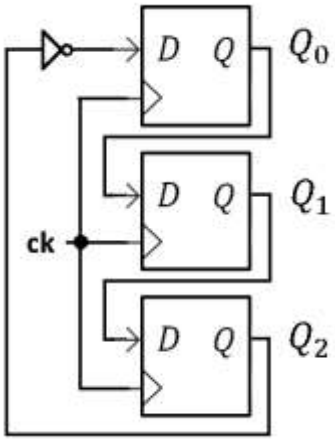
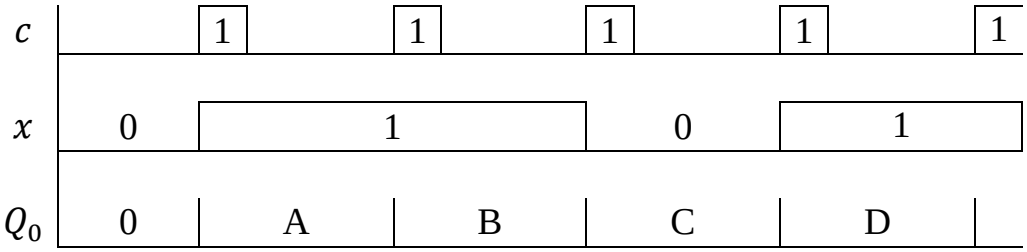
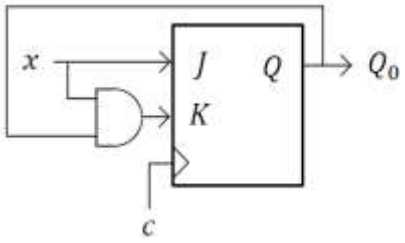
8. The shift register to the right has $Q_0 = 1, Q_1 = 0, Q_2 = 1$ at some time, t. What are the register contents of $Q_0, Q_1,$ and Q_2, respectively, three clock cycles later?

   a. 1,0,1
   b. 0,0,1
   c. 0,1,0 … 101 → 010 → 101 → 010
   d. 0,1,1
   e. 1,0,0

   NOT



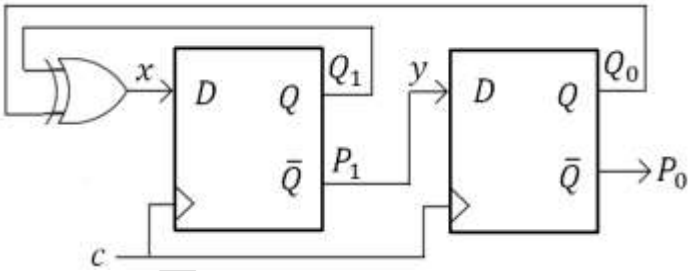




9. Given the partial timing diagram above for the given circuit, what are the values of Q_0 in the labeled regions, A, B, C and D?

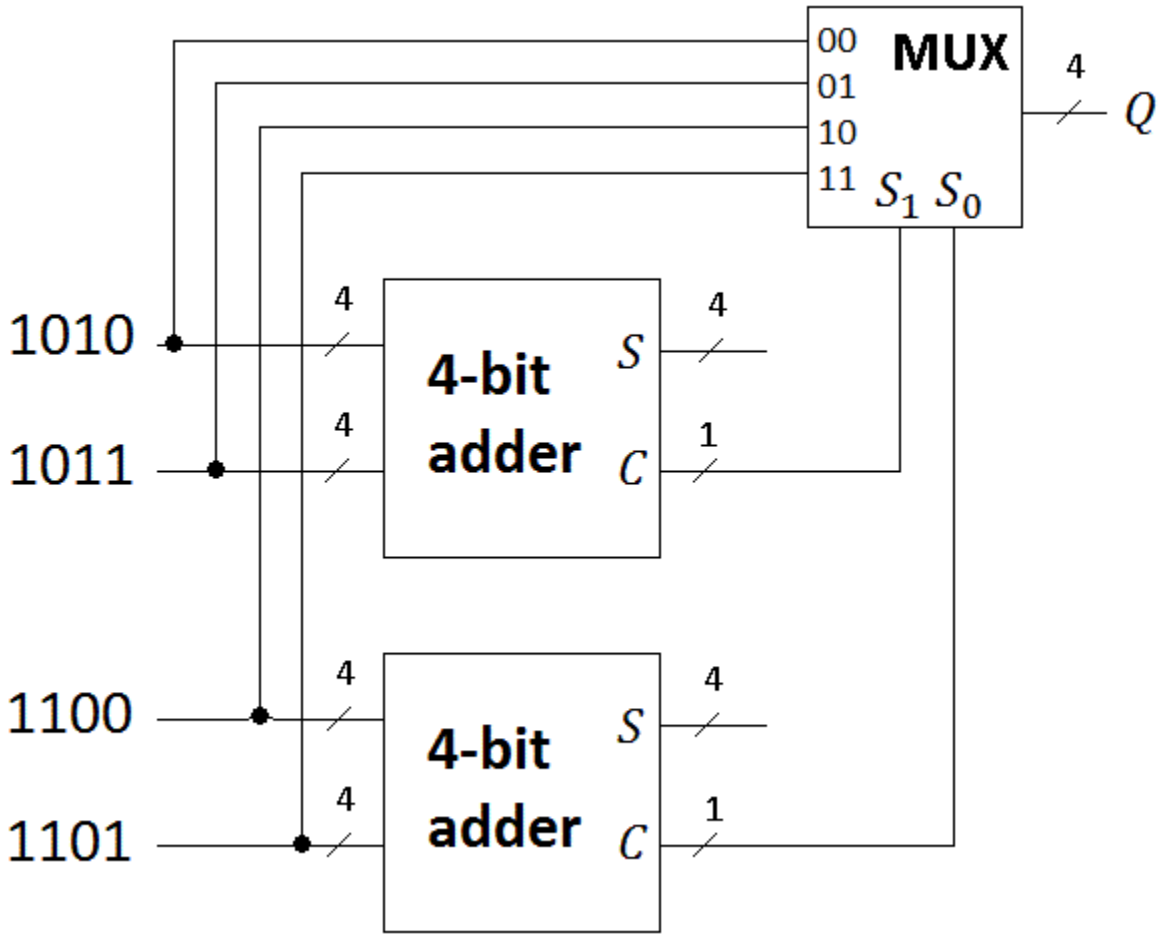
Again, draw horizontal lines just before the rising clock edges to find value of $x, Q_0, and\ x \cdot Q_0$.

a. 1001
b. 1100
c. 1010
d. 1111
e. 0100



10. Given $Q_1 = 0, P_1 = 1, Q_0 = 0, P_0 = 1$ at time t, What are these values one clock cycle later?

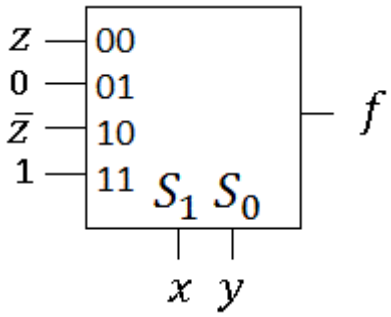
a. $Q_1 = 0, P_1 = 1, Q_0 = 0, P_0 = 1$
b. $Q_1 = 0, P_1 = 0, Q_0 = 0, P_0 = 1$
c. $Q_1 = 1, P_1 = 0, Q_0 = 0, P_0 = 1$
d. $\boldsymbol{Q_1 = 0, P_1 = 1, Q_0 = 1, P_0 = 0}$
e. $Q_1 = 0, P_1 = 0, Q_0 = 0, P_0 = 0$



11. Given the 4-bit inputs in the circuit above, the output Q, in HEX, is

a. A_{16}
b. B_{16}
c. C_{16}
d. D_{16}
e. Cannot tell from the information provided.

Both carry bits will be high. The MUX selector is set to 11 allowing 1101 to pass out to Q. $1101_2 = 13_{10} = D_{16}$



12. Which truth table describes the output of the MUX above given by f?

a.

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

b.

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

c.

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

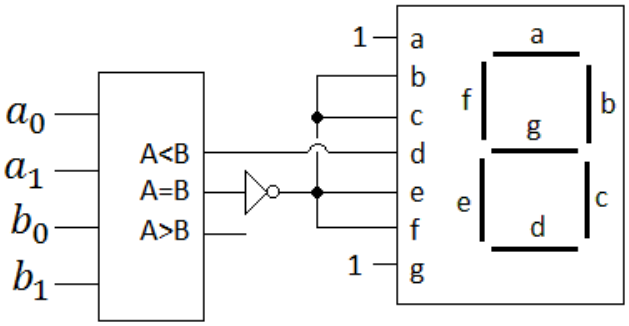
d.

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

e.

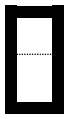
x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Consider this circuit for the next two problems:



where $A = a_1a_0$ and $B = b_1b_0$, so that a_1 and b_1 are the most significant bits of A and B, respectively.

13. What is displayed when $a_1 = b_0 = 1$ and $a_0 = b_1 = 0$?

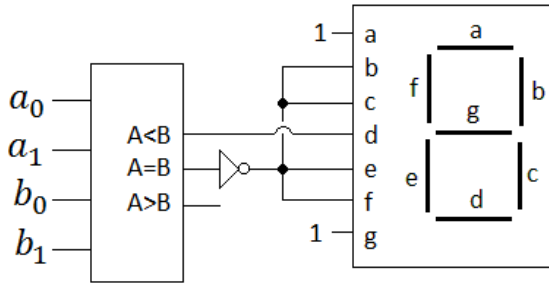
a. 

b. 

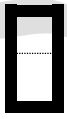
c. 

d. 

e. 



14. What is displayed when $a_0 = a_1 = b_0 = b_1 = 1$?

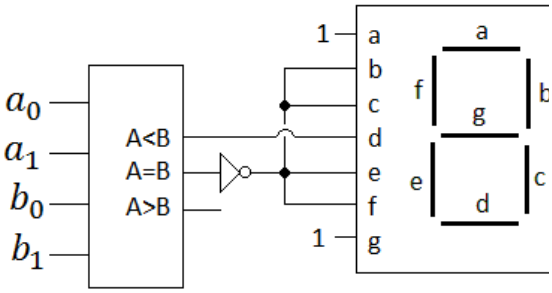
a. 

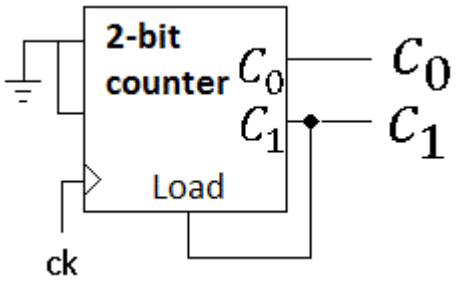
b. 

c. 

d. 

e. 





The default is to count up. This circuit will count 00, 01, 10 at which point the Load pin goes high and the device is reset to 00.

15. The counter above has grounded inputs and a clock signal, ck. As the clock runs, what is the decimal equivalent of the binary sequence provided by c_1c_0?

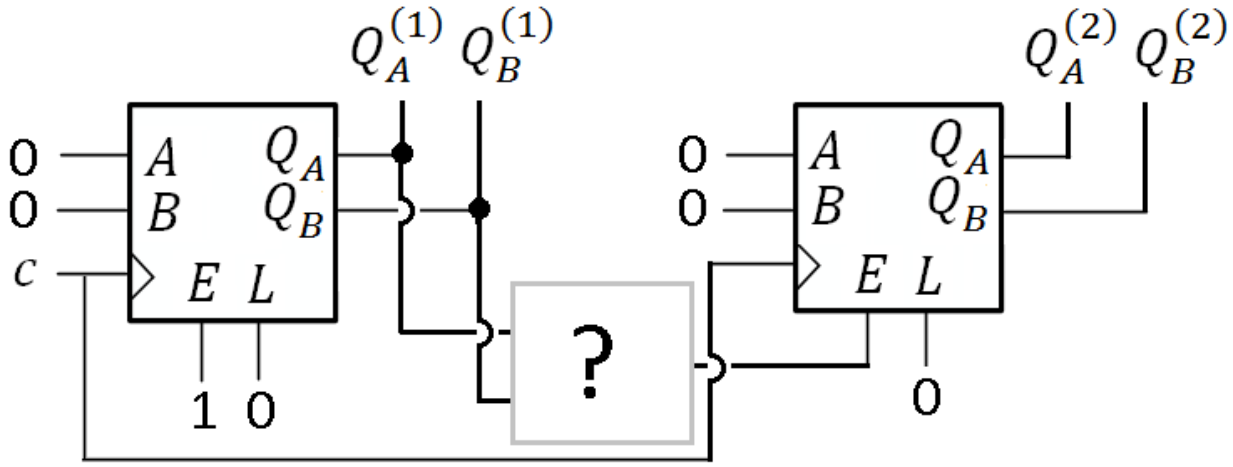
    a. 0, repeat
    b. 0,1, repeat
    c. 0,1,2, repeat
    d. 0,1,2,3, repeat
    e. 0,1,2,1, repeat

16. What is the duty cycle of c_0?

    a. 25%
    b. 33%
    c. 50%
    d. 66%
    e. 75%

If we watch the bit of LSB c_0, we see that it goes 0 1 0 0 1 0 0 1 0…changing on the rising edges of the clock. Therefore, it is one for one of three clock cycles.

The configuration below can be used to turn two 2-bit upcounters into a single 4-bit upcounter with 4-bit output $Q_B^{(2)}Q_A^{(2)}Q_B^{(1)}Q_A^{(1)}$.



17. What logic gate belongs in the box labeled with the question mark to complete the upcounter design?

a. OR
b. NOR
c. XOR
d. AND
e. NAND

Consider what needs to happen in a 4-bit counter:

0000
0001
0010
0011 so far, the right two bits count up, now it is time for the left two bits to count once, so the enable should go high.
0100 since the lower two bits continue to count as well.
0101
0110
0111 and now we want the two MSB bits to go up again!
1000
1001
1010
1011
1100
1101
1110
1111…The AND gate gives us the enable when we need it!

18. If a voice waveform is sampled with $T_s = 100\mu s$ and each sample is quantized to 256 levels, the resulting data rate is

a. 40 kbps
b. 80 kbps
c. 160 kbps
d. 800 kbps
e. 2.56 Mbps

$$256 = 2^b \Rightarrow b = 8\frac{bits}{Sample}$$
$$1\frac{Sample}{100\mu s} \times \frac{8bits}{Sample} = \frac{8}{100}e6 = 8e4\ bps = 80kbps$$

19. With which sampling rate is the frequency $f = 101\ kHz$ not an alias pair with $1\ kHz$?

a. $20\ kHz$
b. $25\ kHz$
c. $34\ kHz$
d. $40\ kHz$
e. $50\ kHz$

$g = |f - mf_s|$ such that $0 \le g < \frac{f_s}{2}$
a. $m = 5\ works$
b. $m = 4\ works$
c. $m = 3\ works$
d. $doesn't\ work\ for\ any\ m$
e. $m = 2\ works$

20. The analog signal $s(t) = 4\cos(15\pi t)$ is sampled, starting at $t = 0$, with a sampling rate of $20\ Hz$ producing the sequence $s[0], s[1]$, ... What is the 11^{th} value of the sampled sequence, $s[10]$?

a. -4
b. -1
c. 0
d. 0.92
e. 3.67

Just like in Lon Capa, use your calculator in radians. The presence of PI in the argument should alert you to this fact in the future.

$$4\cos(15\pi t) \Rightarrow 4\cos\left(\frac{15\pi n}{20}\right)$$
$$= 4\cos\left(\frac{3\pi \times 10}{4}\right) = 4\cos(7.5\pi) = 4\cos(7.5\pi - 6\pi)$$
$$= 4\cos(1.5\pi) = 4 \times 0\ since \cos\left(\frac{3\pi}{2}\right) = 0.$$

Fact Sheet:

a2 a1 a0 a6 a5 a4 a3	000	001	010	011	100	101	110	111
0000	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL
0001	BS	HT	LF	VT	FF	CR	SO	SI
0010	DLE	DC1	DC2	DC3	DC4	NAK	SYN	ETB
0011	CAN	EM	SUB	ESC	FS	GS	RS	US
0100	SP	!	"	#	$	%	&	'
0101	(	)	*	+	,	–	.	/
0110	0	1	2	3	4	5	6	7
0111	8	9	:	;	<	=	>	?
1000	@	A	B	C	D	E	F	G
1001	H	I	J	K	L	M	N	O
1010	P	Q	R	S	T	U	V	W
1011	X	Y	Z	[	\	]	^	_
1100	`	a	b	c	d	e	f	g
1101	h	i	j	k	l	m	n	o
1110	p	q	r	s	t	u	v	w
1111	x	y	z	{	|	}	~	DEL

ASCII Table

Digit	Code	Digit	Code
1	00011	6	01100
2	00101	7	10001
3	00110	8	10010
4	01001	9	10100
5	01010	0	11000

POSTNET digit assignments

D Flip-Flop

D	Q^+
0	0
1	1

SR Flip-Flop

S	R	Q^+
0	0	Q memory
0	1	0 reset
1	0	1 set
1	1	?

JK Flip-Flop

J	K	Q^+
0	0	Q memory
0	1	0 reset
1	0	1 set
1	1	$\overline{Q}$ complement

Decimal	Binary	Hexa
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F