

Lecture 11 Uniform Circuit Complexity

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 - SIZE(T') ⊊ SIZE(T) if T=Ω(†2⁺) and T'=O(2⁺/†)

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 - $NP \subseteq P/\log \Rightarrow NP = P$
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Most functions on t bits (that ignore last n-t bits) are in SIZE(T) but not in SIZE(T')

Oniform circuit family: constructed by a TM

Output of the second second

 Undecidable languages are undecidable for these circuits families

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Can relate their complexity classes to classes defined using TMs

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Substant Logspace-uniform:

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Logspace-uniform:

An O(log n) space TM can compute the circuit

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 \odot So NC = AC

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- Open problem: Is NC = P?

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Total "work" is size of the circuit

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⊘ PARITY in NC¹

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• Circuit should evaluate $x_1 \oplus x_2 \oplus ... \oplus X_n$

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 - Total depth O(log n)

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 - Length of path = depth of circuit = O(log n)

$\mathsf{NL} \subseteq \mathsf{A}C^1$

\odot Recall PATH $\in AC^1$

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- \odot Recall PATH $\in AC^1$
- Also recall PATH is NL-complete
 - with respect to log-space reductions
 - In fact, with respect to NC¹ reductions
 - Exercise! (For NL machine M, can build (in log-space) NC¹ circuit which on input x, outputs (i,j)th entry of the adjacency matrix of configuration graph of M(x).)
 - Combining the NC¹ circuits for reduction and the AC¹ circuit for PATH, we get an AC¹ circuit
$\odot \mathsf{NC}^{\mathsf{i}} \subseteq \mathsf{AC}^{\mathsf{i}} \subseteq \mathsf{NC}^{\mathsf{i+1}} \subseteq \mathsf{NC} = \mathsf{AC} \subseteq \mathsf{P}$

 $\odot \mathsf{NC}^0 \subsetneq \mathsf{AC}^0 \subsetneq \mathsf{NC}^1 \subseteq \mathsf{L} \subseteq \mathsf{NL} \subseteq \mathsf{AC}^1$

NCⁱ ⊆ ACⁱ ⊆ NCⁱ⁺¹ ⊆ NC = AC ⊆ P
NC⁰ ⊊ AC⁰ ⊊ NC¹ ⊆ L ⊆ NL ⊆ AC¹
AC⁰ ⊊ NC¹ as PARITY ∉ AC⁰ (later)
Open: whether NCⁱ ⊊ ACⁱ ⊊ NCⁱ⁺¹ for larger i

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Open: Is NC = P? (Can all polynomial time decidable languages be sped up to poly-log time using parallelization?) Zoo



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Coincides with EXP (Why?)

Restricted to depth k, 2^{poly(n)} size, unbounded fan-in DC uniform circuit families decide exactly languages in $\Sigma_k^P \cup \Pi_k^P$

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 Given a DC uniform circuit (w.l.o.g alternating levels of AND and OR gates, and NOT gates only at the input level) of depth k, an equivalent quantified expression with k alternations

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 - Given a quantified expression with k alternations, an equivalent DC uniform circuit of depth k

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- Input accepted by the circuit iff Alice has a winning strategy (i.e., if the quantified expression is true)
- Each edge has a polynomially long label, and quantified variables take values from the same domain. Checking if edge is a correct wire in poly time (uniformity)

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- Circuit has sub-circuits evaluating the poly-time condition for each possible assignment of the quantified variables.
- Hang these sub-circuits at the leaves of a k-level AND-OR tree appropriately
- Circuit can be implicitly computed in polynomial time. Size 2^{O(total length of variables)}









Ρ

 \bigcirc NCⁱ and ACⁱ

Ø DC-uniform

OPH levels and EXP



Today

P

- DC-uniform
 - PH levels and EXP
- Later, more circuits and non-uniform computation (time permitting)



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 - Decision trees, Branching programs
 - Connections between circuit lowerbounds and other complexity class separations

NC

NCK

NC¹

NC⁰

NL

AC

ACK

ACK-1

AC¹

AC⁰