Intel Alder Lake CPU Architectures

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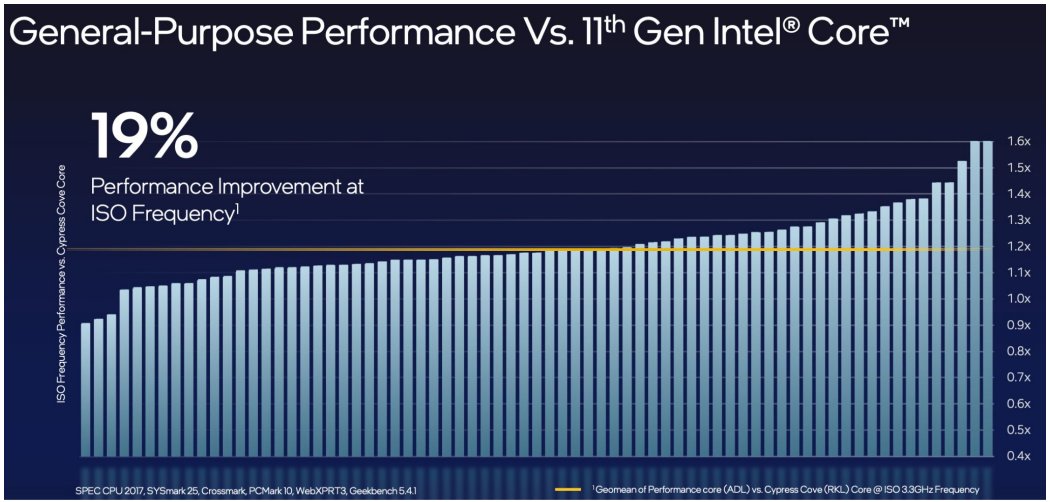
Source: Intel Architecture Day 2021 Presentation

Motivation



- Intel holds 60%+ x86 market share (Statistica)
- X86 is still dominant in desktop and server CPU market
- First Successful Gen Featuring Hybrid x86 Architecture

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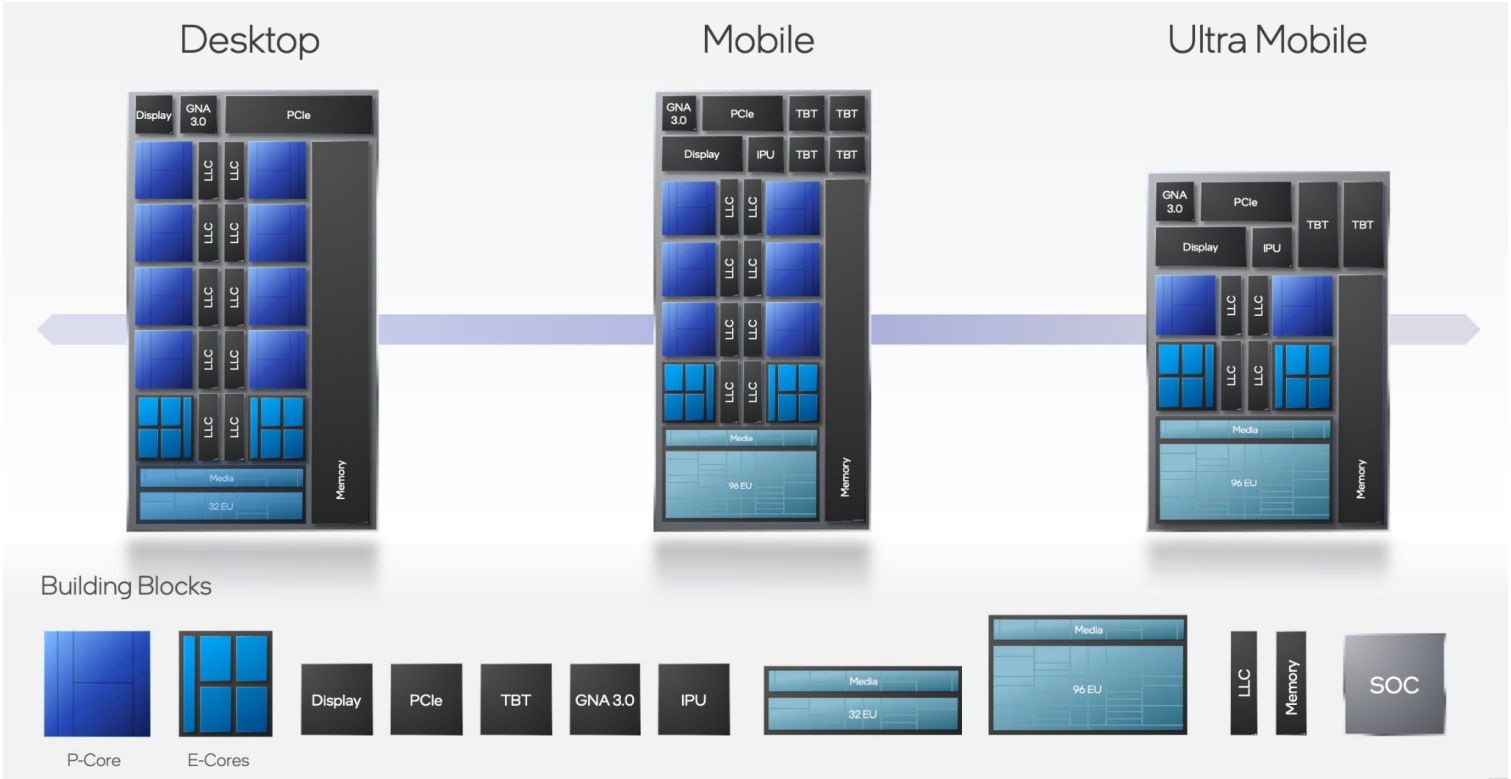
High-Level Overview



Source:
Intel Architecture Day 2021 Presentation
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P-Core

Wider & deeper execution pipeline
Frontend:

- 16 → 32 byte/cycle fetch
- 5 → 6 decoders
- 2.25 → 4k µop cache w/ 8 µop bw

Backend:

- 5 → 6 rename/allocation width
- 10 → 12 execution ports, with more units added to some
- 352 → 512 ROB size

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E-Core

Frontend:

- 32 byte/cycle fetch
- 6 decoders

Backend:

- 5 rename/allocation width
- 12 + 5 execution ports
- 256 ROB size

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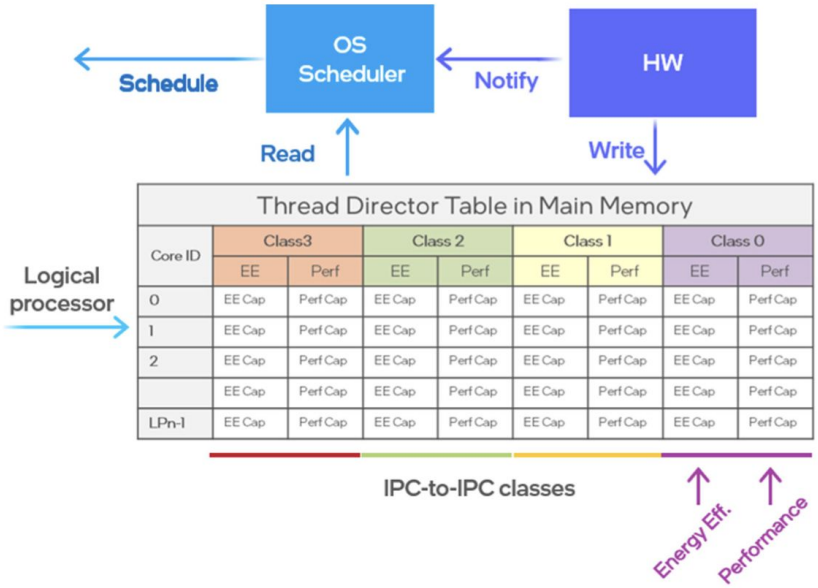
Thread Director

- Thread Director puts the threads on the right core at the right time.
- It requires support from hardware and OS.
- On the hardware
  - Thread Director predicts the category of a thread using architectural attributes and runtime characteristics of the thread, saving it with thread context for OS
  - Thread Director also fills a thread directing table enumerating the performance and efficiency of each core running different categories
- On the OS
  - Thread Director decides which core to run the thread given the information



Source:
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Memory Hierarchy

P-Core:

- 2x 64B read and write ports
- 1.25MiB L2 for each core

E-Core:

- 2x 16B read and write ports
- 2MiB L2, with 64 reqs and 16 evicts competitively shared among 4 cores

Up to 30MiB LLC

Each type of core have large instruction and data TLBs, with a 2048 entry second level TLB. Up to 4 page walks can be handled in parallel.

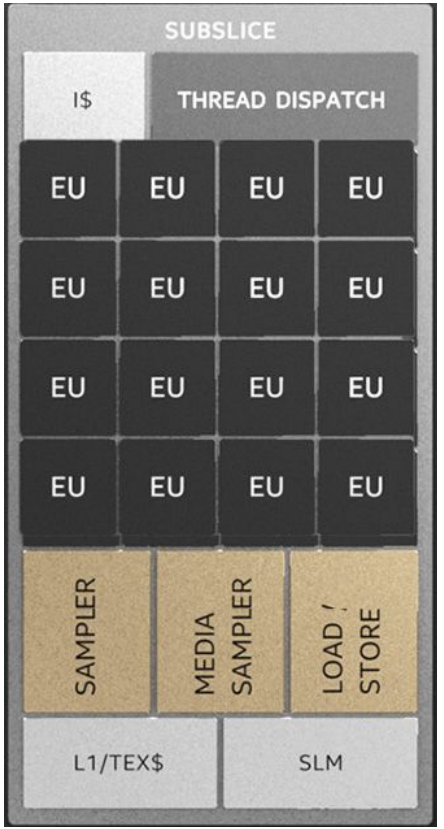
GPU

- Intel Xe
- Xe-LP variant
- Execution units
  - Desktop: 32 EUs
  - Mobile: 96 EUs

Sources: [AnandTech]

GPU (cont.): Xe-LP Subslice

- 1 slice = 6 subslices
- Each subslice
  - 16 EUs, 8 thread control units
  - Texture sampler – 8 texels/clock
  - 64KB L1 data/texture cache

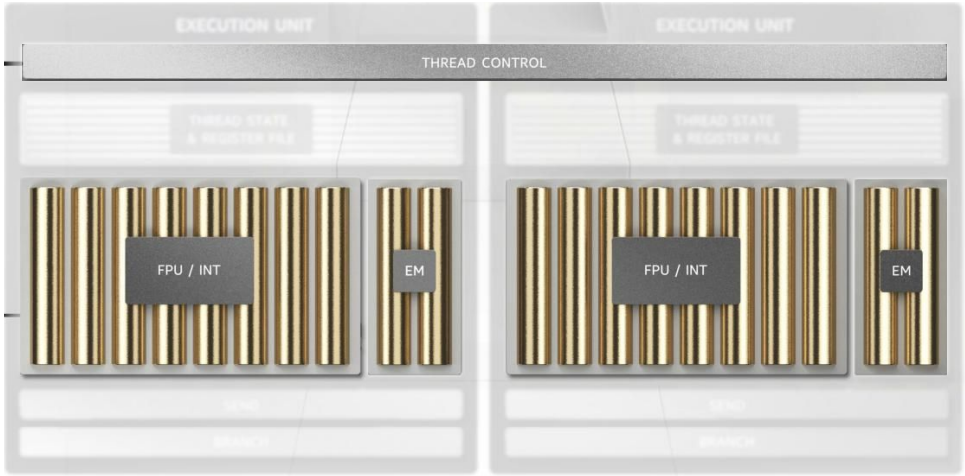


Xe-LP subslice

Sources: AnandTech

GPU (cont.): Xe-LP Execution Unit

- 6 subslices, 16 EUs each
- 2 EUs share 1 thread control unit
- Each EU
  - 8 ALUs
  - SIMD-8 – FP/INT
  - SIMD-2 – extended math



Xe-LP EU pair

Sources: AnandTech

Additional Features

Source:
Get Outstanding Computational Performance without a Specialized Accelerator - Intel
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- Advanced Vector Extension (AVX)
  - Intel AVX-512 has a register width of 512 bits. This large register supports **32 double-precision and 64 single-precision floating-point numbers**, in addition to eight 64-bit and sixteen 32-bit integers.
  - Application
    - HPC: scientific simulations, DNA sequencing, 3D advanced modeling, and financial analytics
    - Cryptography and data compression, working with Intel Crypto Acceleration and Intel QuickAssist Technology
    - Image and audio/video processing
    - AI and DL, working with Intel Deep Learning Boost (Intel DL Boost)