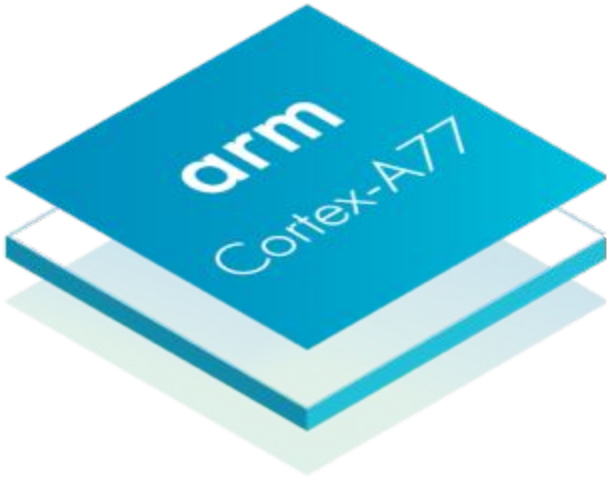
ARM Cortex A77 (*Deimos*)



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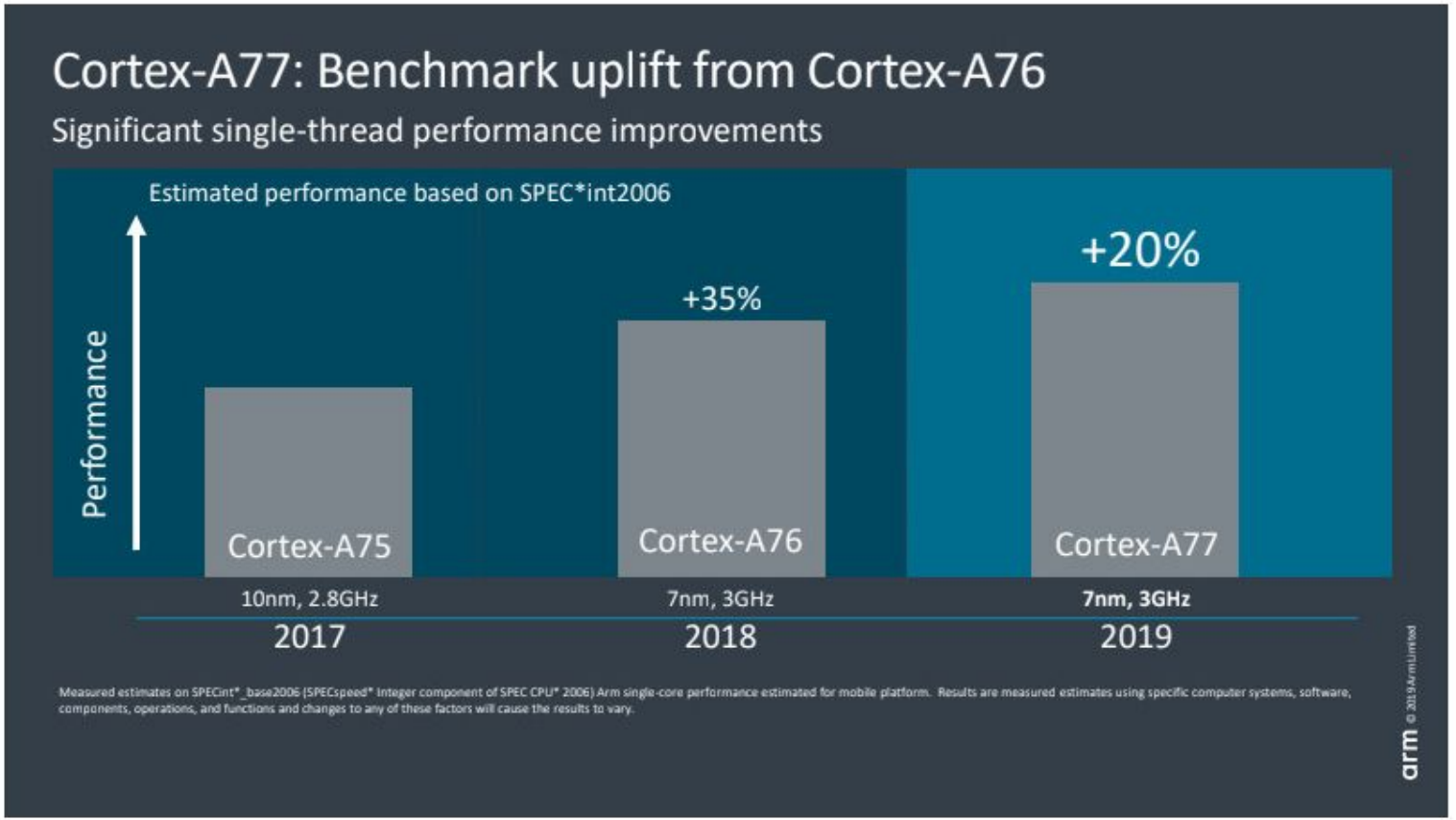
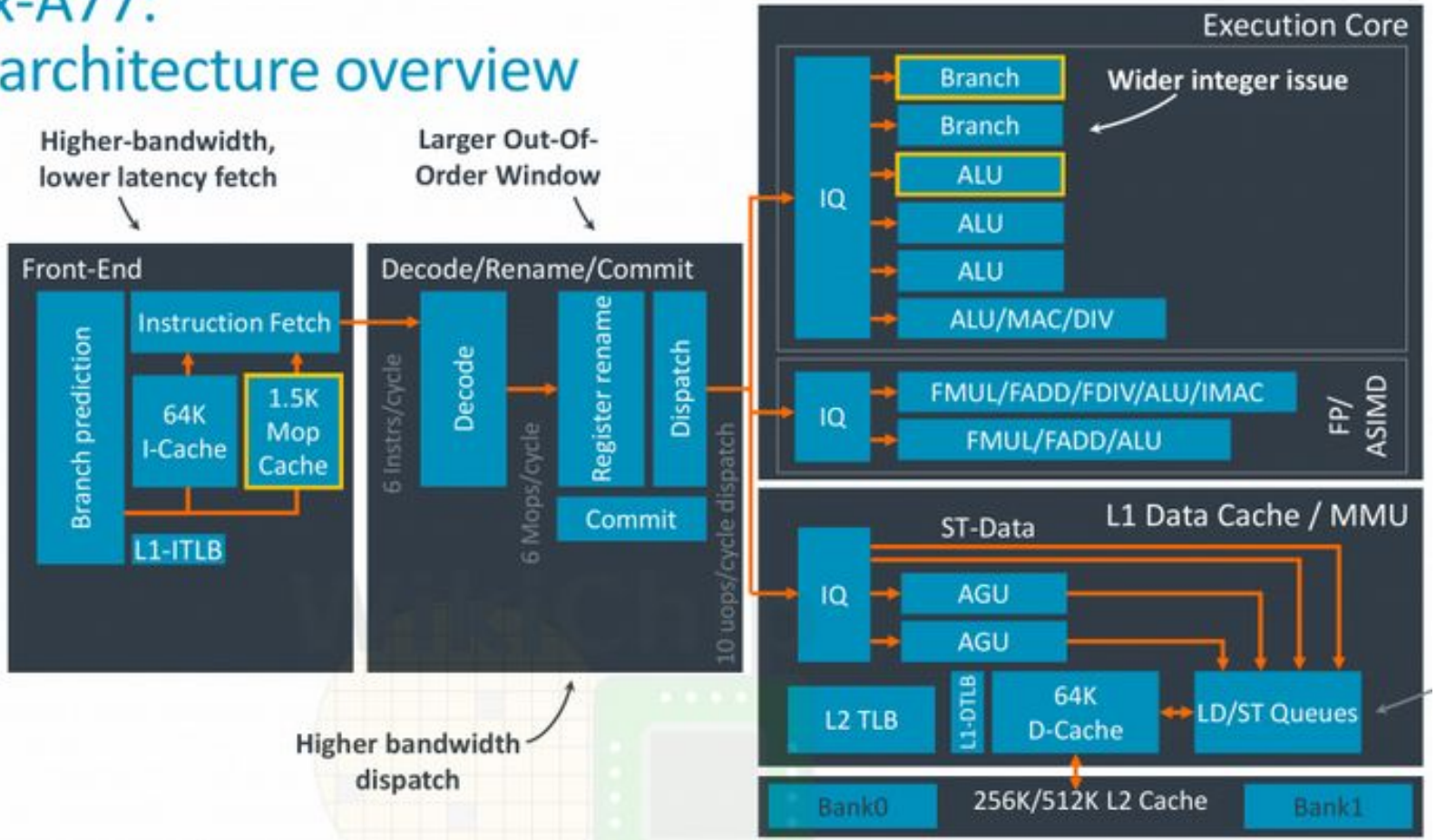
Agenda

- **Processor core microarchitecture**
- **Memory hierarchy**
- **Multicore support**

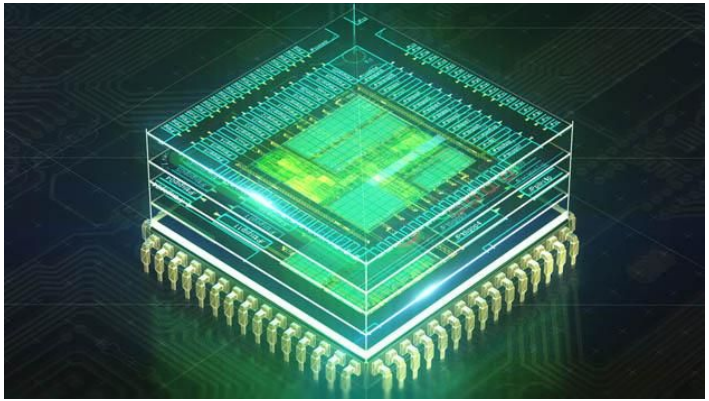
Improvements in Micro-architecture



Cortex-A77: Microarchitecture overview



MEMORY HIERARCHY



KEY FEATURES – L0 & L1

- L0 MOP Cache–1536 Entry
  (1.5 K)
- 64 KB L1, Instruction Private Cache Parity, ECC
  - L1 I - 4-way set associative,
  - 64-byte cache lines, Write-back,
  - *Optional parity protection*
- 64 KB L1, Data Private Cache
  - L1 D - 4-way set associative,
  - 64-byte cache lines, Write-back,
  - 4-cycle fastest load-to-use latency,
  - Optional ECC protection per 32 bits
  - Virtually Indexed, Physically Tagged
  - Implements Pseudo LRU Cache Replacement Policy.
  - Supports up to 20 outstanding non-prefetch misses.

KEY FEATURES – L2 & L3 Cache

- 256 KB/512 KB Private L2 Cache ECC
  - 8-way set associative
  - 9-cycle fastest load-to-use latency
  - optional ECC protection per 64 bits
  - Modified Exclusive Shared Invalid(MESI) coherency
  - Strictly inclusive of the L1 data cache & non-inclusive of the L1 instruction cache
  - Write-back
  - L2 can support up to 46 outstanding misses to the L3 which is located in the DSU itself
  - support up to 46 outstanding misses to the L3 which is located in the DSU itself.
- 512 KB – **4 MB** Shared L3 Cache ECC
  - Shared by all the cores in the cluster
  - Located in the DynamicIQ big.little Shared Unit(*DSU*)
  - 16-way set associative
  - 26-31 cycles load-to-use
  - up to two 32 bytes may be transferred from or to the L2 from the L3 cache
  - Up to 94 outstanding misses are supported from the L3 to main memory
- 1x or 2x 128-bit AMBA Cache ECC

KEY FEATURES

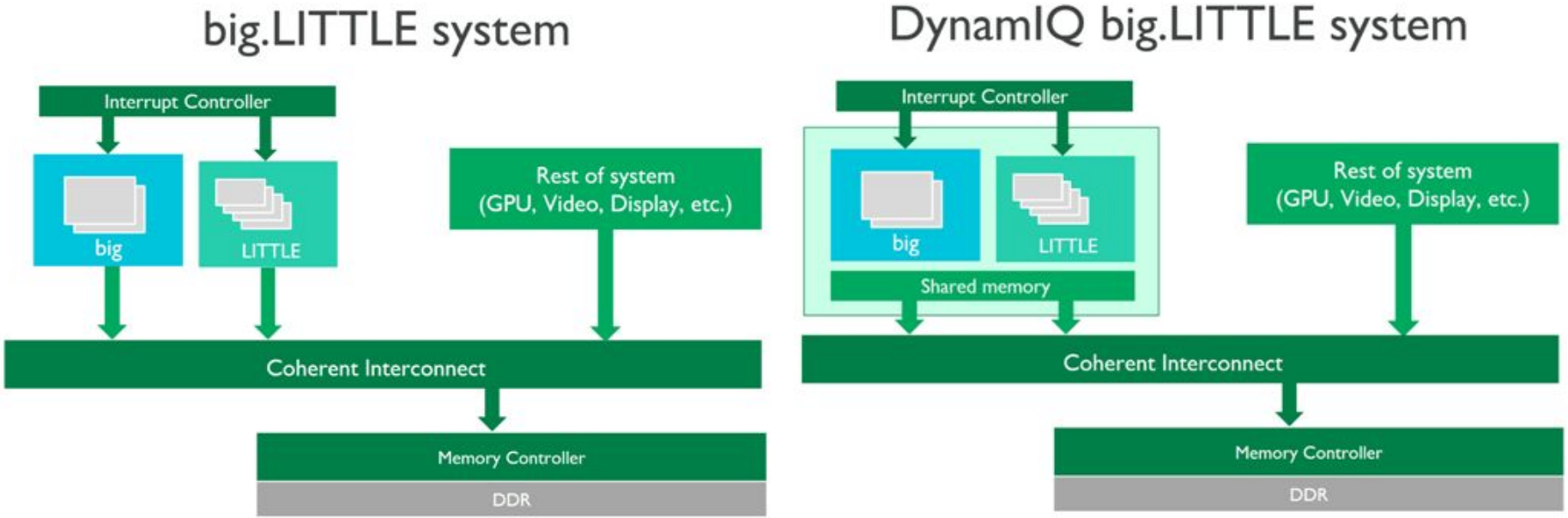
- Dedicated L1 TLB for instruction cache (ITLB).
  - 4 KiB, 16 KiB, 64 KiB, 2 MiB, and 32 MiB page sizes
  - 48-entry fully associative
- Dedicated L1 TLB for data cache (ITLB).
  - 48-entry fully associative
  - 4 KiB, 16 KiB, 64 KiB, 2 MiB, and 512 MiB page sizes
- *Unified* L2 TLB (STLB)
  1280-entry 5-way set associativity
- Physical Address Size is 40 Bits.
- System Aware Prefetching

Multicore and Thread-Level Parallelism

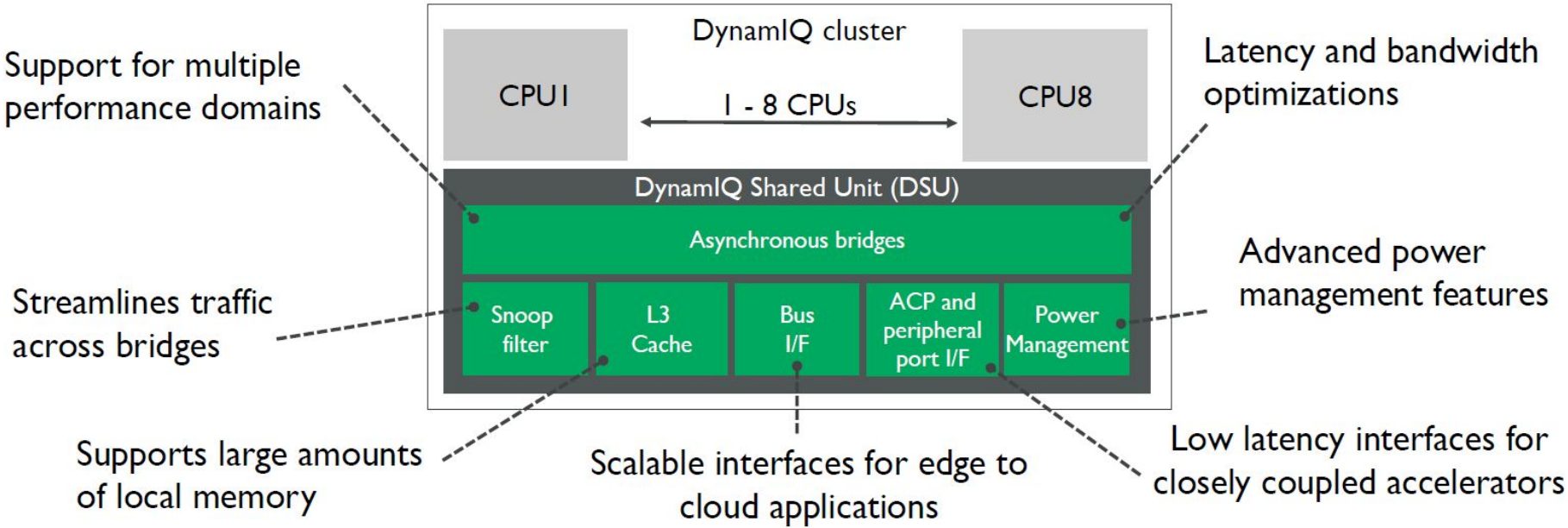
What is big.LITTLE?

- Heterogeneous processing architecture
- *big*: maximum compute performance
- *LITTLE*: maximum power efficiency

What changed in DynamIQ?



DynamIQ Shared Unit (DSU)

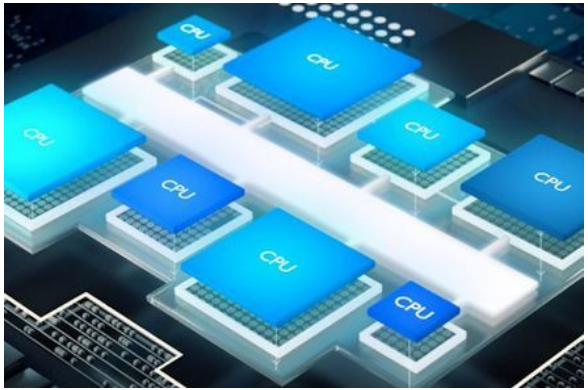


DynamIQ big.LITTLE introduces the following benefits:

- **Wider product differentiation** within a fully integrated solution
- **Higher user experience (UX)** from increased single thread performance
- **More energy efficiency** through advanced power management features

Use Cases of A77

- 5G
- Smartphones
- Artificial Intelligence and Machine Learning



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- Research Paper - Prefetch-Aware Shared-Resource Management for Multi-Core Systems

THANK YOU!!