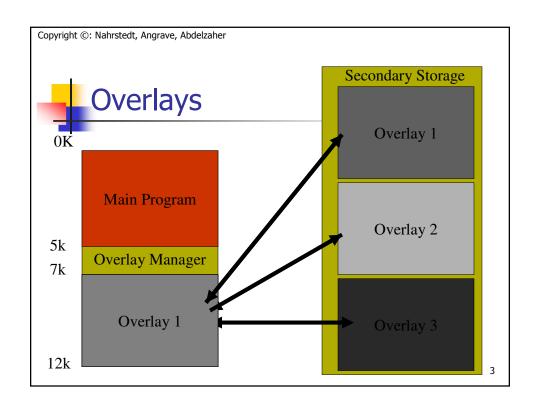
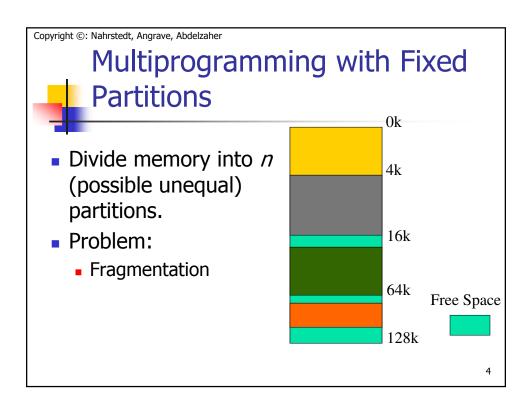


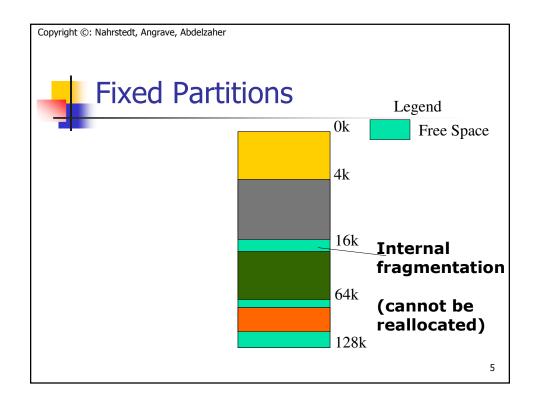


Memory Allocation

- Compile for overlays
- Compile for fixed Partitions
 - Separate queue per partition
 - Single queue
- Relocation and variable partitions
 - Dynamic contiguous allocation (bit maps versus linked lists)
- Fragmentation issues
- Swapping
- Paging







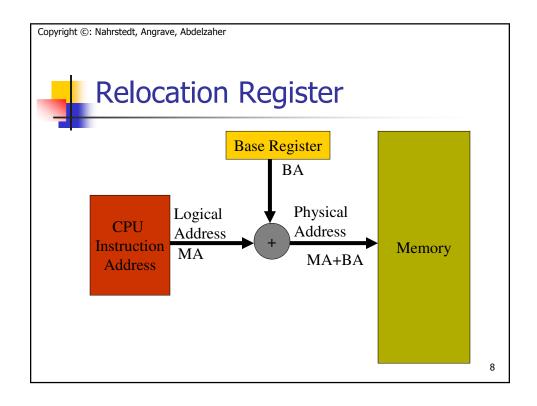


- Requires sorting the incoming jobs and putting them into separate queues
- Inefficient utilization of memory
 - when the queue for a large partition is empty but the queue for a small partition is full. Small jobs have to wait to get into memory even though plenty of memory is free.
- One single input queue for all partitions.
 - Allocate a partition where the job fits in.
 - Best Fit
 - Worst Fit
 - First Fit



Relocation

- Correct starting address when a program starts in memory
- Different jobs will run at different addresses
 - When a program is linked, the linker must know at what address the program will begin in memory.
- Logical addresses, Virtual addresses
 - Logical address space , range (0 to max)
- Physical addresses, Physical address space
 - range (R+0 to R+max) for base value R.
- User program never sees the real physical addresses
- Memory-management unit (MMU)
 - map virtual to physical addresses.
- Relocation register
 - Mapping requires hardware (MMU) with the base register



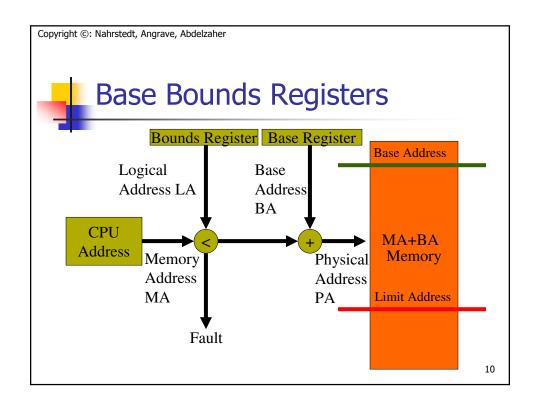
Question 1 - Protection

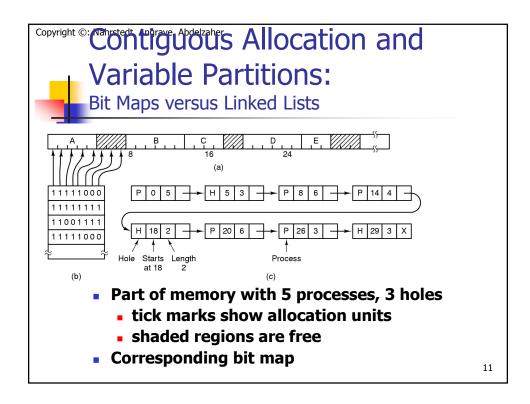
Problem:

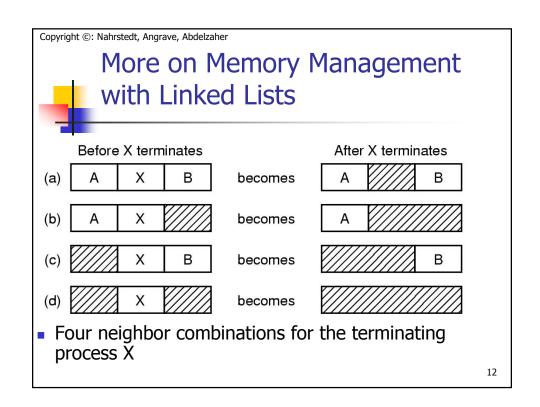
How to prevent a malicious process to write or jump into other user's or OS partitions

Solution:

Base bounds registers









Contiguous Variable Partition Allocation schemes

- Bitmap and link list
 - Which one occupies more space?
 - Depending on the individual memory allocation scenario.
 In most cases, bitmap usually occupies more space.
 - Which one is faster reclaim freed space?
 - On average, bitmap is faster because it just needs to set the corresponding bits
 - Which one is faster to find a free hole?
 - On average, a link list is faster because we can link all free holes together

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Storage Placement Strategies

- Best fit
 - Use the hole whose size is equal to the need, or if none is equal, the whole that is larger but closest in size.
 - Rationale?
- First fit
 - Use the first available hole whose size is sufficient to meet the need
 - Rationale?
- Worst fit
 - Use the largest available hole
 - Rationale?



Storage Placement Strategies

- Every placement strategy has its own problem
 - Best fit
 - Creates small holes that cant be used
 - Worst Fit
 - Gets rid of large holes making it difficult to run large programs
 - First Fit
 - Creates average size holes

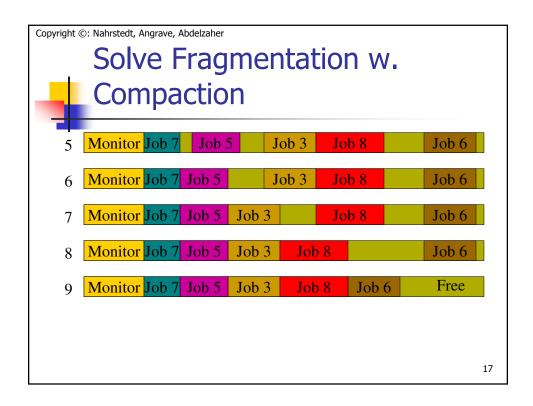
15

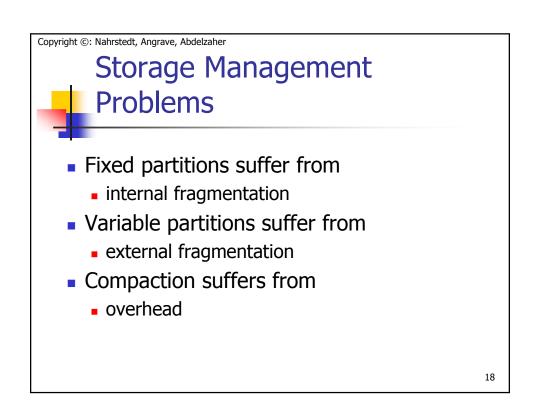
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How Bad Is Fragmentation?

- Statistical arguments Random sizes
- First-fit
- Given N allocated blocks
- 0.5*N blocks will be lost because of fragmentation
- Known as 50% RULE

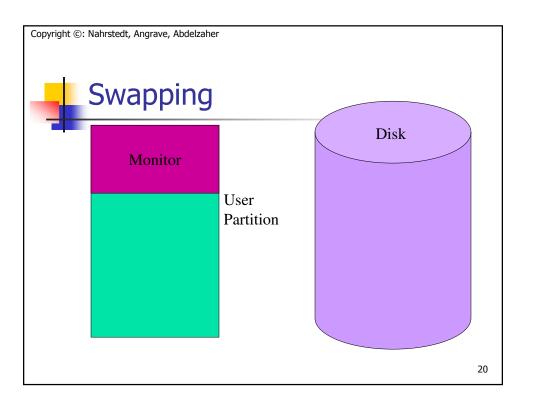


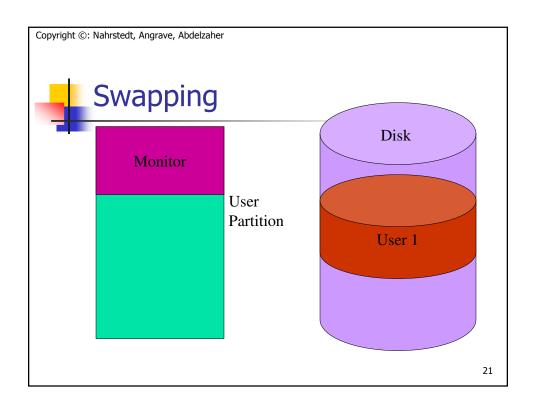


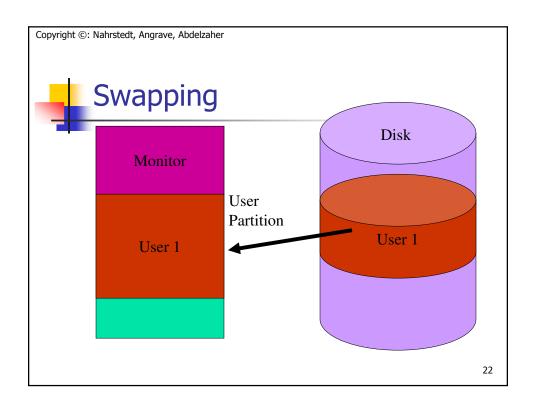
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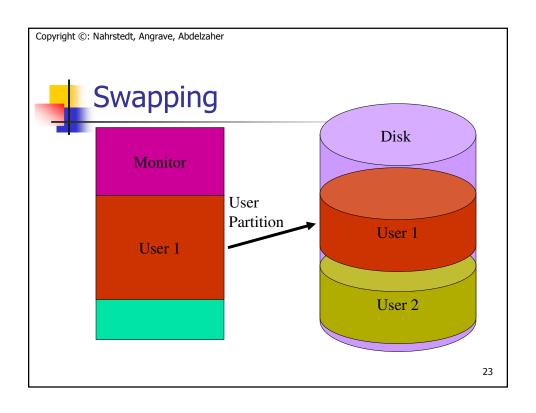
Question

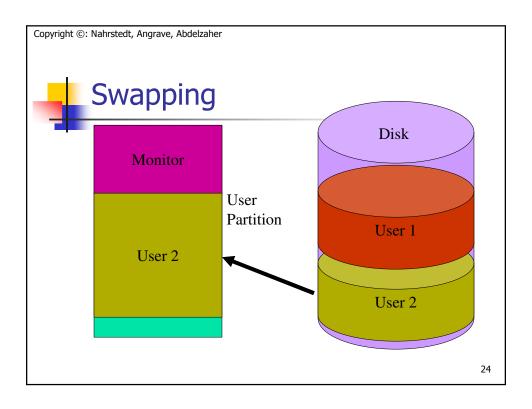
What if there are more processes than what could fit into the memory?

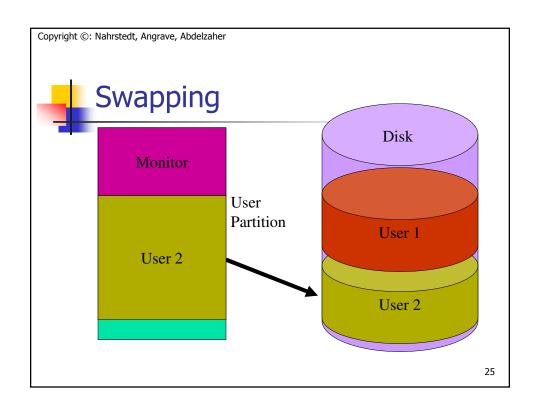


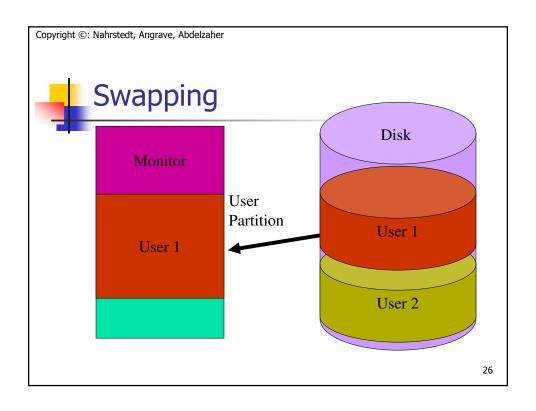


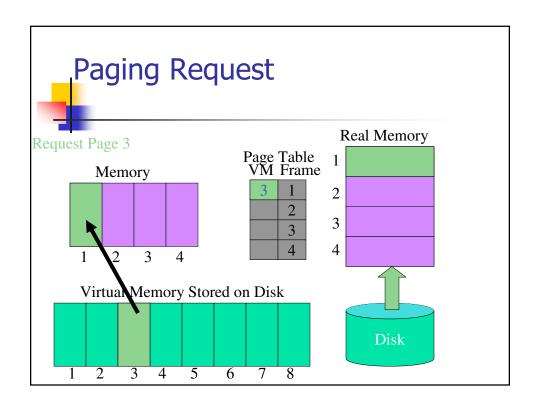


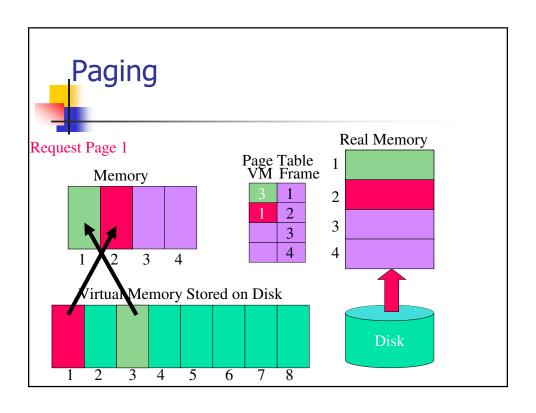


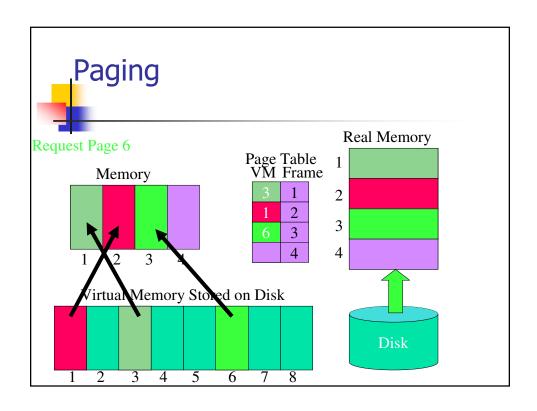


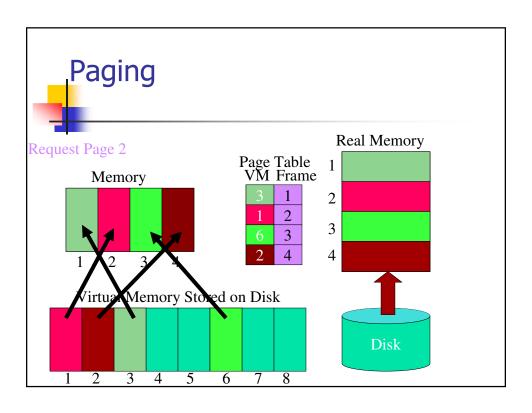


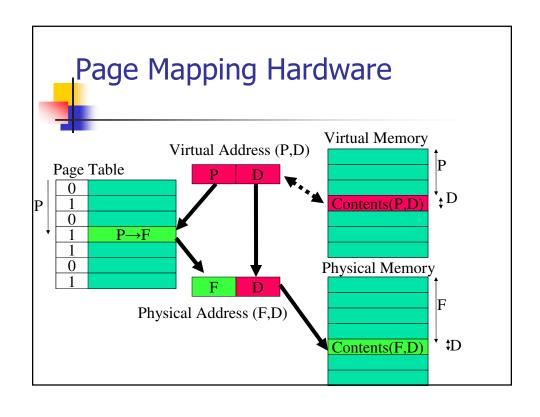


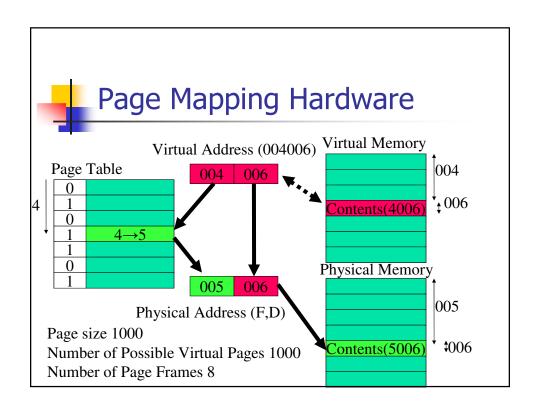














Page Fault

- Access a virtual page that is not mapped into any physical page
 - A fault is triggered by hardware
- Page fault handler (in OS's VM subsystem)
 - Find if there is any free physical page available
 - If no, evict some resident page to disk (swapping space)
 - Allocate a free physical page
 - Load the faulted virtual page to the prepared physical page
 - Modify the page table



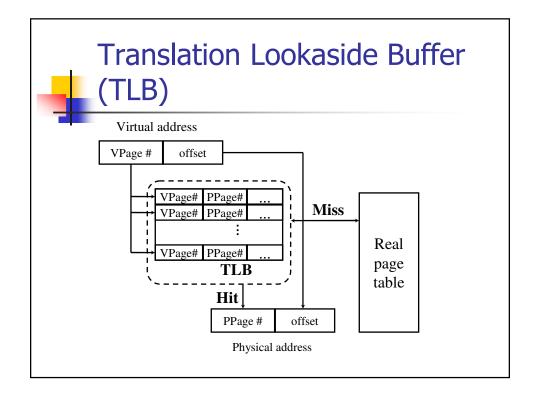
Paging Issues

- Page size is 2ⁿ
 - usually 512 bytes, 1 KB, 2 KB, 4 KB, or 8 KB
 - E.g. 32 bit VM address may have 2²⁰ (1 MB) pages with 4k (2¹²) bytes per page
- Page table:
 - 2²⁰ page entries take 2²² bytes (4 MB)
 - page frames must map into real memory
 - Page Table base register must be changed for context switch
- No external fragmentation; internal fragmentation on last page only



Virtual-to-Physical Lookups

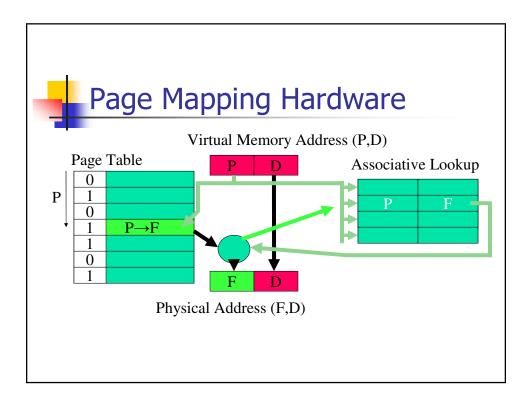
- Programs only know virtual addresses
 - The page table can be extremely large
- Each virtual address must be translated
 - May involve walking hierarchical page table
 - Page table stored in memory
 - So, each program memory access requires several actual memory accesses
- Solution: cache "active" part of page table
 - TLB is an "associative memory"





TLB Function

- If a virtual address is presented to MMU, the hardware checks TLB by comparing all entries simultaneously (in parallel).
- If match is valid, the page is taken from TLB without going through page table.
- If match is not valid
 - MMU detects miss and does a page table lookup.
 - It then evicts one page out of TLB and replaces it with the new entry, so that next time that page is found in TLB.





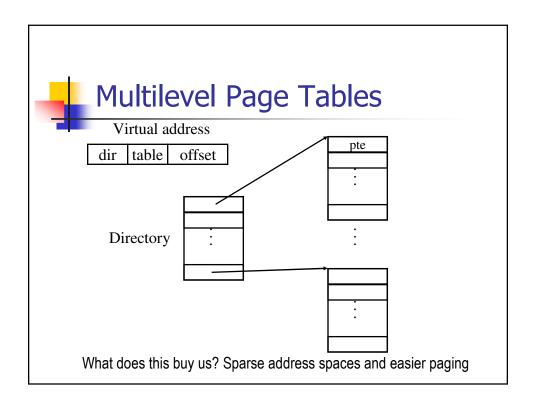
Effective Access Time

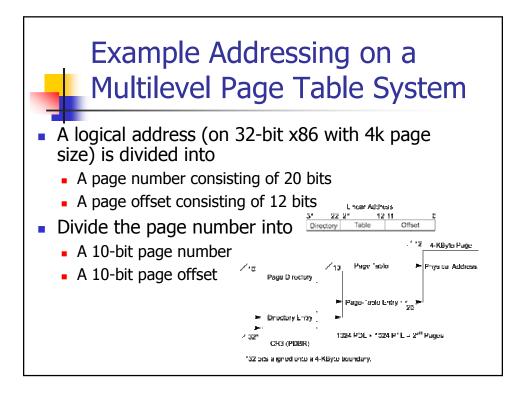
- TLB lookup time = σ time unit
- Memory cycle = $m \mu s$
- ■TLB Hit ratio = η
- Effective access time
 - $Eat = (m + \sigma) \eta + (2m + \sigma)(1 \eta)$
 - $Eat = 2m + \sigma m\eta$



Multilevel Page Tables

- Since the page table can be very large, one solution is to page the page table
- Divide the page number into
 - An index into a table of second level page tables
 - A page within a second level page table
- Advantage
 - No need to keep all the page tables in memory all the time
 - Only recently accessed memory's mapping need to be kept in memory, rest can be fetched on demand

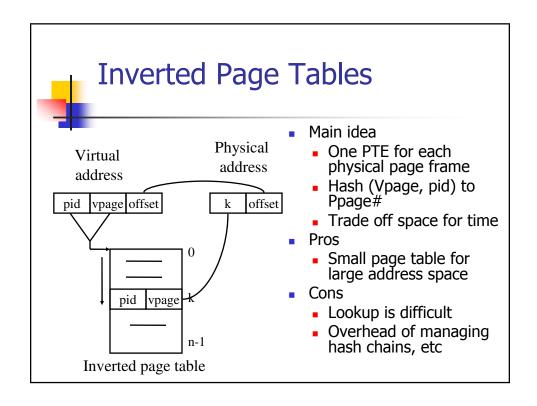






Multilevel Paging and Performance

Since each level is stored as a separate table in memory, converting a logical address to a physical one with a n-level page table may take n+1 memory accesses. Why?





Paging

- Provide user with virtual memory that is as big as user needs
- Store virtual memory on disk
- Cache parts of virtual memory being used in real memory
- Load and store cached virtual memory without user program intervention