

# Binary Math, Two's Complement and Logic Gates

The background of the slide features a classical statue, likely the 'Alma Mater' statue at the University of Illinois, set in a wooded area. The entire image is overlaid with a semi-transparent red filter. The statue is a female figure in a long, flowing robe, standing on a pedestal. The trees in the background are bare, suggesting a late autumn or winter setting.

**CS 240 - The University of Illinois**

Wade Fagen-Ulmschneider

August 31, 2021

# Dream Computer



# Binary Addition

**0b 010011**

**+0b 001001**

0b 0011

+0b 0111

# Negative Numbers

0b 010011

-0b 001001

0b 0011

-0b 0111



0b 0011  $\Rightarrow$  0011

-0b 0111  $\Rightarrow$  + 1111

$\Rightarrow$  10010

# Two's Complement

# Two's Complement

**Big Idea:** Represent numbers signed numbers in binary in a way that:

# Two's Complement

Method:

$$-17 =$$

$$-4 =$$

$$-1 =$$

42

-18



18

-42

-42

- 32

# Overflow Detection

-31

- 42

# Towards Multiplication

$$10 \times 2 =$$

$$10 \times 4 =$$

$$10 \times 9 =$$



**Left Shift:**

**Right Shift:**

# Logic Gates

The image features a central photograph of the Alma Mater statue at the University of California, Berkeley. The statue is a large, classical-style sculpture of a woman in a long, flowing gown, standing on a pedestal. In the foreground, a crowd of people is visible, some looking towards the statue. The background consists of bare tree branches. The entire scene is overlaid with a semi-transparent orange filter. The text "Logic Gates" is centered over the image in a large, white, sans-serif font.

# Logic Gate #1

# Logic Gate #2

# Logic Gate #3

# Logic Gate #4

# Functionally Complete Gate?

A	B	A&B	A   B	A^B	
0	0	0	0	0	
0	1	0	1	1	
1	0	0	1	1	
1	1	1	1	0	

# Hardware Schematics



## CD4001B, CD4002B, CD4025B Types

### CMOS NOR Gates

High-Voltage Types (20-Volt Rating)

Quad 2 Input – CD4001B  
Dual 4 Input – CD4002B  
Triple 3 Input – CD4025B

■ CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shroud small-outline packages (PW and PWR suffixes).

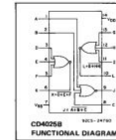
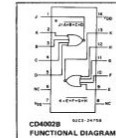
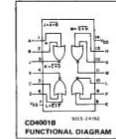
### Features:

- Propagation delay time = 60 ns (typ.) at  $C_L = 50$  pF,  $V_{DD} = 10$  V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 15 V and 25°C
- Noise margin lower full package temperature range:
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

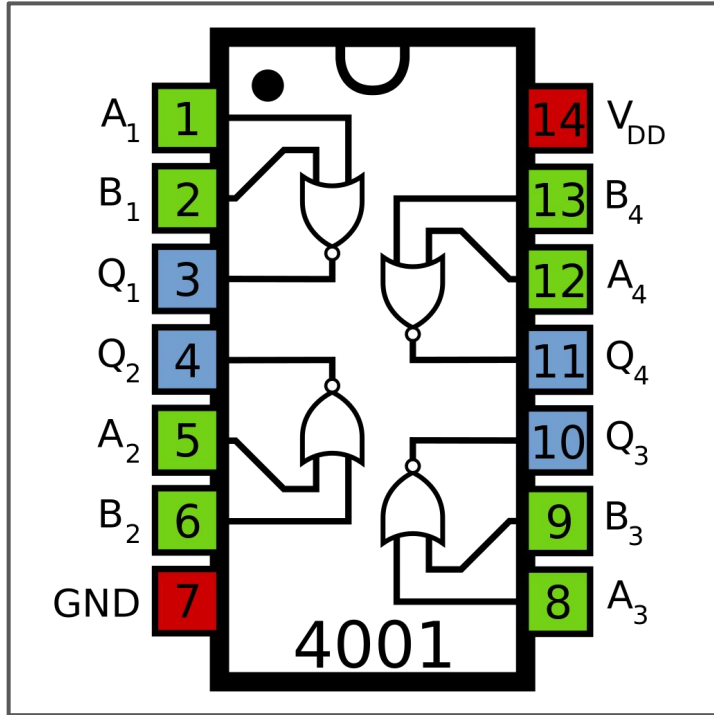
### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	$V_D$ (V)	$V_{IH}$ (V)	$V_{DD}$ (V)	-55			+25		+125		
				-40	+05	+125	Min.	Typ.			Max.
Quiescent Device Current, $I_{DD}$ Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	$\mu$ A
Output Low (Sink) Current, $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.30	0.51	1	-	
Output High (Source) Current, $I_{OH}$ Min.	0.5	1.0	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
Output Voltage, $V_{OH}$ Max.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.30	-0.51	1	-	mV
Input Low Voltage, $V_{IL}$ Max.	0.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
Input High Voltage, $V_{IH}$ Min.	1.5	1.5	15	4.2	4	2.8	2.4	3.4	-6.8	-	
Input Current, $I_{IH}$ Max.	-	0.5	5	0.05	-	-	0	0.05	-	-	$\mu$ A
Input Current, $I_{IH}$ Max.	-	0.10	10	0.05	-	-	0	0.05	-	-	$\mu$ A
Output Voltage, $V_{OH}$ Max.	-	0.5	5	4.95	4.95	4.95	4.95	5	-	-	V
Output Voltage, $V_{OH}$ Max.	-	0.10	10	9.95	9.95	9.95	9.95	10	-	-	V
Input Low Voltage, $V_{IL}$ Max.	0.5	0.5	5	1.5	-	-	-	1.5	-	-	V
Input High Voltage, $V_{IH}$ Min.	1.5	1.5	15	4	-	-	-	4	-	-	V
Input Current, $I_{IH}$ Max.	0.18	18	+0.1	+0.1	11	11	-	-	-	-	$\mu$ A





# Hardware Schematics



**TEXAS INSTRUMENTS**  
Data sheet prepared from Harris Semiconductor  
SICH5015C - Revised August 2003

## CD4001B, CD4002B, CD4025B Types

### CMOS NOR Gates

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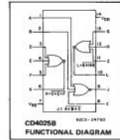
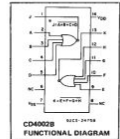
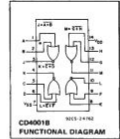
### Features:

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- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 15 V and 25°C
- Noise margin (over full package temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V

Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"

### STATIC ELECTRICAL CHARACTERISTICS

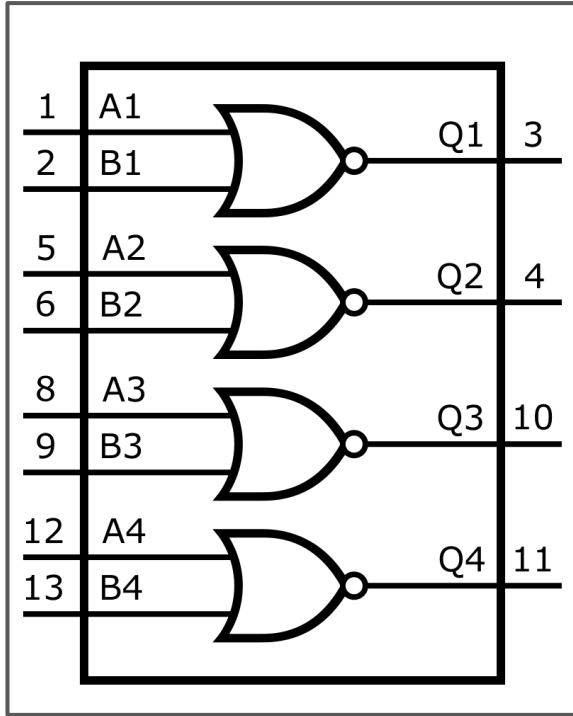
CHARACTERISTIC	CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)										UNITS			
	V <sub>O</sub>	V <sub>IH</sub>	V <sub>DD</sub>	-55						+25						
				-55	-40	+05	+125	Min.	Typ.	Max.	Min.	Typ.		Max.		
Quiescent Device Current, I <sub>DD</sub> Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	-	-	-	-	-	$\mu$ A
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5	-	-	-	-	-	
	-	0.15	15	1	1	30	30	-	0.01	1	-	-	-	-	-	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.30	0.51	1	-	-	-	-	-	-	$\mu$ A
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	-	-	-	-	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	-	-	-	-	-	mA
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.30	-0.51	1	-	-	-	-	-	-	$\mu$ A
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	-	-	-	-	-	
	3.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	-	-	-	-	-	
Output Voltage, V <sub>OL</sub> Max.	-	0.5	5	-	-	0.05	-	0	0.05	-	-	-	-	-	-	V
	-	0.10	10	-	-	0.05	-	0	0.05	-	-	-	-	-	-	
	-	0.15	15	-	-	0.05	-	0	0.05	-	-	-	-	-	-	
Output Voltage, V <sub>DH</sub> Min.	-	0.5	5	4.95	4.95	4.95	4.95	5	-	-	-	-	-	-	-	V
	-	0.10	10	9.95	9.95	9.95	9.95	10	-	-	-	-	-	-	-	
	-	0.15	15	14.95	14.95	14.95	15	-	-	-	-	-	-	-	-	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	-	5	1.5	-	-	-	-	1.5	-	-	-	-	-	-	V
	1.9	-	10	3	-	-	-	-	3	-	-	-	-	-	-	
	1.5, 13.5	-	15	4	-	-	-	-	4	-	-	-	-	-	-	
Input High Voltage, V <sub>IH</sub> Min.	0.5	-	5	3.5	-	-	-	-	3.5	-	-	-	-	-	-	V
	1	-	10	7	-	-	-	-	7	-	-	-	-	-	-	
	1.5	-	15	11	-	-	-	-	11	-	-	-	-	-	-	
Input Current, I <sub>IN</sub> Max.	0.18	18	+0.1	+0.1	11	11	-	-	-	-	-	-	-	-	-	$\mu$ A
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	



3  
COMMERCIAL CMOS  
HIGH VOLTAGE CH



# Hardware Schematics



**TEXAS INSTRUMENTS**  
Data sheet prepared from Harris Semiconductor  
SICH915C - Revised August 2003

## CD4001B, CD4002B, CD4025B Types

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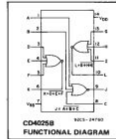
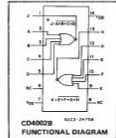
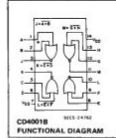
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■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specification for Description of "B" Series CMOS Devices"

### STATIC ELECTRICAL CHARACTERISTICS

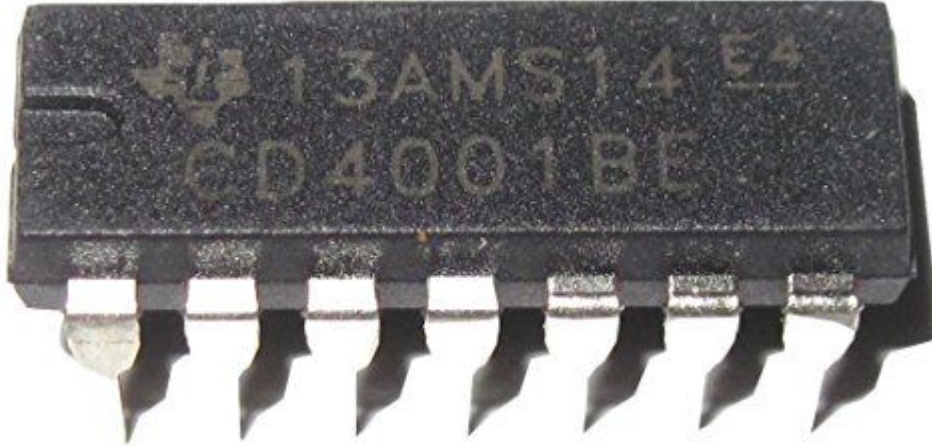
CHARACTERISTIC	CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)										UNITS	
	$V_D$ (0)	$V_{IH}$ (1)	+25											
			-55	-40	+05	+125	Min.	Typ.	Max.					
Quiescent Device Current, $I_{DD}$ Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25				$\mu$ A
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5				
	-	0.15	15	1	1	30	30	-	0.01	1				
Output Low (Sink) Current, $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.30	0.51	1				$\mu$ A	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6					
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8					
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.30	-0.51	1				mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2					
	3.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6					
Output Voltage, $V_{OL}$ Max.	-	0.5	5	0.05		0		0.05					V	
	-	0.10	10	0.05		0		0.05						
	-	0.15	15	0.05		0		0.05						
Output Voltage, $V_{OH}$ Min.	-	0.5	5	4.95		4.95		5					V	
	-	0.10	10	9.95		9.95		10						
	-	0.15	15	14.95		14.95		15						
Input Low Voltage, $V_{IL}$ Max.	0.5, 4.5	-	5	1.5		-		1.5					V	
	1.9	-	10	3		-		3						
	1.5, 13.5	-	15	4		-		4						
Input High Voltage, $V_{IH}$ Min.	0.5	-	5	3.5		3.5		-					V	
	1	-	10	7		7		-						
	1.5	-	15	11		11		-						
Input Current, $I_{IH}$ Max.	0.18	18	+0.1	+0.1	11	11	-	-	-	-	-	-	$\mu$ A	
	-	-	-	-	-	-	-	-	-	-	-	-		
	-	-	-	-	-	-	-	-	-	-	-	-		



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# Hardware Schematics



**TEXAS INSTRUMENTS**  
Data sheet prepared from Harris Semiconductor  
SICH5015C - Revised August 2003

## CMOS NOR Gates

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## CD4001B, CD4002B, CD4025B Types

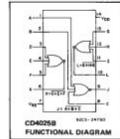
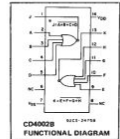
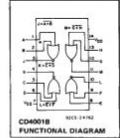
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### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS		LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
	$V_D$ (V)	$V_{IH}$ (V)	-55				+125				
			Typ.	Max.	Typ.	Max.					
Quiescent Device Current, $I_{DD}$ Max.	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	$\mu$ A	
	5	10	0.5	0.5	15	15	-	0.01	0.5		
	15	15	1	1	30	30	-	0.01	1		
Output Low (Sink) Current, $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.30	0.51	1	mA	
	0.5	10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	15	15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.30	-0.51	-1	mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2		
	3.5	10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6		
Output Voltage Low Level, $V_{OL}$ Max.	0.5	5	-	0.05	-	-	0	0.05	-	V	
	10	10	-	0.05	-	-	0	0.05	-		
	15	15	-	0.05	-	-	0	0.05	-		
Output Voltage High Level, $V_{OH}$ Min.	0.5	5	4.95	4.95	4.95	4.95	5	-	-	V	
	10	10	9.95	9.95	9.95	10	-	-	-		
	15	15	14.95	14.95	14.95	15	-	-	-		
Input Low Voltage, $V_{IL}$ Max.	0.5, 4.5	-	5	1.5	-	-	-	1.5	-	V	
	1.0	-	10	3	-	-	-	3	-		
	1.5, 13.5	-	15	4	-	-	-	4	-		
Input High Voltage, $V_{IH}$ Min.	0.5	-	5	3.5	-	-	3.5	-	-	V	
	1	-	10	7	-	-	7	-	-		
	1.5	-	15	11	-	-	11	-	-		
Input Current $I_{IH}$ Max.	0.18	18	+0.1	+0.1	-11	-11	-	-10	-5	$\mu$ A	
	10.1	10.1	-	-	-	-	-	-	-		



3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs



# Binary Addition

# Binary Addition

Half Adder:

A	B	A + B	SUM	CARRY

# Half Adder Circuit Diagram

# Binary Addition

Full Adder:

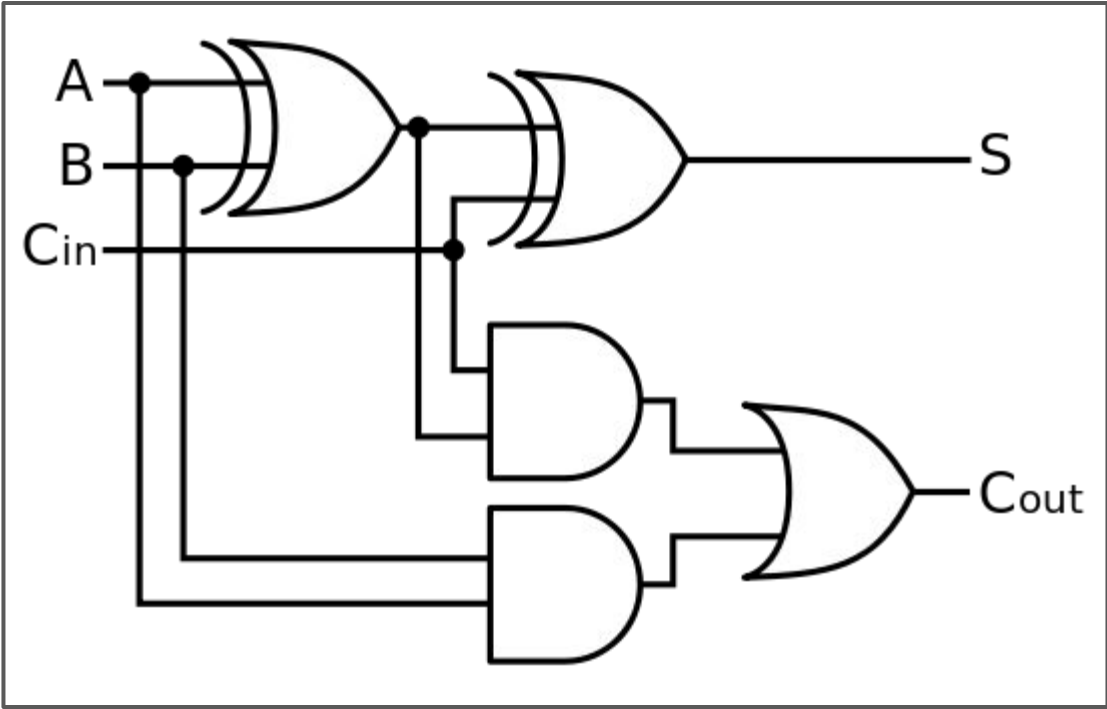




# Full Adder Circuit Diagram

# Full Adder Circuit Diagram

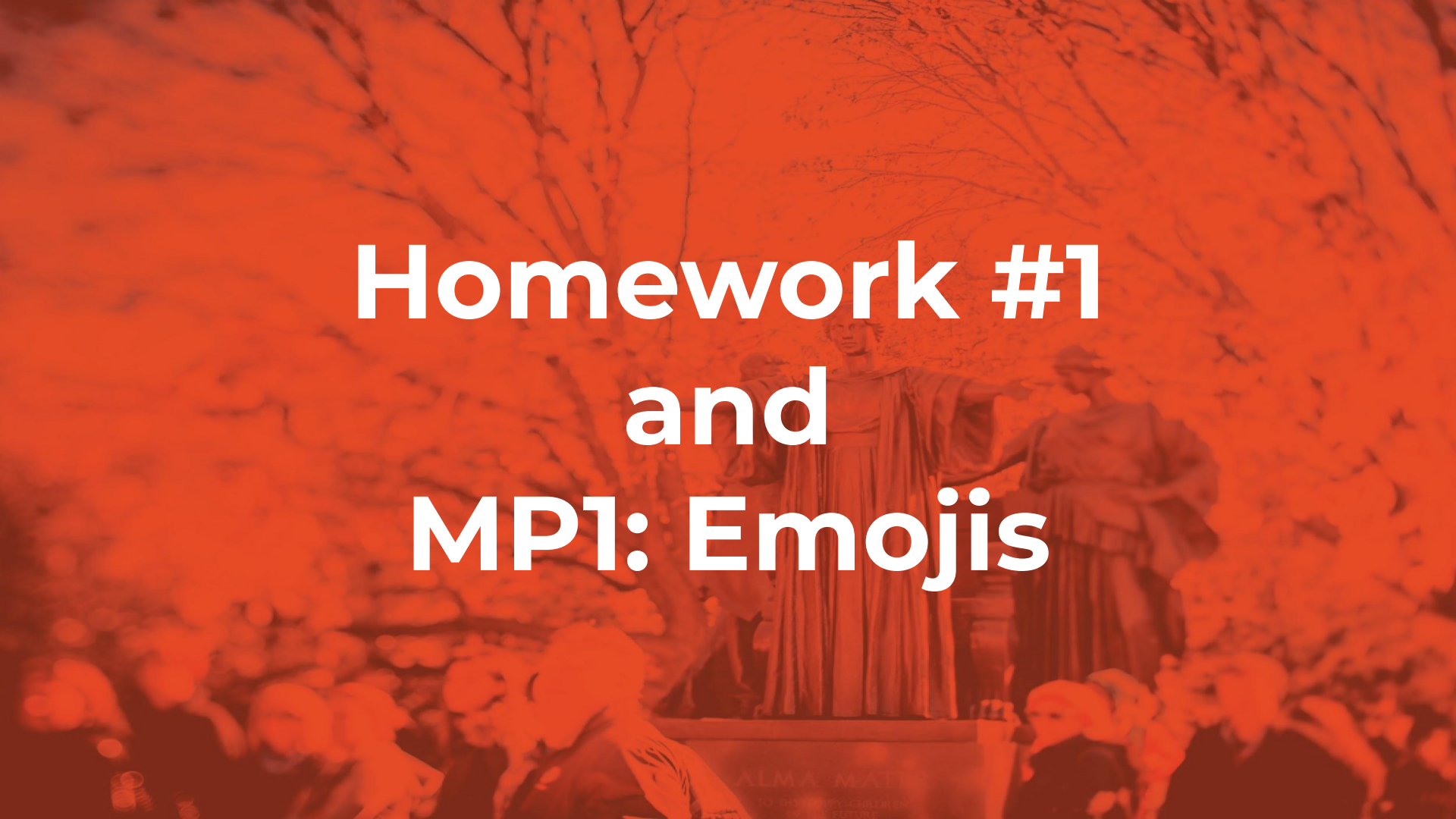
*...or, with only "simple gates":*



# What more do we need?

# Ripple Carry Adder (RCA)

# Disadvantages



# Homework #1 and MP1: Emojis