

1. Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, and 11. Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

Solution:

2 miss, 3 miss, 11 miss, 16 miss, 21 miss, 13 miss, 64 miss, 48 miss, 19 miss, 11 hit, 3 miss, 22 miss, 4 miss, 27 miss, 6 miss, 11 miss.

Index	Cache Contents
0	16 64 48
1	
2	2
3	3 19 3
4	4
5	21
6	22 6
7	
8	
9	
10	
11	11 27 11
12	
13	13
14	
15	

2. Assume that 33% of the instructions in a program are data accesses. The cache hit ratio is 97% and the hit time is one cycle, but the miss penalty is 20 cycles.

$$\begin{aligned}
 AMAT &= \text{Hit time} + (\text{Miss rate} \times \text{Miss penalty}) \\
 &= 1 \text{ cycle} + (3\% \times 20 \text{ cycles}) \\
 &= 1.6 \text{ cycles}
 \end{aligned}$$

Let I be the total number of instructions.

$$\begin{aligned}
 \text{Memory Stall Cycles} &= \text{Memory Accesses} \times \text{Miss rate} \times \text{Miss penalty} \\
 &= 0.33I \times 0.03 \times 20 \\
 &= 0.198I
 \end{aligned}$$

If the cache was perfect and never missed, the AMAT would be one cycle. But even with just a 3% miss rate, the AMAT here increases 1.6 times!

3. The Corleone2004 processor has two levels of data caches, with the characteristics shown below. You can also assume that it takes 50 clock cycles to request and complete a 32-byte transfer between main memory and the L2 cache.

Find the average memory access time (AMAT) for both the L2 and L1 cache.

Table 1. Cache Parameters for Q1

	L1	L2
Data Size	32KB	256KB
Block Size	8bytes	32bytes
Associativity	Direct-mapped	4-way
Hit Time	1 cycle	19 cycles
Miss Rate	5%	2%

Solution:

Per assumption, it takes 50 cycles to retrieve 32 bytes of data from main memory, so this is the miss penalty for the L2 cache.

$$AMAT_{L2} = 19 \text{ cycles} + (0.02 \times 50 \text{ cycles}) = 20 \text{ cycles}$$

The L2 AMAT is 20 cycles.

AMAT of L2 is the miss penalty for the L1 cache. When there is a miss in the primary cache, the average time to get data from the L2 is 20 cycles.

$$AMAT_{L1} = 1 \text{ cycle} + (0.05 \times 20) \text{ cycles} = 2 \text{ cycles.}$$

So, the AMAT of the L1 cache is 2 cycles.