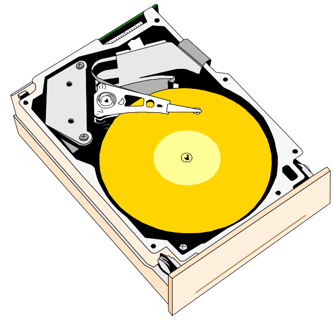
CS232 Disk/Bus example problems:



1) Assume a disk has the following specifications.

- An average seek time of 3ms
- A 6000 RPM rotational speed
- A 10MB/s average transfer rate
- 2ms of overheads for making a request

How long does it take to read a random 1,024 byte sector?

- The average rotational delay is: .5 x (1 minute/6000 rev) = 5ms.
- The transfer time will be about: (1024 bytes / 10 MB/s) = 0.1ms.
- The response time is then: 3ms + 5ms + 0.1ms + 2ms = 10.1ms.

How long would it take to read a whole track (512 sectors) selected at random, if the sectors could be read in any order?

Since the sectors can be read in any order, there is no rotational delay. The seek time and overhead remain the same. The transfer time is: (512kB / 10MB/s) = ~51.2ms

The response time is: 3ms + 0ms + 51.2ms + 2ms = 56.2ms

2) Assume the following system:

- A CPU and memory share a 32-bit bus running at 100MHz.
- The memory needs 50ns to access a 64-bit value from one address.

For this system, a single read can be performed in eight cycles or 80ns for an effective bandwidth of (12.5 x 10^6 reads/second) x (8 bytes/read) = 100MB/s.

If the memory was widened, such that 128-bit values could be read in 50ns, what is the new effective bandwidth?

A 128-bit read can now be done in (1 + 5 + 4) = 10 cycles, or 100ns. This yields an effective bandwidth of (10 x 10^6 reads/second) x (16 bytes/read) = 160MB/s.

What is the bus utilization (fraction of cycles the bus is used) to achieve the above bandwidth?

Of the 10 cycle access, sending the address takes 1 cycle, transferring the data takes 4 cycle = (5/10) = 50%.

If utilization were 100% (achievable by adding additional memories), what effective bandwidth would be achieved?

Since we have 1 address transfer for every 4 data transfers the effective bandwidth would be 80% of the total bandwidth: (32b x 100Mhz) x 80% = (400MB/s) x .8 = 320MB/s.