Lecture 7 - 8: Circuit Analysis - KCL, Node Voltage Analysis

Learning Objectives:

1. **Define Kirchhoff's current law (KCL)**
2. **Compute voltages in simple circuits using KCL**
3. **Use node voltage analysis method to compute node voltages**
4. **Derive current division formula and analyze the limitations of of current divider**

Last few lectures we used loop analysis technique to determine currents in a circuit. Loop analysis technique is based on the Kirchhoff's voltage law. Node voltage analysis, based on Kirchhoff's Current Law (KCL), is another procedural method that can be used to determine the voltage at a various nodes in a circuit.

1. Kirchhoff's Current Law (KCL)

KCL states that the **algebraic** sum of currents entering or exiting a node is zero. As we discussed earlier a **node** is a point in a circuit where two or more elements are connected together. Consider some circuits shown in Fig. 1.1 below, the algebraic sum of currents in each case is also shown. As shown in this examples we take currents coming out of a node as positive. Note that the actual current might be coming into the node but that will not affect our computations.

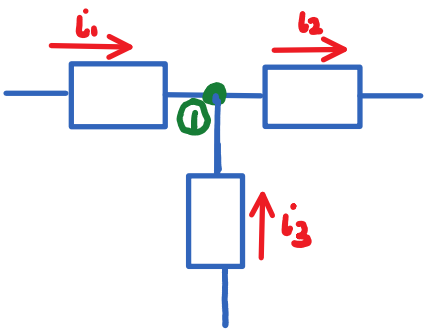


Fig. 1.1(a)

$-i_1 + i_2 - i_3 = 0$

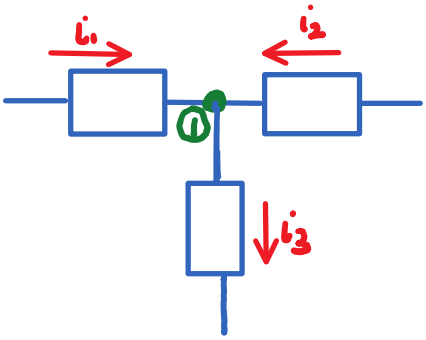


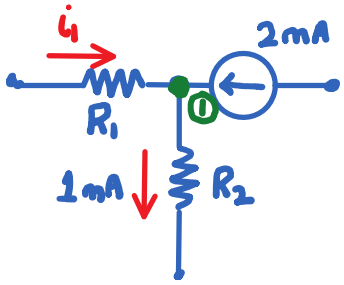
Fig. 1.1(b)

$-i_1 - i_2 + i_3 = 0$

Fig 1.1. Illustration of KCL

Notation: The currents leaving a node are taken as positive.

Example 1.1: Apply KCL to node 1 shown in circuit below and compute current i_1.



Solution: $-i_1 + 1 - 2 = 0$

$\Rightarrow i_1 = -1\ \text{mA}$

Note that in example 1.1, current i_1 came out negative. This just means that the actual current leaving node 1. We will see in further examples that assuming a certain direction of current does not constrain us in any way.

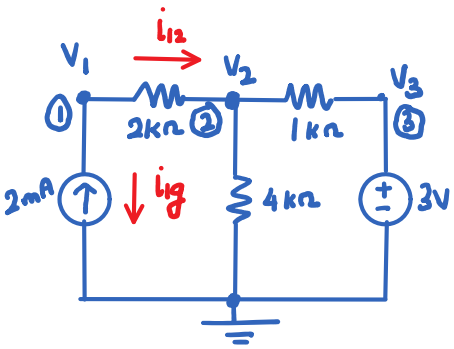
2. Node voltage analysis

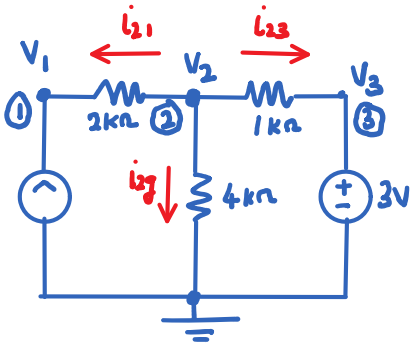
We will now apply KCL to larger circuits with many nodes and compute voltages as different nodes in the circuit. As mentioned earlier this procedure is called node voltage analysis. Thus, loop analysis method discussed earlier is based on KVL and node voltage analysis is based on KCL. It should be noted that since in

node voltage analysis we are solving for the voltage at a node, we must identify a **ground node** as a reference point. For most of the problems we discuss in this class, the ground node will be clearly specified. Node voltage analysis involves the following steps:

- **Identify the nodes in a circuit.**
- **For each node assume that the currents are leaving the node. An incorrect assumption will still yield a correct voltage as long as KCL is correctly applied.**
- **Set up node equations.**
- **Solve node equations to obtain node voltages.**

Example 2.1: Compute voltages $\mathbf{V_1, V_2, V_3}$ **in** the circuit shown below.





Solution:

By inspection: $\mathbf{V_3 = 3\ V}$

Node 1 (KCL): $\mathbf{i_{12} + i_{1g} = 0}$

By Ohm's Law: $\mathbf{i_{12} = \frac{V_{12}}{2k\Omega} = \frac{V_1 - V_2}{2}}$

By Inspection: $\mathbf{i_{1g} = -2mA}$

Hence Node 1 equation can be written as,

Node 1: $\mathbf{\frac{V_1 - V_2}{2} - 2 = 0 \Rightarrow V_1 - V_2 = 4}$ **(1)**

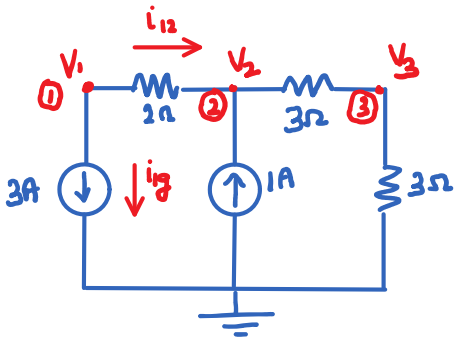
Node 2: $\mathbf{i_{21} + i_{2g} + i_{23} = 0}$

Ohms' Law: $\mathbf{-2 + \frac{V_2 - 0}{4} + \frac{V_2 - V_3}{2} = 0}$

$$\mathbf{5V_2 - 12 = 8 \Rightarrow V_2 = 4\ V}$$

From (1), $\mathbf{V_1 = 8V}$

Example 2.2: Find voltages $\mathbf{V_1, V_2, V_3}$ in the circuit shown below.



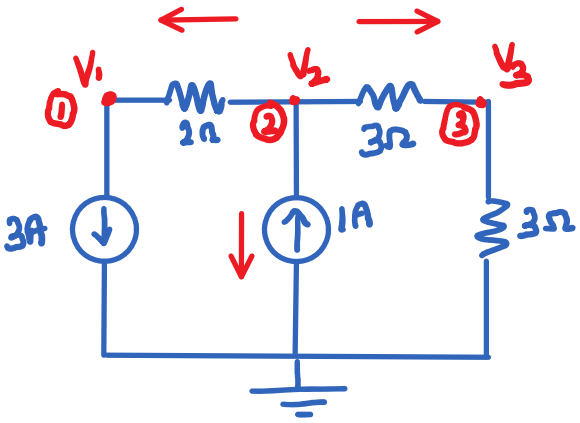
Solution:

Node 1 (KCL): $\mathbf{i_{12} + i_{1g} = 0}$

By Ohm's Law: $\mathbf{i_{12} = \frac{V_{12}}{2\Omega} = \frac{V_1 - V_2}{2}}$

By Inspection: $\mathbf{i_{1g} = 3A}$

Node 1: $\mathbf{\frac{V_1 - V_2}{2} + 3 = 0 \Rightarrow -V_1 + V_2 = 6}$ **(1)**



Node 2 (KCL): $i_{21} + i_{2g} + i_{23} = 0$

By Ohm's Law: $i_{21} = \frac{V_{21}}{2\Omega} = \frac{V_2 - V_1}{2}$

$$i_{23} = \frac{V_{23}}{3\Omega} = \frac{V_2 - V_3}{3}$$

By Inspection: $i_{2g} = -1A$

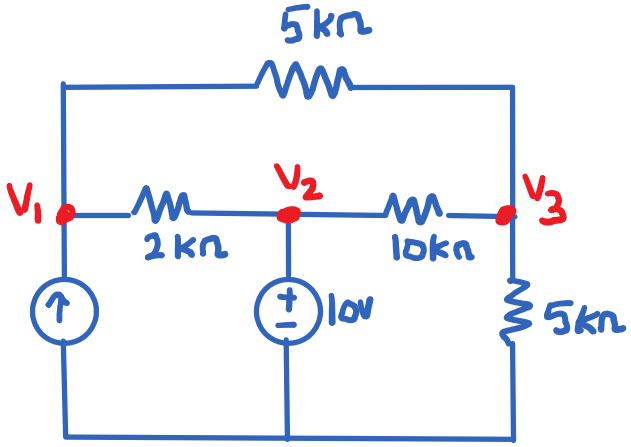
Node 2: $\frac{V_2 - V_1}{2} + \frac{V_2 - V_3}{3} - 1 = 0 \Rightarrow \boxed{-3V_1 + 4V_2 = 6}$ (2)

Solving (1) and (2),

$$\begin{bmatrix} -1 & 1 \\ -3 & 4 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 6 \\ 6 \end{bmatrix} \Rightarrow \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ -3 & 4 \end{bmatrix}^{-1} \begin{bmatrix} 10 \\ 2 \end{bmatrix}$$

$$\boxed{\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} -18 \\ -12 \end{bmatrix} \text{V}}$$

Example 2.3: Compute voltages V_1, V_2, V_3 in the circuit shown below.

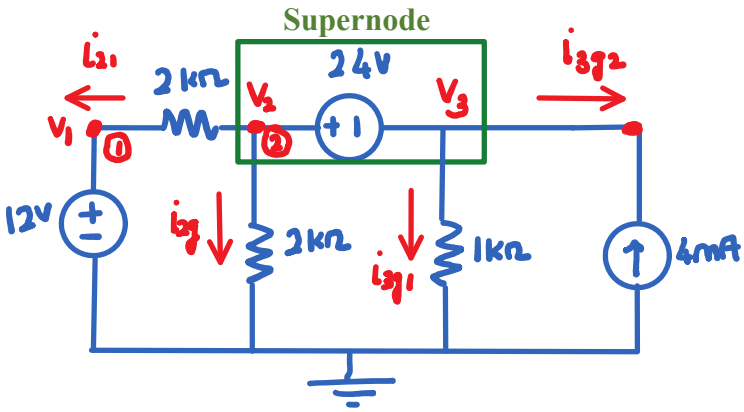


Solution: Solved in class as part of worksheet.

3. Supernodes

Earlier we had discussed the concept of superloops or "bigger loops". This concept came up when we had a current source in a branch that was common to two loops. The concept of supernodes is similar to superloops. We will use the idea of supernodes when there are multiple voltage sources in a circuit and some of them are not referenced to the ground in the circuit. We will see that similar to superloops, we will form a "bigger node" and then apply KCL to all currents coming out of the "bigger node". Let us look at the following example to get familiar with supernodes.

Example 3.1: Compute voltages $\mathbf{V_1, V_2, V_3}$ in the circuit shown below.



Solution:

By inspection: $\boxed{\mathbf{V_1 = 12\ V}}$

Supernode Equation (KCL):

Look at all the currents coming out of the circled supernode.

$$\mathbf{i_{21} + i_{2g} + i_{3g1} + i_{3g2} = 0}$$

$$\frac{\mathbf{V_2 - 12}}{\mathbf{2}} + \frac{\mathbf{V_2}}{\mathbf{2}} + \frac{\mathbf{V_3}}{\mathbf{1}} - \mathbf{4} = \mathbf{0}$$

$$\boxed{\mathbf{V_2 + V_3 = 10}} \quad (1)$$

Voltage relationships at supernode:

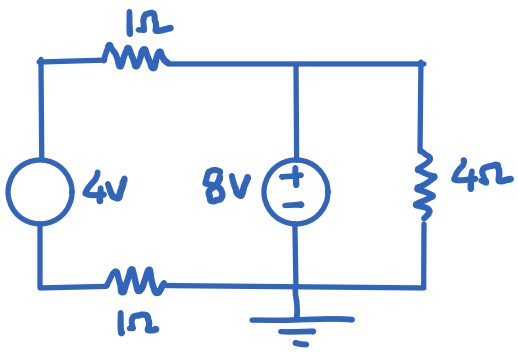
$$\boxed{\mathbf{V_2 - V_3 = 24}} \quad (2)$$

Solving (1) and (2),

$$\begin{bmatrix} \mathbf{1} & \mathbf{1} \\ \mathbf{1} & \mathbf{-1} \end{bmatrix} \begin{bmatrix} \mathbf{V_2} \\ \mathbf{V_3} \end{bmatrix} = \begin{bmatrix} \mathbf{10} \\ \mathbf{24} \end{bmatrix} \Rightarrow \begin{bmatrix} \mathbf{V_2} \\ \mathbf{V_3} \end{bmatrix} = \begin{bmatrix} \mathbf{1} & \mathbf{1} \\ \mathbf{1} & \mathbf{-1} \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{10} \\ \mathbf{24} \end{bmatrix}$$

$$\boxed{\begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \end{bmatrix} = \begin{bmatrix} \mathbf{17} \\ \mathbf{-7} \end{bmatrix} \mathbf{V}}$$

Example 3.2: Compute voltages $\mathbf{V_1, V_2, V_3, V_4}$ in the circuit shown below.



Solution:

By inspection: $\mathbf{V_3 = V_4 = 8V}$

Supernode Equation (KCL):

$$i_{1g} + i_{23} = 0$$

$$\frac{V_1 - 0}{1} + \frac{V_2 - V_3}{3} = 0 \Rightarrow 3V_1 + V_2 = 8 \quad (1)$$

Voltage relationships at supernode:

$$-\mathbf{V_1} + \mathbf{V_2} = \mathbf{4} \qquad \textbf{(2)}$$

Solving (1) and (2),

$$\begin{bmatrix} \mathbf{3} & \mathbf{1} \\ \mathbf{-1} & \mathbf{1} \end{bmatrix} \begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \end{bmatrix} = \begin{bmatrix} \mathbf{8} \\ \mathbf{4} \end{bmatrix} \Rightarrow \begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \end{bmatrix} = \begin{bmatrix} \mathbf{3} & \mathbf{1} \\ \mathbf{-1} & \mathbf{1} \end{bmatrix}^{\mathbf{-1}} \begin{bmatrix} \mathbf{8} \\ \mathbf{4} \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \end{bmatrix} = \begin{bmatrix} \mathbf{1} \\ \mathbf{5} \end{bmatrix} \mathbf{V}$$

Alternate method: When we first look at example 3.2, it seems to be a supernode problem. As we just saw applying the supernode node method to the problem does work! At the same time the problem can be simplified. This is shown in Fig. 3.1 below. As shown in Fig. 3.1 (a), the highlighted elements are series connected and hence their order can be interchanged. Fig. 3.1 (b) shows the circuit after rearranging the elements. The problem can be solved using node voltage method by setting up one equation for node 2.